VESDA Display Standards Updates

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VESDA Compliance Program Manager
October 12, 2023
Agenda

• VESA Overview and Standards Updates: Jim Choate, VESA
• DP Alt Mode v 2.1 Overview and Updates: Tim Wei, Ellisys
• DisplayPort Link Layer CTS v 2.1, Presented by Alok Soni, Teledyne LeCroy
• ClearMR Testing Challenges, Presented by Lexus Lee, Allion Labs
• VESA Compliance Program Updates: Jim Choate
• Summary, Questions & Answers
• Demos
About VESA

- A growing global industry alliance with more than 340 members. Strong growth in membership.

Mission to develop, promote and support ecosystem of vendors and certified interoperable products for the electronics industry.

*Develops OPEN standards, contribution is open to all companies at all stages of development*
• Leading PC/computer, display, hardware, software, and component manufacturers worldwide

• VESA membership continues to grow the most in Asia
VESAs Local Asian Support Capability

- VESA has long had a dedicated Japan Task Group with charter to promote the development of design tools and reference guides, PlugTests, educational seminars, and other activities for the benefit of VESA member companies, particularly those in Japan.

- **NEW:** VESA has added to its local support to Asia to address growing regional membership needs

- China (Mainland) and Taiwan are the fastest growing areas for VESA's membership.

- **Kellen** is VESA's Representative for all Chinese speaking areas of Asia

- This partnership will provide members with a communication option in their native language. Kellen will handle membership related activities including, new membership requests, renewals, PlugTest and event support and translation of VESA member messaging, etc.
VESA Standards Enable Many Market Segments...

Monitors, PCs and laptops

Smartphones and tablets

Gaming consoles and headsets

Automotive

Digital projectors

Digital signage / kiosks
...As Well as Many Aspects of Display Technology

Display Interfaces
- DisplayPort
- Embedded DisplayPort (eDP)
- DisplayPort Alt Mode
- DisplayPort Tunneling (USB4 and Thunderbolt)
- DP Automotive Extensions (DP AE)

Display Data Compression
- Display Stream Compression (DSC)
- VESA Display Codec for Mobile (VDC-M)

Display Metrology
- Standardized Display Performance Measurement
- VESA DisplayHDR Certification (High Dynamic Range)
- VESA ClearMR
- VESA AdaptiveSync

Display Capability Parameters
- DisplayID
- Extended Display Identification Data (EDID)
- Multi-Display Interface
- Bulk Display Protocol
DisplayPort 2.1 Summary

• DisplayPort v2.1 was released in October 2022

• DisplayPort 2.1 brings DisplayPort into convergence with USB4 PHY specifications to ensure the highest video performance across a broad range of consumer products

• Added DP40 (up to UHBR10) and DP80 (up to UHBR20) cable specifications and certification

• Enhanced DP connectors provide highest performance with full sized DP and mDP connectors

DisplayPort 2.1 enables up to 3X increase in video bandwidth performance.

First standard to support 8K resolution (7680 x 4320) at 60 Hz refresh rate with full-color 4:4:4 resolution, including with 30 bits per pixel (bpp) for HDR-10 support.

Beyond 8K resolutions achieved with maximum link rate to up to 20 Gbps/lane and more efficient 128b/132b channel coding.
# DisplayPort 2.1 Resolution Capability

## (Single Display Examples)

<table>
<thead>
<tr>
<th>Port Configuration</th>
<th>DisplayPort 1.4a</th>
<th>DisplayPort 2.1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>No Compression</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 Lanes, max link rate</td>
<td>5K (5120x2800)@60fps 24bpp</td>
<td>10K (10240x4320)@60fps 24bpp</td>
</tr>
<tr>
<td>2 Lanes, max link rate</td>
<td>4K (3840x2160)@60fps 24bpp</td>
<td>8K (7680x4320)@30fps 30bpp</td>
</tr>
<tr>
<td><strong>With Compression (DSC)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 Lanes, max link rate</td>
<td>8K (7680x4320)@60fps 30bpp</td>
<td>16K (15360x8460)@60fps 30bpp</td>
</tr>
<tr>
<td>2 Lanes, max link rate</td>
<td>5K (5120x2800)@60fps 24bpp</td>
<td>10K (10240x4320)@72fps 30bpp</td>
</tr>
</tbody>
</table>

**Notes:**
- 2 Lane configuration is common for USB-C DP Alt Mode
- All above modes assume full 4:4:4 color encoding
- 30bpp is required for DisplayHDR operation

**Key:**
- DSC = Display Stream Compression
- fps = frames per second
- bpp = bits per pixel
Optimization for Shared Interface Use

• Numerous specification enhancements to simplify the use of DisplayPort as an ingredient in the following interface examples:
  • The USB-C connector, using the DisplayPort Alt Mode (DP Alt Mode)
  • VESA Embedded DisplayPort Standard (eDP)
  • ThunderBolt
  • USB4
  • Wireless interfaces
DP 40/DP 80 Cable Specification and Certification

• Developed as part of DP 2.1 specification update
• DP40 and DP80 Certified cables provide added assurance of smooth operation and full compliance at the UHBR data rates
• Dozens of DP40 and DP80 cables have been certified since launch of program
VESDA Technology Development Areas
VESA technology development

• VESA members are collaborating on several key technology areas

• AR/VR Task Group
  • Specification is released. Work started on CTS
  • Focused on creating solutions roadmap to meet performance, power and implementation requirements for future AR/VR needs

• DP Automotive Extension Task Group
  • Working with automotive industry to address needs for high-resolution performance in this market segment
  • Working on DP AE specification and CTS

• Bulk Display Protocol
  • BDP specification and CTS nearing release

• Display Performance Metrics Task Group
  • DisplayHDR, ClearMR, AdaptiveSync
USB4 Overview

- Runs over USB Type-C® interconnect
- Tunnels USB3, PCIe and DP protocols
- Signaling rates of 10 or 20 Gbps (10 to 40Gbps aggregated b/w)
- Helps converge USB Type-C connector ecosystem to minimize end-user confusion
VESA Display Performance Metrics Standards Very Successful
DP Alt Mode v 2.1 Overview and Updates

Presented by Tim Wei, Senior Application Engineer, Ellisys
DP Alt Mode v 2.1 Overview and Updates

Tim Wei – Senior Application Engineer, Ellisys

VESAs Seoul Workshop
October 10, 2023
USB Test and Analysis Solutions

USB Explorer™ 350
Multi-function USB Type-C®, USB 3.2, and Power Delivery Protocol Test Platform
VESPA-Approved Tester for DisplayPort ALT Mode

Type-C Tracker™
Protocol and Electrical Analysis Tool for USB Type-C® Standards
Includes DP AUX and DP ALT Support
Example USB Type-C Configurations

Either end can serve as USB Host, USB-PD Power Consumer, and DisplayPort Video Source (these services are independent of each other.)
DP Alt Mode over USB-C Ecosystem is Mainstream

All types of certified adapters available

• C to DP adapters, Multifunction docks
• Type C protocol converters (HDMI, VGA, DVI) using DP Alt Mode

More are certified every week

▪ Major PC OEMs continue to launch new products with DP Alt Mode over USB-C
▪ Major Display OEMs continue to add USB-C inputs to their products
USB-C Connector Functional Extension
DP Alt Mode

• A passive Full Feature USB Type-C to Type-C cable can carry up to four DisplayPort lanes
  • Same performance and features as a standard DisplayPort connection
  • Allows DisplayPort data rates to increase in the future, since the USB Type-C connector has very high data rate capability

• DisplayPort can be combined with USB 3.2 operation over the same USB Type-C cable

• USB 2.0 and USB Power Delivery is available in all configurations
• Uses a standard “Full Feature” USB-C to USB-C cable which is designed to include DisplayPort
• The above configuration uses two high-speed lanes each for DisplayPort and USB 3.2
  • Ideal for docking stations, or for displays or TVs that include USB 3.2 functions
4xDP Over a USB Type-C to USB Type-C Full Feature Passive Cable

- Utilizes optional DP Alt Mode capability of USB Type-C connector
- DisplayPort can use all four high speed lanes to deliver full DisplayPort performance
- The DisplayPort AUX Channel uses the SBU pins
- The DisplayPort HPD / IRQ is transmitted over the CC pin using the USB-PD protocol
- USB 2.0 and USB Power Delivery always available
### Typical DisplayPort Alternate Mode Flow

<table>
<thead>
<tr>
<th>Item</th>
<th>Directed</th>
<th>Bit Rate</th>
<th>Source Direct</th>
<th>Sink Direct</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOP Discover Identity (x 4)</td>
<td></td>
<td>296.78 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>Source Capabilities (1 Fixed 5V 1.5A)</td>
<td></td>
<td>296.63 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>Request (1 Fixed 5V 1.5A, Requested 1.5A, Max 1.5A)</td>
<td>Accepted</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PowerOn</td>
<td></td>
<td>296.67 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>DisplayPort Discover Modes Ack (UFP_D Capable, CD)</td>
<td></td>
<td>296.63 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>DisplayPort Discover Modes Ack (UFP_D Capable, CD)</td>
<td></td>
<td>296.63 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>Apple Discover Modes</td>
<td>Ack (0x00000002, 0x00000003)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Apple Discover Modes</td>
<td></td>
<td>296.63 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>Apple Discover Modes Ack (0x00000002, 0x00000001)</td>
<td></td>
<td>296.63 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>DisplayPort Enter Mode (Mode=1)</td>
<td>Ack</td>
<td>296.64 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>DisplayPort Enter Mode (Mode=1)</td>
<td></td>
<td>296.64 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>DisplayPort Enter Mode Ack</td>
<td></td>
<td>300.481 kbit/s</td>
<td>IN</td>
<td>OK</td>
</tr>
<tr>
<td>DisplayPort Status Update (DFP_D connected, Not Enabled)</td>
<td>Ack (UFP_D connected, Enabled, HFP Low)</td>
<td>296.64 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>DisplayPort Status Update (DFP_D connected, Not Enabled)</td>
<td></td>
<td>296.64 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>DisplayPort Status Update Ack (UFP_D connected, Enabled, HFP Low)</td>
<td></td>
<td>300.533 kbit/s</td>
<td>IN</td>
<td>OK</td>
</tr>
<tr>
<td>DisplayPort Configure (Set Config as DP Sink, D)</td>
<td>Ack</td>
<td>296.64 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>DisplayPort Configure (Set Config as DP Sink, D)</td>
<td></td>
<td>296.64 kbit/s</td>
<td>OUT</td>
<td>OK</td>
</tr>
<tr>
<td>DisplayPort Configure Ack</td>
<td></td>
<td>300.481 kbit/s</td>
<td>IN</td>
<td>OK</td>
</tr>
</tbody>
</table>
DisplayPort Alternate Mode 2.1 Update

- SVDM Header Update (by USB PD Spec)
- Cable DP Capabilities VDO update to support UHBR20 and UHBR13.5
  - Both passive and active cables
- SOP' Active Cable DisplayPort Configurations VDO update
- DP Capabilities VDO Update (DPAM Version field)
- SOP DisplayPort Configurations VDO Update
  - Cable information
  - DPAM Version
- DisplayPort Status Update VDO Update
## SVDM Header Update

<table>
<thead>
<tr>
<th>Time</th>
<th>Field Description</th>
<th>Value Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>12:11</td>
<td>Structured VDM Version (Minor)&lt;sup&gt;a&lt;/sup&gt;</td>
<td>Version number (Minor) of the SVDM (not the USB PD version number).&lt;br&gt;00b = Version 2.0 or earlier&lt;br&gt;01b = Version 2.1&lt;br&gt;All other values are RESERVED.</td>
</tr>
<tr>
<td>14:13</td>
<td>Structured VDM Version (Major)&lt;sup&gt;a&lt;/sup&gt;</td>
<td>Version number (Major) of the SVDM (not the USB PD version number).&lt;br&gt;00b = Version 2.0 or earlier.&lt;br&gt;01b = Version 2.x. (x indicates SVDM minor version)&lt;br&gt;All other values are RESERVED.</td>
</tr>
</tbody>
</table>

12:11 was reserved
### Table 4-5: SOP+ Cable DP Capabilities (VDO in the Responder USB PD Discover Modes VDM)

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>RESERVED</td>
<td>RESERVED (always 000b).</td>
</tr>
<tr>
<td>5:2</td>
<td>Signaling for Transport of DisplayPort Protocol&lt;sup&gt;a&lt;/sup&gt;</td>
<td>XXX1b = Supports all defined DP bit rates up to HBR3. XX1Xb = Supports DP bit rate UHBR10. X1XXb = Supports DP bit rate of UHBR20 (e.g., 0111b supports all DP bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.&lt;sup&gt;4&lt;/sup&gt;</td>
</tr>
<tr>
<td>7:6</td>
<td>RESERVED</td>
<td>RESERVED (always 000b).</td>
</tr>
<tr>
<td>15:8</td>
<td>DP Source Device Pin Assignments Supported</td>
<td>0Ch = Pin Assignments C and D are supported. 10h = USB-C and DP connector Pin Assignment E is supported. All other values are RESERVED.</td>
</tr>
<tr>
<td>23:16</td>
<td>DP Sink Device Pin Assignments Supported</td>
<td>0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10h = USB-C and DP connector Pin Assignment E is supported. All other values are RESERVED.</td>
</tr>
<tr>
<td>25:24</td>
<td>RESERVED</td>
<td>RESERVED (always 000b).</td>
</tr>
<tr>
<td>29&lt;sup&gt;6&lt;/sup&gt;</td>
<td>UHBR13.5</td>
<td>0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.&lt;sup&gt;4&lt;/sup&gt;</td>
</tr>
<tr>
<td>27</td>
<td>RESERVED</td>
<td>RESERVED (always 0).</td>
</tr>
<tr>
<td>29:28&lt;sup&gt;5&lt;/sup&gt;</td>
<td>Active Component</td>
<td>00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.</td>
</tr>
<tr>
<td>31:30</td>
<td>DPAM Version</td>
<td>00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.</td>
</tr>
</tbody>
</table>

---

### Table 4-2: Active Cable DP Capabilities (VDO in the Responder USB PD Discover Modes VDM)

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>RESERVED</td>
<td>RESERVED (always 000b).</td>
</tr>
<tr>
<td>5:2</td>
<td>Signaling for Transport of DisplayPort Protocol&lt;sup&gt;a&lt;/sup&gt;</td>
<td>XXX1b = Supports DP bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.</td>
</tr>
<tr>
<td>7:6</td>
<td>RESERVED</td>
<td>RESERVED (always 000b).</td>
</tr>
<tr>
<td>15:8</td>
<td>DP Source Device Pin Assignments Supported</td>
<td>0Ch = Pin Assignments C and D are supported. All other values are RESERVED.</td>
</tr>
<tr>
<td>23:16</td>
<td>DP Sink Device Pin Assignments Supported</td>
<td>0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). All other values are RESERVED.</td>
</tr>
<tr>
<td>31:24</td>
<td>RESERVED</td>
<td>RESERVED (always 000b).</td>
</tr>
</tbody>
</table>

<sup>a</sup> "X" value indicates "Don't Care."
### Table 4.7: SOP Active Cable DisplayPort Configurations

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Select Configuration</td>
<td>00b = Set configuration for USB, 01b = Set configuration for active cable as a DP Source device (UPF_U is a DP Source device), 10b = Set configuration for active cable as a DP Sink device (UPF_U is a DP Sink device), 11b = RESERVED.</td>
</tr>
<tr>
<td>5:2</td>
<td>Signaling for Transport of DisplayPort Protocol</td>
<td>0h = Bit rate is unspecified (used only when the Select Configuration field is programmed for USB Configuration), 1h = Select DP bit rates and electrical settings. All other values are RESERVED.</td>
</tr>
<tr>
<td>7:6</td>
<td>RESERVED</td>
<td>RESERVED (always 00b).</td>
</tr>
<tr>
<td>15:8</td>
<td>Configure Active Cable Pin Assignment</td>
<td>00h = Deselect pin assignment, 04h = Select Pin Assignment C, 08h = Select Pin Assignment D, 10h = Select Pin Assignment E, All other values are RESERVED.</td>
</tr>
<tr>
<td>31:16</td>
<td>RESERVED</td>
<td>RESERVED (always 0000000h).</td>
</tr>
</tbody>
</table>

### Table 4.3: Active Cable DisplayPort Status Update

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:0</td>
<td>RESERVED</td>
<td>RESERVED (always 00b).</td>
</tr>
<tr>
<td>3</td>
<td>Enabled</td>
<td>0 = Active cable DP functionality is disabled, 1 = Active cable DP functionality is enabled and operational.</td>
</tr>
<tr>
<td>31:4</td>
<td>RESERVED</td>
<td>RESERVED (always 00000000b).</td>
</tr>
</tbody>
</table>
### Table 5-6: DP Capabilities (VDO in the Responder USB PC Discover Modes VDM)

<table>
<thead>
<tr>
<th>BN(s)</th>
<th>Description</th>
<th>Values*</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Port Capability</td>
<td>0b = RESERVED. 1b = DP Sink Device Capable (including DP Branch device). 10b = DP Source Device Capable (including DP Branch device). 11b = Both DP Source and Sink Device Capable.</td>
</tr>
<tr>
<td>5:2</td>
<td>Signaling for Transport of DisplayPort Protocol</td>
<td>XXXX1 = Supports DP latency and electrical settings (shall always be set apart from diagnostic purposes). XXXX0 = RESERVED. XXXX0 = RESERVED. XXXX0 = RESERVED.</td>
</tr>
<tr>
<td>6</td>
<td>Receptacle Indication</td>
<td>0 = DP interface is present on a USB-C plug. 1 = DP interface is present on a USB-C receptacle.</td>
</tr>
<tr>
<td>7</td>
<td>USB 2.0 Signaling Not Used</td>
<td>0 = USB 2.0 may be needed on A6 = A7 or B6 = B7 while in DisplayPort Configuration. 1 = USB 2.0 is not needed on A6 = A7 or B6 = B7 while in DisplayPort Configuration.</td>
</tr>
</tbody>
</table>

### Table 5-6: DP Capabilities (VDO in the Responder USB PD Discover Modes VDM)

<table>
<thead>
<tr>
<th>BN(s)</th>
<th>Description</th>
<th>Values*</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Port Capability</td>
<td>0b = RESERVED. 01b = DP Sink device-capable (including DP Branch device). 10b = DP Source device-capable (including DP Branch device). 11b = Both DP Source and Sink device-capable.</td>
</tr>
<tr>
<td>5:2</td>
<td>Signaling for Transport of DisplayPort Protocol</td>
<td>XXXX0 = Supports DP latency rates and electrical settings (shall always be set apart from diagnostic purposes). XXXX0 = RESERVED. XXXX0 = RESERVED. XXXX0 = RESERVED. XXXX0 = RESERVED.</td>
</tr>
<tr>
<td>6</td>
<td>Receptacle Indication</td>
<td>0 = DP interface is present on a USB-C plug. 1 = DP interface is present on a USB-C receptacle.</td>
</tr>
<tr>
<td>7</td>
<td>USB 2.0 Signaling Not Used</td>
<td>0 = USB 2.0 may be needed on A6 = A7 or B6 = B7 while in DisplayPort Configuration. 1 = USB 2.0 is not needed on A6 = A7 or B6 = B7 while in DisplayPort Configuration.</td>
</tr>
</tbody>
</table>

If SVDM Version is 2.1 or higher, DPAM Version field is applicable else this field shall be set to 00b.
A Bit More Background

From DisplayPort Alt Mode 2.0 Spec

Future versions of this Standard may describe other modes associated with the DP_SID. Such modes shall be identified by having a non-zero value in bits 31:24 of the VDO. The DFP_U shall examine the list of modes returned until it finds 0s in bits 31:24 of the VDO and a non-zero value in bits 23:0 of the VDO (i.e., DP Capabilities). The DFP_U and UFP_U shall use the corresponding offset (indexed from 1) as the Object Position in the following commands:
SOP DisplayPort Configurations VDO Update

This is the most challenging part for DPAM 2.1 DFP_U
**DisplayPort Status Update VDO Update**

<table>
<thead>
<tr>
<th>Table 5-7: DisplayPort Status Update</th>
<th>Bit(s)</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>DP Source/Sink Device Connected</td>
<td>00b – Neither a DP Source device nor DP Sink device is connected, –or– the adapter is disabled. 01b = DP Source device is connected. 10b = DP Sink device is connected. 11b = Both a DP Source and Sink device are connected.</td>
<td></td>
</tr>
<tr>
<td>2b</td>
<td>Power Low</td>
<td>0 = Adapter is not in low power state or functioning normally or is disabled. 1 = Adapter has detected low power and disabled DP support.</td>
<td></td>
</tr>
<tr>
<td>3b</td>
<td>Enabled</td>
<td>0 = Adapter DP functionality is disabled. 1 = Adapter DP functionality is enabled and operational.</td>
<td></td>
</tr>
<tr>
<td>4b</td>
<td>Multifunction Preferred</td>
<td>0 = No preference for multifunction. 1 = Multifunction is preferred.</td>
<td></td>
</tr>
<tr>
<td>5b</td>
<td>DisplayPort/USB Configuration Request</td>
<td>0 = Request change to DisplayPort Configuration (if currently in USB Configuration). 1 = Request change to USB Configuration (if currently in DisplayPort Configuration).</td>
<td></td>
</tr>
<tr>
<td>6b</td>
<td>Exit DisplayPort Alt Mode Request</td>
<td>0 = Maintain the current mode. 1 = Request exit from DisplayPort Alt Mode (if currently in DisplayPort Alt Mode).</td>
<td></td>
</tr>
<tr>
<td>7b</td>
<td>HPD State</td>
<td>0 = HPD_Low. 1 = HPD_High.</td>
<td></td>
</tr>
<tr>
<td>8b</td>
<td>IRQ_HPDP</td>
<td>0 = IRQ_HPDP has not been issued since the last status message. 1 = IRQ_HPDP.</td>
<td></td>
</tr>
<tr>
<td>9b</td>
<td>NO_DPAM_SUSPEND</td>
<td>0 = UFP_U DP Sink device has no preference for entry into low power state. 1 = UFP_U DP Sink device prefers not to enter low power state.</td>
<td></td>
</tr>
<tr>
<td>31:10</td>
<td>RESERVED</td>
<td>RESERVED (always 00000000h).</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 5-8: DisplayPort Status Update</th>
<th>Bit(s)</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>DP Source/Sink Device Connected</td>
<td>00b – Neither a DP Source device nor DP Sink device is connected, –or– the adapter is disabled. 01b = DP Source device is connected. 10b = DP Sink device is connected. 11b = Both a DP Source and Sink device are connected.</td>
<td></td>
</tr>
<tr>
<td>2b</td>
<td>Power Low</td>
<td>0 = Adapter is functioning normally or is disabled. 1 = Adapter has detected low power and disabled DP support.</td>
<td></td>
</tr>
<tr>
<td>3b</td>
<td>Enabled</td>
<td>0 = Adapter DP functionality is disabled. 1 = Adapter DP functionality is enabled and operational.</td>
<td></td>
</tr>
<tr>
<td>4b</td>
<td>Multifunction Preferred</td>
<td>0 = No preference for multifunction. 1 = Multifunction is preferred.</td>
<td></td>
</tr>
<tr>
<td>5b</td>
<td>DisplayPort/USB Configuration Request</td>
<td>0 = Request change to DisplayPort Configuration (if currently in USB Configuration). 1 = Request change to USB Configuration (if currently in DisplayPort Configuration).</td>
<td></td>
</tr>
<tr>
<td>6b</td>
<td>Exit DisplayPort Alt Mode Request</td>
<td>0 = Maintain the current mode. 1 = Request exit from DisplayPort Alt Mode (if currently in DisplayPort Alt Mode).</td>
<td></td>
</tr>
<tr>
<td>7b</td>
<td>HPD State</td>
<td>0 = HPD_Low. 1 = HPD_High.</td>
<td></td>
</tr>
<tr>
<td>8b</td>
<td>IRQ_HPDP</td>
<td>0 = IRQ_HPDP has not been issued since the last status message. 1 = IRQ_HPDP.</td>
<td></td>
</tr>
<tr>
<td>31:9</td>
<td>RESERVED</td>
<td>RESERVED (always 00000000h).</td>
<td></td>
</tr>
</tbody>
</table>

Three New timers:
- tAttentionSpacing min 10ms
- tHpdConvertPd max 5ms
- tAttentionToDPConfigure max 500ms
## DPAM Version Resolution

<table>
<thead>
<tr>
<th>DPAM Version</th>
<th>DFP_U</th>
<th>Cable</th>
<th>UFP_U</th>
<th>DPAM Version Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPAM Version</td>
<td>2.0 or earlier</td>
<td>2.0 or earlier</td>
<td>2.0 or earlier</td>
<td>2.0 or earlier&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>2.1 or higher</td>
<td>2.0 or earlier</td>
<td>2.0 or earlier</td>
<td>2.0 or earlier&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>2.0 or earlier</td>
<td>2.1 or higher</td>
<td>2.0 or earlier</td>
<td>2.0 or earlier&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>2.0 or earlier</td>
<td>2.0 or earlier</td>
<td>2.1 or higher</td>
<td>2.0 or earlier&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>2.1 or higher</td>
<td>2.1 or higher</td>
<td>2.0 or earlier</td>
<td>2.0 or earlier&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>2.0 or earlier</td>
<td>2.1 or higher</td>
<td>2.1 or higher</td>
<td>2.0 or earlier&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>2.1 or higher</td>
<td>2.0 or earlier</td>
<td>2.1 or higher</td>
<td>DPAM 2.1 or higher&lt;sup&gt;c&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>2.1 or higher</td>
<td>2.1 or higher</td>
<td>2.1 or higher</td>
<td>2.1 or higher&lt;sup&gt;d&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

<sup>a</sup> If Initiator and Responder support SVDM Version 2.0 or earlier and if DisplayPort Alternate Mode is supported all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.0 or earlier.

<sup>b</sup> If Initiator and Responder both support SVDM Version 2.1 or higher and if either Initiator or Responder supports DPAM Version 2.0 or earlier, then all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.0 or earlier.

<sup>c</sup> When DPAM 2.1 or higher DFP_U and DPAM 2.1 or higher UFP_U are connected with a legacy active DPAM 2.0 cable, then the system shall exchange all DP Capabilities as per DisplayPort Alt Mode on USB Type-C specification 2.1 or higher but support HBR3 rates.

<sup>d</sup> If Initiator and Responder both support SVDM Version 2.1 or higher and DPAM Version 2.1 all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.1 or higher.
Typical DPAM 2.1 Flow

<table>
<thead>
<tr>
<th>Item</th>
<th>Structured VDM Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOP Discover Identity &gt; Ack (Type-C to Type-C 3A)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>Source Capabilities (max SV 0.5A)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>Request (max SV 0.5A, Requested 0.5A, Max 0.5A) &gt; Accepted</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>PsRdy</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>Discover Identity &gt; Ack (POUSB Peripheral, POUSB Host)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>Discover SVIDs &gt; Ack (DisplayPort)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>Discover SVIDs</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>Discover SVIDs Ack (DisplayPort)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>DisplayPort Discover Modes &gt; Ack (UPF_D Capable, CDE)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP Discover SVIDs &gt; Ack (Intel, DisplayPort)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Discover Modes &gt; Ack (DPP_D=CD, UPF_D=CD)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Discover Modes</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Discover Modes Ack (DPP_D=CD, UPF_D=CD)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Discover Modes Ack (Thunderbolt Cable, No retimer, 20Gb/s)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP Intel Discover Modes</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP Intel Discover Modes Ack (Thunderbolt Cable, No retimer, 20Gb/s)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>DisplayPort Enter Mode (Mode=1) &gt; Ack</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Enter Mode (Mode=1)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Enter Mode Ack</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>DisplayPort Enter Mode (Mode=1) &gt; Ack</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Enter Mode (Mode=1)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Enter Mode Ack</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Status Update (DPP_D connected, Not Enabled) &gt; Ack</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Status Update (DPP_D connected, Not Enabled)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>DisplayPort Status Update (DPP_D connected, Not Enabled)</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Configure (Set Config as DP Sink, C) &gt; Ack</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Configure</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>DisplayPort Configure (Set Config as DP Sink, C) &gt; No Response</td>
<td>Version 2.1</td>
</tr>
<tr>
<td>SOP DisplayPort Configure (Set Config as DP Sink, C)</td>
<td>Version 2.1</td>
</tr>
</tbody>
</table>
DPAM 2.1 CTS Update (1)

• All these tests were added to make sure the DFP_U set correct cable information in DisplayPort Configurations VDO
DPAM 2.1 CTS Update (2)

• DPAM Version Resolution Tests
  - 10.3.23 DPAM Version 2.1 DFP_U Connected to DPAM Version 2.0 or 2.1 UFP_U
  - 10.4.3 DPAM Version 2.1 Cable Connected to DPAM Version 2.0 or 2.1 DFP_U
  - 10.2.8 DPAM Version 2.1 UFP_U Connected to DPAM Version 2.0 or 2.1 DFP_U

- 10.6.3 DPAM Discovery Interoperability Flow for USB-C to DP Adapters
Questions?

DisplayPort over USB-C
The most advanced display connection now uses the most versatile connector.

Learn More  Go to www.displayport.org
DisplayPort Link Layer CTS v 2.1

Presented by Alok Soni, Teledyne LeCroy
DP v2.1 Link Layer Compliance Tests

• Test Setup Details
• DP Source Compliance Tests
• DP Sink Compliance Tests
• LTTPR and DP Tunnel Compliance Tests
• DP Link Layer Test Equipment from Teledyne LeCroy
• Q/A

Presenter: Alok K. Soni
Teledyne LeCroy
Alok.Soni@Teledyne.com
Test Setup Details:

Source DUT  
LTTP R

TE (Reference Sink)

Source DUT  
LTTP R

Sink DUT

TE (Reference Source)

Sink DUT

LTTPR or DP Tunnel DUT

Source DUT  
LTTP R

Sink DUT

Source DUT  
LTTP R

Sink DUT

LTTPR or DP Tunnel DUT

Source DUT  
LTTP R

Sink DUT

Source DUT  
LTTP R

Sink DUT

LTTPR or DP Tunnel DUT

Source DUT  
LTTP R

Sink DUT

Source DUT  
LTTP R

Sink DUT

LTTPR or DP Tunnel DUT

Source DUT  
LTTP R

Sink DUT

Source DUT  
LTTP R

Sink DUT

LTTPR or DP Tunnel DUT

Source DUT  
LTTP R

Sink DUT

Source DUT  
LTTP R

Sink DUT

LTTPR or DP Tunnel DUT

Source DUT  
LTTP R

Sink DUT

Source DUT  
LTTP R

Sink DUT

LTTPR or DP Tunnel DUT
DP Source Device Tests:

• How to Tests
  • CDF Entries to provide supported capabilities of Source DUT.
  • Fill out information about what DUT support for example:
    • Lane count, Link Rate, Colors, BPC, Test Automation, Video format Supported, FEC, DSC, Adaptive Sync etc.
• Select group of tests to run
• Execute the tests (may require operator interaction during the tests).
• End of the test, generate reports and logs for certification.
DP Source Device Tests:

- AUX Tests
- HPD Tests
- EDID Protocol Tests
- DPCD Read Tests
- AUX read interval testing for Link Training
- Link Training Tests HBR rates
- Link Training Tests UHBR rates
- Link Maintenance Tests
DP Source Device Tests:

• Video Timestamp generation tests (HBR and UHBR)
• Video Tests (HBR and UHBR)
  • All color and bit per components tests
  • Least pack tests
  • Most pack tests
• Power Management tests
• *Audio Tests (new version for UHBR rate under development)
• FEC Tests
• DSC Tests
DP Source Device Tests:

- EDID/Display ID and/or Native Display ID tests
  - Video tests
  - Audio tests
  - EDDC tests
  - Display ID tests
  - Adaptive Sync tests
- Adaptive Sync Tests
  - Fix average vtotal tests
  - Adaptive vtotal tests
- LTTPR tests
  - Tests Source DUT handling of LTTPR.
DP Sink Device Tests:

• How to Tests
  • No CDF needed Reference Source (TE) will read the capabilities and run/skip the tests accordingly.
  • Select group of tests to run
  • Execute the tests (may require operator interaction during the tests).
  • End of the test generate reports and logs.
DP Sink Device Tests:

- AUX Tests (syntax and procedure tests)
- DPCD Declaration Tests
  - Certain DPCD values for various state setup by Ref Source.
  - Symbol error tests
- Link Training Tests HBR rates
- Link Training Tests UHBR rates
- Link Maintenance Tests
- Video Tests based on EDID and fallback capability
- Power management tests
- Audio tests (UHBR rate tests are under development)
DP Sink Device Tests:

- Split SDP tests
- FEC tests including error counter validation
- DSC tests
- EDID, embedded Display ID tests
  - EDID Base block tests
  - CTS block tests
  - Embedded Display ID (rev 1.x and 2.x) tests
- *Native Display ID tests
  - Many tests under development.
- Adaptive Sync tests
- Embedded LTTPR tests (Capability and Link Training)
LTTPR and DP Tunnel Tests:

Note: DP Tunnel here is discrete DP Tunnel treated as pseudo LTTPR.

• How to Tests
  • No CDF needed Reference Source (TE) will read the capabilities and run/skip the tests accordingly.
  • Select group of tests to run
  • Execute the tests (may require operator interaction during the tests).
  • End of the test generate reports and logs.
LTTPR and DP Tunnel Tests:

- Capability tests and DPCD values via LTTPR.
- HBR Link Training Tests
  - Non-LTTPR
  - Transparent mode
  - Non-Transparent mode
- UHBR Link Training Tests
- Link Maintenance tests
- Symbol and FEC error counter tests.
- Split SDP handling tests
- Video/DSC tests with and without HDCP in SST or MST mode.
Teledyne LeCroy DP Test Equipment:

- **M42D**
  - Supports DP2.1 link layer CTS
  - Supports DP1.4 link layer CTS
  - EDID/Display ID CTS and Adaptive Sync CTS
  - Verity of Functional Tests
  - Passive Monitoring

- **M21** (handheld device)
  - Supports DP2.1 analyzer capability for functional testing.
  - Supports other protocol for video generation and analyzer.
Teledyne LeCroy DP Test Equipment:

- **M41D**
  - Supports DP1.2 link layer CTS
  - Supports DP1.4 link layer CTS
  - EDID CTS

- **980 with DP1.4 and DP 1.2 card**
  - Supports DP1.2 link layer CTS
  - Supports DP1.4 link layer CTS
  - EDID CTS
Question/Answer
ClearMR Testing Challenges
Presented by Lexus Lee, Allion Labs
VESA ClearMR Testing Challenges
OVERVIEW

• VESA ClearMR Testing Challenges

• VESA AdaptiveSync Testing Challenges

• Allion Test Tool Solution
VESAs ClearMR Testing Challenges
Note: Dependency of VESA Program
What is VESA ClearMR (Clear Motion Ratio)?

Test purpose:

It is to ensure the quality of moving picture on display devices

Note: It does not require DP logo
10000fps is used by High Speed Camera.

Source: the above picture is from VESA
Test Concept Cont’

Test Combination.

<table>
<thead>
<tr>
<th>Luminance before a Transition</th>
<th>0%</th>
<th>25%</th>
<th>33%</th>
<th>67%</th>
<th>75%</th>
<th>100%</th>
</tr>
</thead>
<tbody>
<tr>
<td>0%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>33%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>67%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>75%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Source: the pictures here are from VESA
What can you see from a High Speed Camera.

Data Calculation
ClearMR Logo Tiers

Logo: 11 tiers

• Bigger number means better quality
• Ratio of Clear pixels to Blurry pixels

<table>
<thead>
<tr>
<th>ClearMR Tier</th>
<th>CMR Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>ClearMR 3000</td>
<td>2500 ≤ CMR &lt; 3500</td>
</tr>
<tr>
<td>ClearMR 4000</td>
<td>3500 ≤ CMR &lt; 4500</td>
</tr>
<tr>
<td>ClearMR 5000</td>
<td>4500 ≤ CMR &lt; 5500</td>
</tr>
<tr>
<td>ClearMR 6000</td>
<td>5500 ≤ CMR &lt; 6500</td>
</tr>
<tr>
<td>ClearMR 7000</td>
<td>6500 ≤ CMR &lt; 7500</td>
</tr>
<tr>
<td>ClearMR 8000</td>
<td>7500 ≤ CMR &lt; 8500</td>
</tr>
<tr>
<td>ClearMR 9000</td>
<td>8500 ≤ CMR &lt; 9500</td>
</tr>
<tr>
<td>ClearMR 10000</td>
<td>9500 ≤ CMR &lt; 10500</td>
</tr>
<tr>
<td>ClearMR 11000</td>
<td>10500 ≤ CMR &lt; 11500</td>
</tr>
<tr>
<td>ClearMR 12000</td>
<td>11500 ≤ CMR &lt; 12500</td>
</tr>
<tr>
<td>ClearMR 13000</td>
<td>12500 ≤ CMR</td>
</tr>
</tbody>
</table>
Here Comes The First Challenges

Now, you can guess What they are?

• Challenge1: How Clear is Clear according to the Log Tiers?
• Challenge2: Which Log Tier Should I target for our products?
ClearMR Performance Tier

Source: the above picture is from VESA
ClearMR Performance Tier Cont’

Source: the above picture is from VESA
Here Comes The Second Challenges

Now, you can guess What they are?

• Challenge3: Our panel suppliers do NOT know their panels’ capability against the logo tiers.

• Challenge4: What if my product fails to meet the criteria of the desired tier?

(Over driving vs CMR value, which takes some time to find a suitable OD setting.)
Suitable Products for certification

Focusing on panels

Monitor/TV

Laptop
CTS download and product listing

- CTS Download
  https://vesa.org/join-vesamemberships/member-downloads/
- Product listing
  https://www.clearmr.org/certified-products/
VESAS AdaptiveSync Testing Challenges
What is AdaptiveSync? Example: 1920x1080p60

Note: It requires DP Logo.
Adaptive-Sync Logo Tier

For Maximum Gaming Experience

AdaptiveSync Display guarantees higher refresh rates and low latency, optimized for gaming, plus a lab-certified max refresh rate so you know your display's full potential.

Minimum requirement of refresh rate: 60-144Hz

For Video Production and Playback

MediaSync Display is designed for jitter-free media playback supporting all international broadcast video formats.

Minimum requirement of refresh rate: 48-60Hz
Test Methodology

- Flicker at Fixed fps and 4 Dynamic waveforms
  - 23.976/24/25/29.97/30/47.952/48/50/59.94/60
  - Zigzag/Sine/Square/Random
Test Methodology

• Frame Drop and Frame Jitter

• G2G, Overshoot, and Undershoot
Suitable Products for certification

Focusing on Panels

Monitor/TV

Laptop
Test Issue

• The most frequently failed test items.
  - G2G (Gray to Gray)
    » 20 tests as shown on the right table

<table>
<thead>
<tr>
<th>Test case</th>
<th>Rise/Fall time(ms)</th>
<th>overshoot</th>
<th>undershoot</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-63</td>
<td>29.89</td>
<td>0.00</td>
<td>2.24%</td>
</tr>
<tr>
<td>0-127</td>
<td>3.16</td>
<td>0.00</td>
<td>5.39%</td>
</tr>
<tr>
<td>0-191</td>
<td>10.67</td>
<td>0.00</td>
<td>1.86%</td>
</tr>
<tr>
<td>0-255</td>
<td>6.40</td>
<td>0.00</td>
<td>2.73%</td>
</tr>
<tr>
<td>63-127</td>
<td>3.12</td>
<td>0.00</td>
<td>27.67%</td>
</tr>
<tr>
<td>63-191</td>
<td>3.75</td>
<td>0.00</td>
<td>7.58%</td>
</tr>
<tr>
<td>63-255</td>
<td>4.51</td>
<td>0.00</td>
<td>3.43%</td>
</tr>
<tr>
<td>127-191</td>
<td>2.18</td>
<td>0.00</td>
<td>34.13%</td>
</tr>
<tr>
<td>127-255</td>
<td>4.40</td>
<td>0.00</td>
<td>1.96%</td>
</tr>
<tr>
<td>191-255</td>
<td>3.40</td>
<td>0.00</td>
<td>2.13%</td>
</tr>
<tr>
<td>255-63</td>
<td>4.50</td>
<td>0.00</td>
<td>3.19%</td>
</tr>
<tr>
<td>255-127</td>
<td>2.97</td>
<td>0.00</td>
<td>33.02%</td>
</tr>
<tr>
<td>255-191</td>
<td>3.74</td>
<td>0.00</td>
<td>11.56%</td>
</tr>
<tr>
<td>127-63</td>
<td>2.81</td>
<td>0.00</td>
<td>31.57%</td>
</tr>
<tr>
<td>191-63</td>
<td>3.16</td>
<td>0.00</td>
<td>20.15%</td>
</tr>
<tr>
<td>191-127</td>
<td>3.59</td>
<td>0.00</td>
<td>14.76%</td>
</tr>
<tr>
<td>255-0</td>
<td>7.31</td>
<td>0.00</td>
<td>2.58%</td>
</tr>
<tr>
<td>191-0</td>
<td>7.00</td>
<td>0.00</td>
<td>1.43%</td>
</tr>
<tr>
<td>127-0</td>
<td>6.85</td>
<td>0.00</td>
<td>1.78%</td>
</tr>
<tr>
<td>63-0</td>
<td>6.91</td>
<td>0.00</td>
<td>2.65%</td>
</tr>
<tr>
<td>AVG</td>
<td>6.02</td>
<td>MAX</td>
<td>34.13%</td>
</tr>
</tbody>
</table>

Code value: 0->black, 63->Dark gray, 127-> Mid gray, 191-> Light Gray, 255->White
Test Issue Cont’

• The most frequently failed test items.
  – Flicker
    » Worst pattern
      • Square wave
  – How to Fix the failure
    » Can’t be fixed by firmware only.
    » Always replaced with an another panel

<table>
<thead>
<tr>
<th>Refresh rates</th>
<th>Flicker (dB)</th>
<th>Judge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
<td>-52.53</td>
<td>Pass</td>
</tr>
<tr>
<td>23.976</td>
<td>-52.52</td>
<td>Pass</td>
</tr>
<tr>
<td>24</td>
<td>-52.49</td>
<td>Pass</td>
</tr>
<tr>
<td>25</td>
<td>-54.57</td>
<td>Pass</td>
</tr>
<tr>
<td>29.97</td>
<td>-80.90</td>
<td>Pass</td>
</tr>
<tr>
<td>30</td>
<td>-80.86</td>
<td>Pass</td>
</tr>
<tr>
<td>47.952</td>
<td>-52.88</td>
<td>Pass</td>
</tr>
<tr>
<td>48</td>
<td>-52.49</td>
<td>Pass</td>
</tr>
<tr>
<td>50</td>
<td>-54.57</td>
<td>Pass</td>
</tr>
<tr>
<td>59.94</td>
<td>-80.55</td>
<td>Pass</td>
</tr>
<tr>
<td>60</td>
<td>-80.48</td>
<td>Pass</td>
</tr>
<tr>
<td>Type</td>
<td>Flicker (dB)</td>
<td>Judge</td>
</tr>
<tr>
<td>Zigzag</td>
<td>-62.29</td>
<td>Pass</td>
</tr>
<tr>
<td>Sine wave</td>
<td>-63.60</td>
<td>Pass</td>
</tr>
<tr>
<td>Random</td>
<td>-52.64</td>
<td>Pass</td>
</tr>
<tr>
<td>Square</td>
<td>-51.17</td>
<td>Pass</td>
</tr>
</tbody>
</table>
A monitor that uses frame buffer exists.

- Dynamic waveform (frame rate) sent out by a DP TX
- Constant waveform (frame rate) sent out by a Scaler
Test Issue Cont’

Panel

Luminance meter

AS operation is not working

AS operation is working
The Major Change in AdaptiveSync CTS 1.1 certification

G2G: Percentage(1.0,5x5) VS Delta-PQ(1.1,9x9)
The Major Change in AdaptiveSync CTS 1.1 certification Cont’

Table A-1: EOTF SMPTE ST 2084 PQ Code to Luminance Level Lookup Table (Informative)

<table>
<thead>
<tr>
<th>EOTF SMPTE ST 2084 10-bit PQ Code Value</th>
<th>Luminance Level&lt;sup&gt;a&lt;/sup&gt; (cd/m&lt;sup&gt;2&lt;/sup&gt;)</th>
<th>EOTF SMPTE ST 2084 10-bit PQ Code Value</th>
<th>Luminance Level&lt;sup&gt;a&lt;/sup&gt; (cd/m&lt;sup&gt;2&lt;/sup&gt;)</th>
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<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>450</td>
<td>49.79</td>
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<tr>
<td>8</td>
<td>0.0015</td>
<td>452</td>
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<tr>
<td>16</td>
<td>0.0054</td>
<td>515</td>
<td>95.50</td>
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<tr>
<td>24</td>
<td>0.0119</td>
<td>520</td>
<td>100.23</td>
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<tr>
<td>36</td>
<td>0.0277</td>
<td>592</td>
<td>199.15</td>
</tr>
<tr>
<td>48</td>
<td>0.0520</td>
<td>616</td>
<td>249.03</td>
</tr>
<tr>
<td>56</td>
<td>0.0738</td>
<td>636</td>
<td>249.03</td>
</tr>
<tr>
<td>64</td>
<td>0.101</td>
<td>668</td>
<td>401.51</td>
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<tr>
<td>120</td>
<td>0.498</td>
<td>692</td>
<td>499.33</td>
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<tr>
<td>153</td>
<td>0.992</td>
<td>712</td>
<td>598.33</td>
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<td>156</td>
<td>1.051</td>
<td>728</td>
<td>691.16</td>
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<td>193</td>
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<td>206</td>
<td>2.483</td>
<td>769</td>
<td>998.93</td>
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<tr>
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<td>807</td>
<td>1404</td>
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<td>254</td>
<td>5.031</td>
<td>846</td>
<td>2000</td>
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<tr>
<td>256</td>
<td>5.172</td>
<td>884</td>
<td>2803</td>
</tr>
<tr>
<td>307</td>
<td>10.05</td>
<td>892</td>
<td>3013</td>
</tr>
<tr>
<td>340</td>
<td>14.96</td>
<td>924</td>
<td>4024</td>
</tr>
<tr>
<td>384</td>
<td>24.70</td>
<td>1023</td>
<td>10000</td>
</tr>
</tbody>
</table>

PQ relationship with Luminance
CTS download and product listing

- **CTS Download**
  https://vesa.org/join-vesamemberships/member-downloads/
- **Product listing**
  https://www.adaptivesync.org/certified-products/
Allion Test Tool solution
Test Tools & Fixtures

Customizable Fixtures for Efficient Validation

Allion has developed a wide range of exclusive tests and prides itself on top-quality test fixtures. Our fixtures have been approved by leading international associations and can be tailored to different standards and specifications. With over 100 projects in high-frequency and other fixture designs, we offer customizable solutions that enhance the efficiency and cost-effectiveness of your product validation process.

- **PCI Express**
- **USB**
  - M.2 PCIe CLB5.0 Test Fixture
  - USB-C® – Short Channel Rx Pre***
  - USB-C® Plug TX/RX
- **HDMI / DP**
  - USB-C® Plug
  - DP1.4 AUX Channel
  - HDMI SCDC/EDID Controller
- **Cable Connector**
  - HDMI SCDC/EDID Controller
  - USB4 Passive Cable
  - USB4 Golden Plug
- **Auto Switch**
  - USB-C® – 3.2 1 by 4 Auto Switch
  - USB-C® – 3.2 1 by 2 Auto Switch
  - USB-A 3.1 1 by 4 Auto Switch
  - Conductive Drum
USB Test Fixtures

USB-A 2.0 HSSQ TF Sets

USB-A HS Device SQ Fixture (AUT20132)
- High-Speed Device Signal Quality Test (EL_2, 4, 5, 6, and 7)
- Eye Pattern Test
  Brandnew design AUT20132 for USB-A Host in 2020, which reduce the risk of the SMA damage (easy to change the SMA Connect), improve the quality of the USB 2.0 Signals, redesign the jumper to be a switch, Self Power connector changed to USB Type-C®

USB-A HS Host SQ Fixture (AUT20038)
- High-Speed Host Quality Test (EL_2, 3, 6, and 7)
- Eye Pattern Test
  Allion design a brandnew Product AUT20038 in 2020, which reduce the risk of the SMA damage (easy to change the SMA Connect), improve the quality of the USB 2.0 Signals

USB-C® 3.2 Electrical TF Sets

USB TX/RX Pocet TF (AUT20044)
- Application
  USB-C® 3.1 Tx Signals Integrity Test
  AUT20044 is a substitute for Host 1C & Device 1C in USB31CET Kits. In order to perform the integrity test, you must have the rest of UAB31CET Kits test fixtures.
- Key Features
  - Up to 4GHz Design for Next Gen Combine UFP/DFP testing in one Fixture
  - Better Signals quality than original Test Fixture

USB 3.1 Type-C® TX/RX Breakout TF (AUT20098)
- Application
  USB-C® 3.1 Tx/Rx Signals Integrity Test
  AUT20098 is a substitute for Full Type-C® Breakout in USB31CET Kits. In order to perform the integrity test, you must have the rest of UAB31CET Kits test fixtures.
- Key Features
  - Good Signal Quality compare with original Design
  - Slide switch for CC1/CC2 & Rp/Rd Setting
  - Type-C Connector for Delivery +5V Power instead of DC Jack

USB 5Gbps Electrical Testing

Host Measurement (AUT20135)
- Key Features
  - Up to USB 5 Gbps Data Transfer
  - Standard A Plug Test Fixture
  - Downstream Facing Port Tx/ Rx Long Channel Tests

Host Short Channel (AUT22106)
- Key Features
  - Up to USB 5 Gbps Data Transfer
  - Standard A Plug Test Fixture
  - Downstream Facing Port Rx Short Channel Test

Host Loss/Calibration (AUT2032)
- Key Features
  - Up to USB 5 Gbps Data Transfer
  - Standard B Receptacle 5* Host Test Fixture/ Device Calibration Fixture
  - Upstream Facing Port Calibration
  - Downstream Facing Port Rx Long Channel Test

Device Measurement (AUT21003)
- Key Features
  - Up to USB 5 Gbps Data Transfer
  - Standard A Receptacle Test Fixture
  - Upstream Facing Port Rx Short Channel Test

Device Short Channel (AUT22109)
- Key Features
  - Up to USB 5 Gbps Data Transfer
  - Standard A Receptacle Test Fixture
  - Upstream Facing Port Rx Long Channel Test

Device Loss (AUT22033)
- Key Features
  - Up to USB 5 Gbps Data Transfer
  - Standard A Receptacle Test Fixture
  - Upstream Facing Port Rx Long Channel Test
USB Test Fixtures

USB-C® 2.0 Host/Device HSSQ TF

- **Application**
  - **Host**
    - Packet Parameters (EL_21, EL_25, EL_23, EL_22, EL_55)
    - Chirp Timing (EL_33, EL_34, EL_35)
    - Suspend/Resume Timing (EL_39, EL_41)
  - **Device**
    - High-Speed Signal Quality Test (EL_2, EL_4, EL_6, EL_7)
    - Packet Parameters (EL_21, EL_22, EL_25)
    - Chirp Timing (EL_28, EL_29, EL_31)
    - Suspend/Resume Timing (EL_38, EL_39, EL_40, EL_27, EL_28)
    - Test J1K, SEQ_NAK (EL_9)

- **Key Features**
  - Combine UFP/DFP testing in one Fixture
  - Better Signals quality than original Test Fixture

USB Type-C® 2.0 Device HSSQ TF (AUT17037)

---

USB-C® 40Gbps TF

- **Key Features**
  - Up to USB 40Gbps Data Transfer
  - 5V Input from both USB-C® Connectors
  - USB4® Thunderbolt™4 Rx Test

USB-C® Plug & Receptacle RX TF (AUT20159)

- **Key Features**
  - Up to USB 40Gbps Data Transfer
  - 5V Input from both USB-C® Connectors
  - USB4® Thunderbolt™4 Tx Test

USB-C® Receptacle TX/RX TF (AUT21112)

- **Key Features**
  - Up to USB 40Gbps Data Transfer
  - 5V Input from both USB-C® Connectors
  - USB4® Thunderbolt™4 Tx/Rx Tests

---

USB 40Gbps Electrical Testing

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HDMI & DisplayPort Test Fixtures

**HDMI Type-A Test Fixture**
- **Application**
  - HDMI CTS 1.4b Compliance Electrical Testing
  - HDMI Directly Attach Device Electrical Compliance Testing
- **Features**
  - No twisted wire, reducing signal loss
  - Compatible with Electrical test for TX & RX devices
  - Compatible with Electrical test for Cable & Directly Attach device

- **HDMI Type-A Test Fixture**
  - **Application**
    - HDMI HEAC device Electrical Compliance Testing
    - HDMI Cable Cat.1&2 Electrical Compliance testing
  - **Features**
    - No twisted wire, reducing signal loss

- **HDMI Type A High Frequency Test Fixture**
  - **Application**
    - HDMI 2.1 Compliance Electrical Testing
    - HDMI 1.4b Compliance Electrical Testing
  - **Features**
    - Short and strong cable reducing signal loss
    - Reduced Human factors
    - **Up to 48Gb/s data rate supported**
    - Wire Modularization, easy Setup
    - Supports FRL testing
    - Calibration Board for De-embedding

**DisplayPort Test Fixture**
- **Application**
  - VESA DisplayPort v1.4a PHY Layer Common Tests
  - AUX_CH (Manchester-II) EYE Test
  - AUX_CH_mip Termination DC Test
  - AUX_CH slew rate test
  - DP_PWR DC Level Test / DP_PWR Current Test
- **Features**
  - Measure AD and DC voltage
  - Measure DP_PWR voltage
  - No twisted wire, reducing signal loss

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PCle Gen5 Test Fixtures

**M.2 CLB5.0 Test Fixtures**
- **Key Features**
  - **Worldwide First** PCIe Gen5 M.2 Test Fixture
  - Durable SMPM Connectors, supporting up to 40GHz
  - Flexible Cable Assembly to simplify installation & exchange
  - One for M.2 Lane0/Lane1, the other for M.2 Lane2/Lane3
  - 2X Thru Calibration Board

**U.2/U.3 CLB5.0 Test Fixture**
- **Key Features**
  - **Worldwide First** PCIe Gen5 U.2/U.3 Test Fixture
  - Durable SMPM Connectors, supporting up to 40GHz
  - Flexible Cable Assembly to simplify installation & exchange
  - General support U.2/U.3 PCIe & SAS in one Board
  - 2X Thru Calibration Board

**OCP NIC3.0 CLB5.0 Test Fixtures**
- **Key Features**
  - Durable SMPM Connectors, supporting up to 40GHz
  - Flexible Cable Assembly to simplify installation & exchange
  - One for Lanes L0/12/3 & L8/9/10/11, the other for Lanes 4/5/6/7 & L12/13/14/15
  - 2X Calibration Board

**CEM CLB5.0 Test Fixtures**
- **Key Features**
  - Durable SMPM Connectors, supporting up to 40GHz
  - Flexible Cable Assembly to simplify installation & exchange
  - One for L0/L1/L2/L3, the other for L11/L12/L13/L14
  - 2X Thru Calibration Board
  - Ready for Allion Automation

**E1/E3 CLB5.0 Test Fixtures**
- **Key Features**
  - Durable SMPM Connectors, supporting up to 40GHz
  - Flexible Cable Assembly to simplify installation & exchange
  - One for E1 Lanes 0/1/2/3, the other for E3 Lanes 4/5/6/7
  - 2X Calibration Board
PCIe Gen5 Test Fixtures

### M.2 CBB5.0 Test Fixture
- **Key Features**
  - Up to 40GHz Design for Next Gen.
  - *Worldwide First* PCIe M.2 Test Fixture
  - Power Source from USB-C Port
  - Adjustable Voltage for 3.3V

### U.2/U.3 CBB5.0 Test Fixture
- **Key Features**
  - Up to 40GHz Design for Next Gen
  - 12V Power Source from AC/DC Adaptor or ATX Power Connector

### CEM CBB5.0 Test Fixture
- **Key Features**
  - Up to 40GHz Design for Next Gen
  - Power Source from ATX Power Connector

### OCP NIC3.0 CBB5.0 Test Fixture
- **Key Features**
  - Up to 40GHz Design for Next Gen
  - Backward Compatible for E1/E3
  - Power Source from ATX Power Connector

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AI/ Automation Solutions:
Allion PCIe Automation Measurement System (APMS)

- Control Switch Box to switch lanes automatically
- Control CMTS to toggle test patterns automatically
- Control instrument to load setup file and acquire/save wave automatically
- Flexible configuration selection for Spec. Generation, Lane No. and Preset mode
- One quick button to test all configuration (All generation, all 8 lanes with all preset)
- Conversion SW can be executed simultaneously or independently
- Conversion SW can be executed with human unattended
AI/ Automation Solutions: Cable-Connector Allion Multiport Switch (CAMS)

CAMS can help RD members verify the high-frequency cable and connector design. At the same time to accomplish 100% measured high-frequency cables in the production line.
Q&A
Allion is the premier resource for all of your third party testing needs. Our services bring products to market more quickly, reliably, and cost effectively to protect your brand quality and that of your suppliers.

Thank you

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VESPA PlugTest Events

• Provide significant value to member companies, particularly as new capabilities and products are deployed.
• Demonstrate and improve Traditional Interoperability
• Test Native DP and DP Alt Mode over USB Type-C products
  • UHBR20/13.5/10, DSC, FEC and other new capabilities
  • Verify Test Equipment Correlation (DP 2.1 LL CTS and PHY CTS)
• VESA hosted two successful PlugTests in 2022 (Taiwan and US)
• VESA will host two PlugTests in 2023
  • Taipei, Taiwan: October 2023 (Next week)
  • Burlingame, CA: May 2023 (done)
## Product certifications 2022/2023

<table>
<thead>
<tr>
<th>Products</th>
<th>2022</th>
<th>2023</th>
</tr>
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<td>DP Sources</td>
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<td>DP Sinks</td>
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<td>DP Cables</td>
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<td>DisplayHDR</td>
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<td>ClearMR</td>
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<tr>
<td>AdaptiveSync</td>
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Summary
Summary

• Product shipments and certifications on DP 2.1 based products continue to grow

• DisplayPort over USB-C is now the defacto standard for laptops, tablets and handheld devices

• DP 2.1 Link Layer CTS is major update and improvement of testing coverage for new capabilities introduced in DP v2.1 specification

• Momentum continues to grow for DisplayHDR, ClearMR and VESA AdaptiveSync product certification

• Development and adoption of new technologies continues to drive increases in VESA membership growth
Questions?
Demos
quantumdata M42de
Video Analyzer/Generator

- Protocol Analysis and Video Generator for DisplayPort 2.1 source & sink testing
- Supports DP80, DP40 and USB-C (Alt Mode) compatible devices
- Full support for DP 2.1 10Gb/s, 13.5Gb/s & 20Gb/s lane rates
M21 DisplayPort Capabilities.
- DisplayPort Analyzer (Rx) only.
- Full sized DP up to 10G/lane.
- USB-C DP up to 13.5G/lane.
- Aux Channel monitoring with ACA including passive monitoring between source and sink devices.
Voyager M4x: USB4 Protocol Analyzer

- **Complete Solution**
  - Analyzer, Exerciser, & Compliance Tester

- **Accurate Capture at 40Gb/s**
  - T.A.P.4™ front-end captures link training without distorting equalization process

- **Comprehensive Decoding**
  - View Tunneled PCIe, DisplayPort™, & USB Protocols
T3RapidWave4000: Advanced modular and automated cable tester

Production Configuration

- Continuity
- DC Resistance
- DC Resistance Pins
- EMarker read
- SVID Protocol
- Quiescent Current
- Insertion Loss

✓ PRODUCTION MODULE
  wiring and resistance measurements

✓ >13 K$ +pay-per-test
✓ High Volume Factory Production

Failure Analysis and Signal Integrity testing

- Eye diagram
- Insertion loss
- Cross-talk
- Impedance profile
- Inter-pair skew
- Intra-pair skew

✓ ADVANCED SIGNAL INTEGRITY MODULE
  accurate and rapid signal integrity measurements

✓ > 43 K$ (unlimited testing)
✓ Factory QC labs, Compliance Lab, Standard Organization, OEM Brand
WaveMaster 8000HD Oscilloscope

- **PHY Compliance Testing**
  - 12 Bits all the time; Best in Class Jitter and Eye Measurements
  - 'Unified' Test Fixture Approach for DP2.1 and USB4 Version 2.0
  - Source and Sink (Anritsu MP1900A) PHY Compliance Testing using QualiPHY Software

- **Serial Data Analysis**
  - Built-In SDA Expert DisplayPort PHY CTS Measurements

- **Unique Cross Layer Analysis**
  - DP-AUX Sideband Trigger and Decode
  - CrossSync® PHY for DisplayPort Tunneling using M4X
Allion Demo Booth

Customizable Fixtures for Efficient Electrical Signal Validation

PCI Express 5.0
- M.2 PCIe CLB5.0 Test Fixture
- U.2/U.3 PCIe CLB5.0 Test Fixture

USB 4 and below
- USB-C® – Short Channel Rx
- USB-C® Plug TX/RX
- USB A High Speed Signal Quality Test Fixture Set

DP 2.1 and below
- DP2.1 AUX Channel

More test fixtures on the demo booth
Cybertek VESA DSC Decoder IP Core Demo

DSC Decoder IP Core Feature
- Compliant with VESA DSC 1.2a and 1.2b standards
- Support MMAP, BP, MPP and ICH encoding mechanisms
- YCbCr and RGB video input format
- 4:4:4, 4:2:2, and 4:2:0 native coding
- Support 8/10/12 bits per component
- Support 3 pixels per clock decoding
- Configurable features for gate count and speed
DisplayPort Protocol Analyzer
In Action!

- Connects between ANY Source and ANY Sink
  - Supports 8b/10b, eDP, FEC/DSC, DP1.2b, DP 1.4b, DP 2.1
  - Supports 128b/132b DP 2.1
  - Probe, Decode, and Time Correlate High Speed Main Link and Aux Channel
  - Snooper and Repeater Probing Solutions Available

See our Rep in Taiwan
GRL
DisplayPort 2.1
Solution
A quick and straightforward way to test and debug your DisplayPort 2.1 transmitter products efficiently (GRL-DP21-TX)

**Overview**

- Provides full compliance automation to the DisplayPort 2.1 standard.
- Compatible with Tektronix and Keysight oscilloscopes.
- Flexible selection on test items and data rates (UHBR10, UHBR13.5, and UHBR20).
- DP 2.1 according to current CTS.
- Support AUX Controller automation.
Overview

- Provides full compliance automation to test Sink products to the DisplayPort 2.1 standards
- Automatically calibrates BERT and Scope to create stressed eye for Sink Jitter Tolerance testing
- Compatible with Tektronix and Keysight oscilloscopes paired with the Anritsu MP1900A BERT
- Fully integrated with high-speed test fixtures and AUX controller available from Wilder Technologies (sold separately)
Measurement Disaggregation

Keysight Technologies
Challenge: Test Run Time Optimization

Solution: Measurement Disaggregation

What is it costing you?
- Extensive test plan requires long test time
- 75% of test time is spent processing data

What is an ideal solution?
- Significant test time improvement using Measurement Disaggregation
- Re-use of your invested solution
  - Saves $$$
  - Builds on your present equipment and knowledge
Tektronix DisplayPort Tx Compliance Testing Solution

Automated compliance

Fully automated compliance solution
Supports all data rates till UHBR20

Debugging

Advanced Debugging capability

DisplayPort Test Setup

Compliance Test Points

Supports both TP2 & TP3EQ(CTLE) test points
USB4 cable model are used in the TP3EQ tests

Signal Validation

Pattern validation

Pre Recorded

Offline Mode Cross Geo collaboration

DUT control

Automation with UCD 323 and DPR100

Signal acquisition

Use P76XX series probe with compatible probe tips in absence of fixtures.
**UCD-500 Gen2**
16K DP 2.1 Generator & Analyzer

- DP 2.1 Sinks and Sources up to 10K@60Hz (16K@60Hz with DSC up to UHBR 20 Bit Rate)
- Supports DP and USB-C connectors
  - UHBR 20 Gb max link rate for DP and USB-C connectors
- Adaptive-Sync, DSC, FEC and LTTPR support
- DP 1.4a Link Layer CTS Tool
- DP 2.1 Link Layer CTS Tool including
  - LTTPR CTS
  - DisplayID/EDID CTS
  - Adaptive-Sync CTS
- HDCP 2.3 Compliance Test Device for Transmitters, Receivers and Repeaters
- Color depth 6 to 16bpc
- Capture memory 16GB

---

**USB Explorer™ 350**
Multi-function USB Type-C®, USB 3.2 x1, and Power Delivery Protocol Test Platform

- Broad Specifications Support: USB 2.0 (1.5, 12, 480 Mbps), USB 3.2 x1 Gen 1 (5 Gbps) and Gen 2 (10 Gbps), USB Power Delivery 3.1 and USB Type-C 1.3
- Multi-function: Same unit can operate as protocol analyzer, host/device/sink/source emulator, as well as compliance tester
- Perfect Accuracy: High precision clocking components coupled to Ellisys’ protocol analysis engine provides industry’s unmatched accuracy
- Unequaled Software: Ellisys powerful yet easy to use multi-protocol analysis software offers the most complete feature set in the industry, including essential features such as Instant Timing for precise timing analysis and Instant Throughput for performance characterization
- Integrated Logic Analysis: Logic signals analysis concurrently to traffic capture opens a new debugging dimension to development engineers by visualizing outputs of their FPGA or ASIC