Welcome
VESA Workshop Seoul Korea 2024

VESA Workshop Agenda

Time	Topic	Speaker
10:00am – 10:20am	VESA Overview and Standards Updates, Including DisplayPort v 2.1a and Display Panel Standards	Jim Choate, Compliance Program Manager
10:20am – 11:00am	DisplayPort Link Layer CTS v 2.1	Sergey Grushin, CTO, Unigraf
11:00am – 11:20am	eDP and DP v 2.1 PHY CTS Overview and Updates	Jim Choate, Compliance Program Manager
11:30am – 12:00pm	DP Alt Mode v 2.1a Overview and CTS Updates	Tim Wei, Senior Application Engineer, Ellisys
12:00pm – 1:00pm	Lunch	
1:00pm – 1:45pm	VESA DisplayHDR Specification & AdaptiveSync Overview and Test + Demo	Do Kyun Kim, Professional Engineer, and Seung Hyun Yoo, Senior Research Engineer, LGE
1:45pm – 2:15pm	ClearMR Specifications and Compliance Testing Overview	Dr. Yongwoo Yi, Principal Engineer, Samsung Display
2:15pm – 2:30pm	Break	
2:30pm – 4:00pm	VESA Compliance Program	Jim Choate, Compliance Program Manager
	Summary, Questions & Answers	
4::00pm – 4:15pm	Demo Stations Overview	

VESA Overview and Standards Updates

Jim Choate
VESA Compliance Program Manager
10/07/2024

Agenda

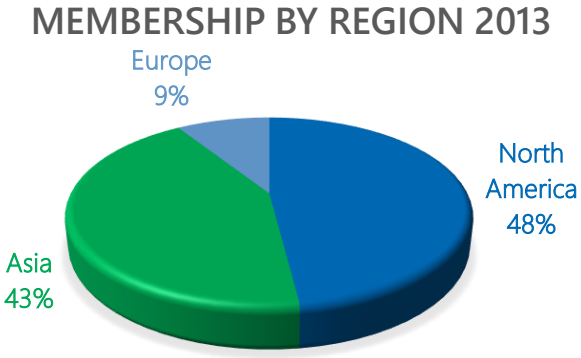
- VESA Overview
- DisplayPort Overview
- VESA Certified DisplayHDR, ClearMR and Adaptive-Sync
- VESA Technology Development Areas
- Summary

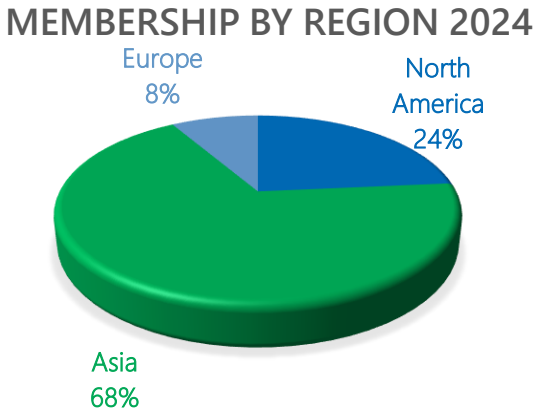
VESA OVERVIEW

About VESA

- A growing global industry alliance with nearly 340 members in 2024. Strong growth in membership over 10 years.
- Mission to develop, promote and support ecosystem of vendors and certified interoperable products for the electronics industry.
- *Develops OPEN standards, contribution is open to all companies at all stages of development*

VESA Membership Growth





Changes from 2013:
Asia + 25%

VESA Standards Enable Many Market Segments…

Monitors, PCs and laptops

Gaming consoles and headsets

Digital signage / kiosks

Smartphones and tablets

Automotive

Digital projectors

...As Well as Many Aspects of Display Technology

Display Interfaces

- DisplayPort
- Embedded DisplayPort
- DisplayPort Alt Mode (Native DisplayPort over USB-C connector)
- DisplayPort Tunneling (USB4 and Thunderbolt)
- Automotive Extensions Services (DP AE specification)

Display Data Compression

- Display Stream Compression (DSC)
- VESA Display Codec for Mobile (VDC-M)

Display Metrology

- Standardized Display Performance Measurement
- DisplayHDR Certification (High Dynamic Range)
- ClearMR Certification
- AdaptiveSync Display Certification

Display Capability Parameters

- DisplayID
- Extended Display Identification Data (EDID)
- Multi-Display Interface (MST)

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VESA Local Asian Support Capability

- VESA continues to provide local support to Asia to address growing regional membership needs
- China (Mainland) and Taiwan are the fastest growing areas for VESA's membership.
- **Kellen** is VESA's Representative in Asia
- This partnership provide members with a communication option in their native language. Kellen handles membership related activities including, new membership requests, renewals, event support and translation of VESA member messaging, etc.
- AsiaVESA@kellencompany.com or at +86 10 6580 0670

DisplayPort ™ Overview

DisplayPort Market Penetration

- DisplayPort adoption continues to grow in 2024
- DisplayPort and DisplayPort Alternate Mode over USB-C
  - The common monitor interface for personal computers
  - Supported on the USB-C interfaces
  - Mandated for USB4 and Thunderbolt
  - Automotive integration with DP AE specification
  - Mobile phones with USB-C
- Embedded DisplayPort (eDP)
  - ~95% penetration in notebook PCs, used in many high-end tablets and now automotive

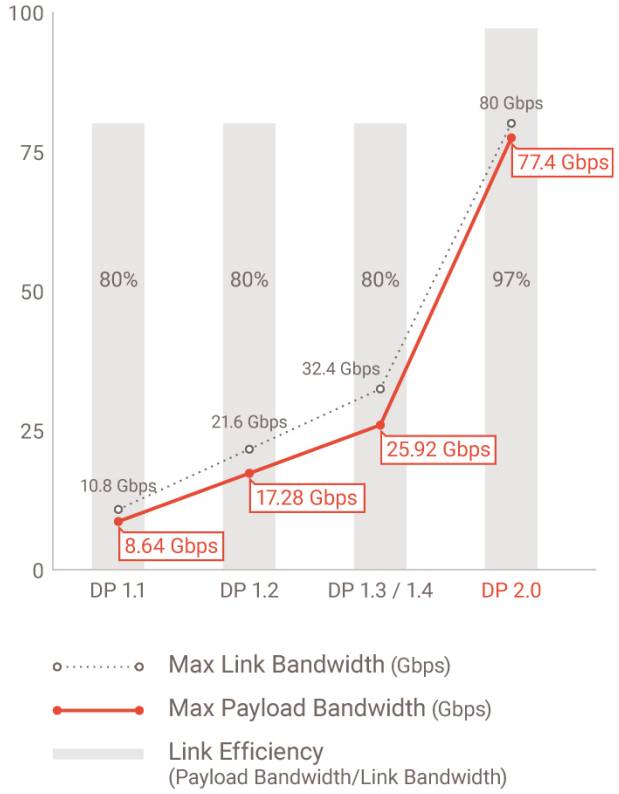
DisplayPort 2.1a Summary

- DisplayPort v2.1a was released in December 2023
- Major features added in **v2.0/v2.1/v2.1a**:
  - Added 128b/132b DP channel coding
  - Increase in data bandwidth performance (almost 3X) with new link rates up to 20 Gbps/lane
  - Panel Replay, similar to PSR (Panel Self Refresh) used for eDP
  - DSC support mandated
  - Enhanced DP connectors and cables (DP40 and DP80)
  - DP PHY specification alignment with USB4 PHY specification
  - Updated DP to HDMI v2.1 or higher protocol converter (PCON)
  - Corrects errata
  - Replaces DP40 cables with DP54 to expand higher rate cable length
  - Expanded Tunneling capability
  - Updates for DP AE Services specification

- DisplayPort **2.1a** enables up to 3X increase in video bandwidth performance vs DP **1.4**
- 3 new data rates added. UHBR10, UHBR13.5 and UHBR20 provides up to 80Gbps link bandwidth for 4 lanes at 20Gbps.
- First standard to support 8K resolution (7680 x 4320) at 60 Hz refresh rate with full-color 4:4:4 resolution, including with 30 bits per pixel (bpp) for HDR-10 support
- Beyond 8K resolutions achieved with maximum link rate to up to 20 Gbps/lane and more efficient 128b/132b channel coding

DisplayPort™

EVOLUTION OF DISPLAYPORT DATA BANDWIDTH



DisplayPort 2.1a Resolution Capability
(Single Display Examples)

Port Configuration	DisplayPort 1.4a	DisplayPort 2.1a
No Compression		
4 Lanes, max link rate	5K (5120x2800)@60fps 24bpp	10K (10240x4320)@60fps 24bpp
2 Lanes, max link rate	4K (3840x2160)@60fps 24bpp	8K (7680x4320)@30fps 30bpp
With Compression (DSC)		
4 Lanes, max link rate	8K (7680x4320)@60fps 30bpp	16K (15360x8460)@60fps 30bpp
2 Lanes, max link rate	5K (5120x2800)@60fps 24bpp	10K (10240x4320)@72fps 30bpp

Notes:

- 2 Lane configuration is common for USB-C DP Alt Mode
- All above modes assume full 4:4:4 color encoding
- 30bpp is required for DisplayHDR operation

Key:

- DSC = Display Stream Compression
- fps = frames per second
- bpp = bits per pixel

VESA Certified DisplayHDR, ClearMR and AdaptiveSync

VESA Display Performance Standards

VESA's display performance work group has been busy since the initial release of the DisplayHDR CTS in 2017.

- VESA Certified DisplayHDR r1.2 - *update covered by LGE*
- VESA Certified AdaptiveSync r1.1 - *update covered by LGE*
- VESA Certified Clear Motion Ratio (CMR) r1.1 – *update covered by Samsung Display*

DisplayHDR Summary

- Industry's first open HDR specification for LCD and emissive (OLED/microLED) displays with a fully transparent testing methodology
- More than 3000 display models certified under logo program to date makes VESA Certified DisplayHDR one of the most successful logo programs in VESA history.
- More details available at https://displayhdr.org

VESA Defines New Standard to Help Speed PC Industry Adoption of High Dynamic Range Technology in Laptop and Desktop Monitor Displays

DisplayHDR is industry's first open HDR specification with a fully transparent testing methodology

SAN JOSE, Calif. – December 11, 2017 – The Video Electronics Standards Association (VESA®) today announced it has defined the display industry's first fully open standard specifying high dynamic range (HDR) quality, including luminance, color gamut, bit depth and rise time, through the release of a test specification. The new VESA High-Performance Monitor and Display Compliance Test Specification (DisplayHDR) initially addresses the needs of laptop displays ar

ClearMR Summary

- VESA developed motion blur performance compliance test specification for LCD and emissive (OLED/microLED) displays with a new Clear Motion Ratio (CMR) metric and fully transparent testing methodology
- More than 116 display models certified under ClearMR logo program to date
- More details available at https://www.clearmr.org/

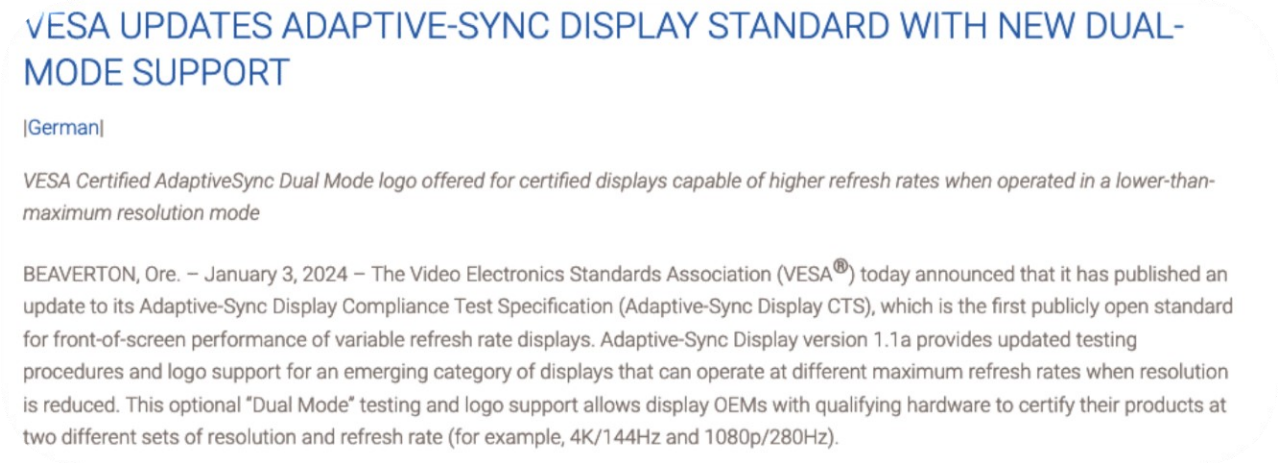
VESA BRINGS CLARITY TO MOTION BLUR IN DIGITAL DISPLAYS WITH NEW COMPLIANCE TEST SPECIFICATION AND LOGO PROGRAM

ClearMR specification and logo program provide consumers with a true quality metric for grading motion blur performance for LCD and OLED panels, TVs, desktop monitors and embedded displays

BEAVERTON, Ore. – August 22, 2022 – The Video Electronics Standards Association (VESA®) today introduced the ClearMR Compliance Test Specification (ClearMR), an industry standard and logo program that provides a new quality metric for grading motion blur in digital displays. ClearMR is applicable to both LCD and emissive display products, including display panels, TVs, monitors, and computers with embedded displays, such as all-in-ones, laptops, notebooks and tablets. The new metric Clear Motion Ratio (CMR), as

VESA Adaptive-Sync Display Summary

- Industry's first publicly open standard for front-of-screen performance of variable refresh rate displays.
- More details available at https://www.adaptivesync.org/



VESA UPDATES ADAPTIVE-SYNC DISPLAY STANDARD WITH NEW DUAL-MODE SUPPORT

|German|

VESA Certified AdaptiveSync Dual Mode logo offered for certified displays capable of higher refresh rates when operated in a lower-than-maximum resolution mode

BEAVERTON, Ore. – January 3, 2024 – The Video Electronics Standards Association (VESA®) today announced that it has published an update to its Adaptive-Sync Display Compliance Test Specification (Adaptive-Sync Display CTS), which is the first publicly open standard for front-of-screen performance of variable refresh rate displays. Adaptive-Sync Display version 1.1a provides updated testing procedures and logo support for an emerging category of displays that can operate at different maximum refresh rates when resolution is reduced. This optional "Dual Mode" testing and logo support allows display OEMs with qualifying hardware to certify their products at two different sets of resolution and refresh rate (for example, 4K/144Hz and 1080p/280Hz).

DP 2.1 Link Layer CTS Update

Sergey Grushin
Unigraf
7.10.2024

DP 2.1 Link Layer Compliance Testing Update

Agenda

- Native DisplayID
- Audio
- USB4 DP Tunneling
- Updates after rev.1.0
- Planned updates

Native DisplayID Tests (Adopted in March 2024)

- Source DUT
  - Section 4.7.6 Native DisplayID Video Tests
  - Section 4.7.7 Native DisplayID Audio Tests
- Sink DUT
  - Section 5.7.19 Native DisplayID Framework Validation Tests
  - Section 5.7.20 Product Identification Data Block Tests
  - Section 5.7.21 Display Parameters Data Block
  - Section 5.7.22 Display Interface Data Block

Audio CTS (TGR)

- Main Targets:
  - Validate Audio at UHBR link rates
  - Validate Audio with DSC enabled
- Challenges:
  1. Streaming high sample rate audio at RB timings
  2. Audio test time
  3. Audio samples distribution during blanking period
- Draft 4 is under TGR (Task Group Review)

Audio CTS (Challenge #1 – 192Khz 8ch)

						SSC	TRUE	0,994					
				(Hz)	(MHz)	FEC	TRUE	0,97			SST		
Hactive	Vactive	Htotal	Hblank	V Freq	Pixel Freq	lane	link_rate	symbol size	2ch, SST AudioSymbolCntReqPerHBlank	8ch, SST AudioSymbolCntReqPerHBlank	StrmSymbolCntAvailPerHBlank	2ch, isValid	8ch, isValid
1920	1080	2000	80	30	65,76	1	162	8	65	254	165	TRUE	FALSE
1920	1080	2000	80	60	133,32	1	162	8	44	127	66	TRUE	FALSE
1920	1080	2000	80	144	333,216	4	162	8	24	88	92	TRUE	TRUE
1920	1080	2000	80	144	333,216	2	270	8	22	86	92	TRUE	TRUE
1920	1080	2000	80	144	333,216	1	540	8	22	85	98	TRUE	TRUE
3840	2160	3920	80	30	257,661	4	162	8	48	128	136	TRUE	TRUE
3840	2160	3920	80	30	257,661	2	270	8	44	128	130	TRUE	TRUE
3840	2160	3920	80	30	257,661	1	540	8	44	127	136	TRUE	TRUE
3840	2160	3920	80	60	522,614	4	162	8	24	88	36	TRUE	FALSE
3840	2160	3920	80	60	522,614	2	540	8	22	86	128	TRUE	TRUE
3840	2160	3920	80	60	522,614	1	810	8	22	85	93	TRUE	TRUE
3840	2160	3920	80	144	1306,206	4	540	8	24	44	68	TRUE	TRUE
3840	2160	3920	80	144	1306,206	2	810	8	22	44	62	TRUE	TRUE
5120	2160	5200	80	30	341,796	4	162	8	48	128	88	TRUE	FALSE
5120	2160	5200	80	30	341,796	2	270	8	44	128	88	TRUE	FALSE
5120	2160	5200	80	30	341,796	1	540	8	44	127	95	TRUE	FALSE
5120	2160	5200	80	60	693,264	4	270	8	24	88	60	TRUE	FALSE
5120	2160	5200	80	60	693,264	2	540	8	22	86	86	TRUE	FALSE
5120	2160	5200	80	60	693,264	1	810	8	22	85	62	TRUE	FALSE
5120	2160	5200	80	120	1427,088	4	540	8	24	44	60	TRUE	TRUE
5120	2160	5200	80	144	1732,723	4	540	8	24	44	36	TRUE	FALSE
7680	4320	7760	80	30	1019,896	4	540	8	24	88	108	TRUE	TRUE
7680	4320	7760	80	30	1019,896	2	810	8	22	86	90	TRUE	TRUE
7680	4320	7760	80	60	2068,66	4	810	8	24	44	64	TRUE	TRUE
10240	4320	10320	80	30	1356,357	4	540	8	24	88	64	TRUE	FALSE
10240	4320	10320	80	30	1356,357	2	810	8	22	86	58	TRUE	FALSE
10240	4320	10320	80	60	2751,105	4	810	8	24	44	32	TRUE	FALSE

Audio tests (Challenge #2 – Test Time)

- Source DUT
  - No Sources supporting DP Test Automation for Audio.
  - Around 2h to execute Audio tests for Source devices at non-UHBR link rates. (test 4.4.4.5 requires around 30 minutes of test operator time).
- Sink DUT
  - Listening check is required when test Sink devices.
  - Around 2h to execute Audio tests for Sink devices at non-UHBR link rates.
- Extending test procedures to cover UHBR link rates and DSC configurations estimated to double test time.

Audio CTS (Challenge #3)

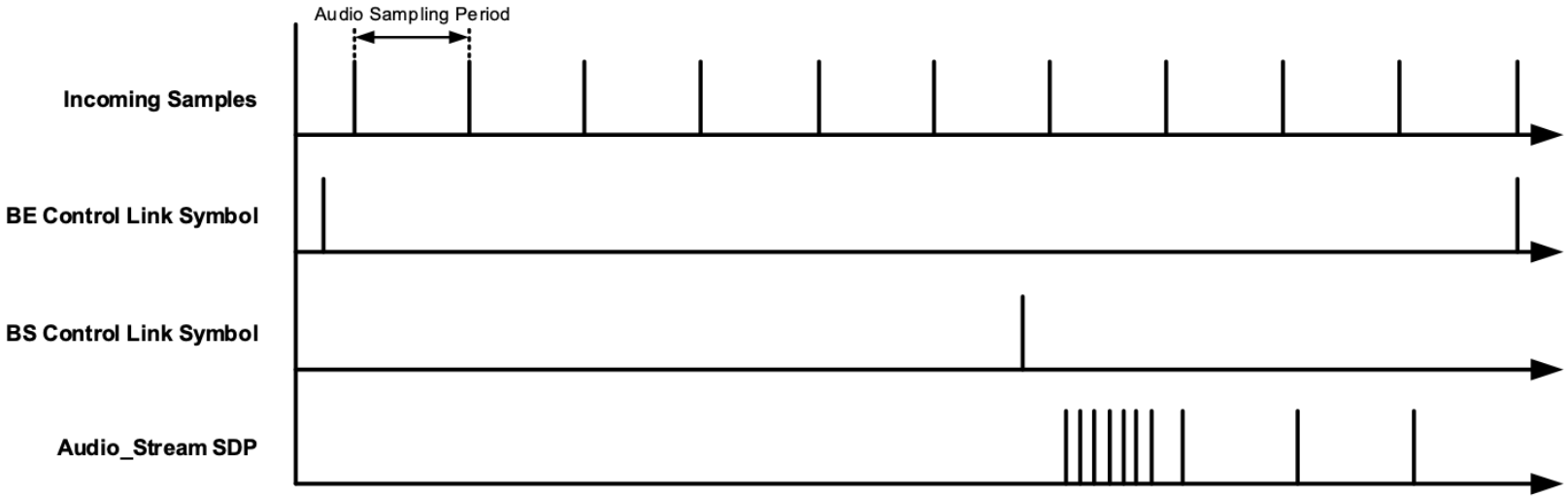


Figure A-2: Audio_Stream SDPs Transfer with Video during Video VActive Period

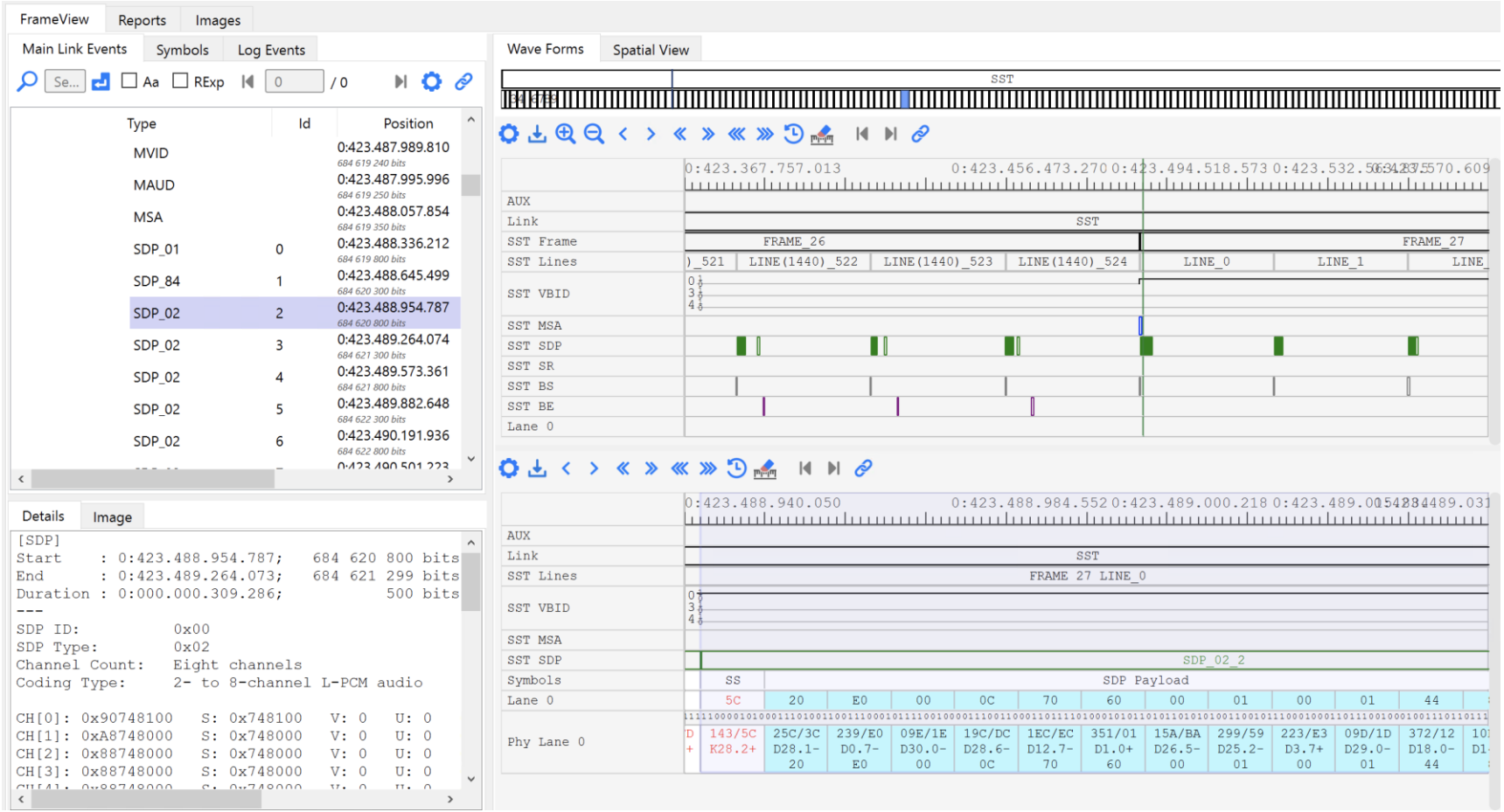
Audio CTS (Challenge #3) continued

$$floor(\frac{nF_s H_{total}}{F_p}) - 4 \le S_{tx} \le floor(\frac{nF_s H_{total}}{F_p}) + 4$$

where:

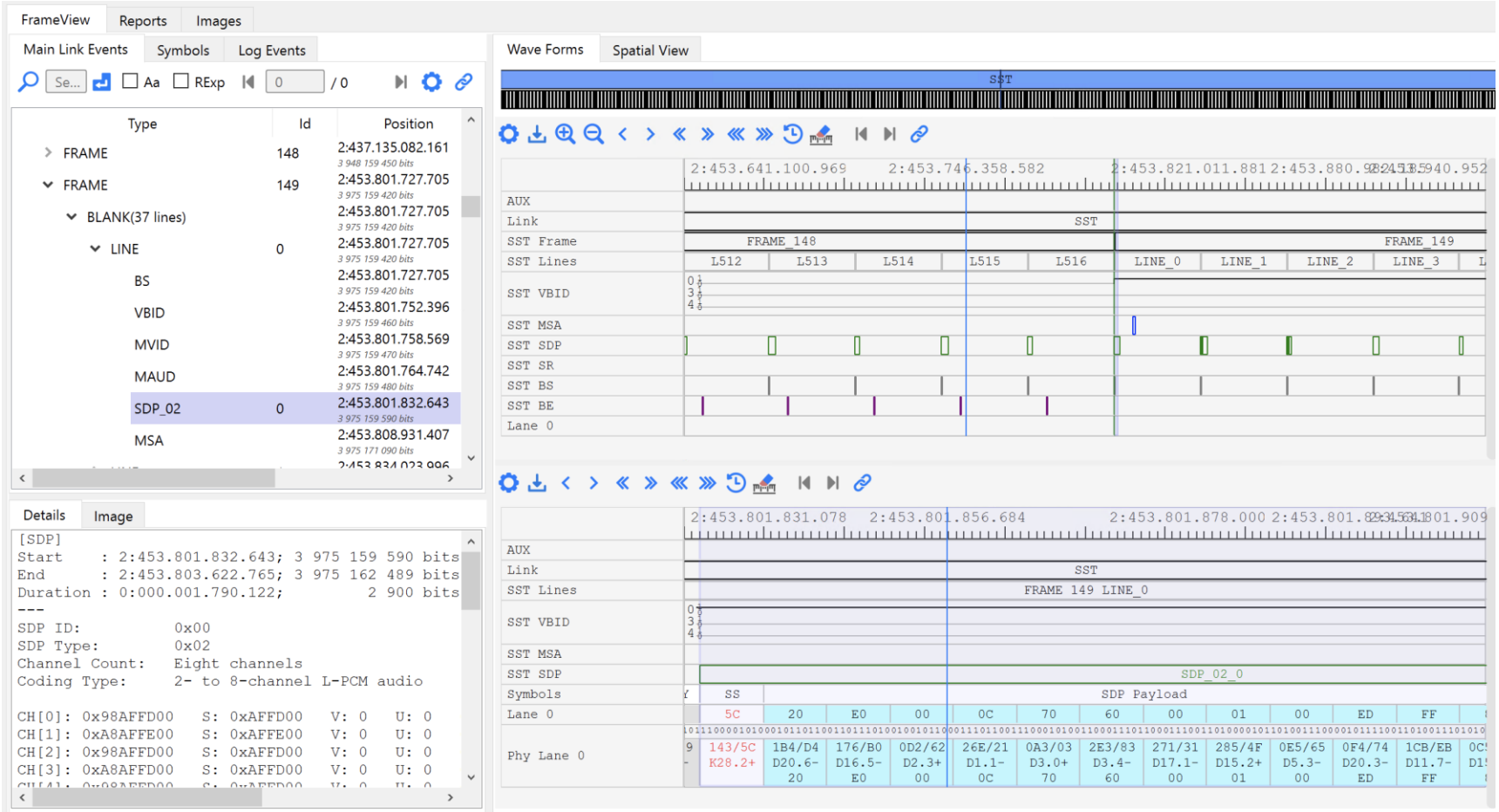
- S_{tx} is the number of audio samples received from the Source DUT over n consecutive lines
- F_s is the nominal audio sampling rate
- H_{total} is the horizontal total
- F_p is the pixel rate
- n is the number of lines

Source #1

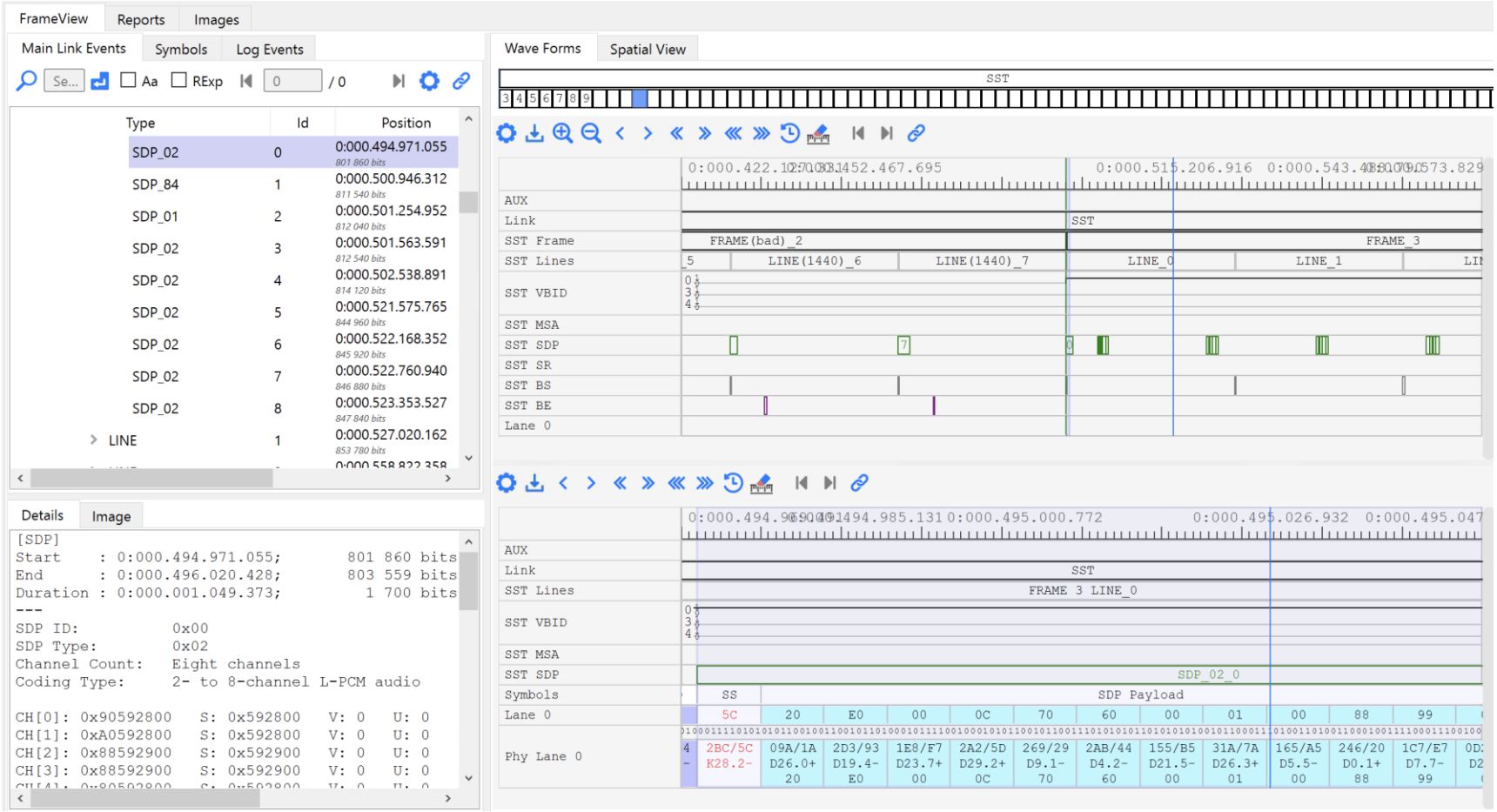

FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Se...
Aa
RExp
0
/ 0
Type
Id
Position
MVID
0:423.487.989.810
684 619 240 bits
MAUD
0:423.487.995.996
684 619 250 bits
MSA
0:423.488.057.854
684 619 350 bits
SDP_01
0
0:423.488.336.212
684 619 800 bits
SDP_84
1
0:423.488.645.499
684 620 300 bits
SDP_02
2
0:423.488.954.787
684 620 800 bits
SDP_02
3
0:423.489.264.074
684 621 300 bits
SDP_02
4
0:423.489.573.361
684 621 800 bits
SDP_02
5
0:423.489.882.648
684 622 300 bits
SDP_02
6
0:423.490.191.936
684 622 800 bits
Details
Image
[SDP]
Start : 0:423.488.954.787; 684 620 800 bits
End : 0:423.489.264.073; 684 621 299 bits
Duration : 0:000.000.309.286; 500 bits

SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x90748100 S: 0x748100 V: 0 U: 0
CH[1]: 0xA8748000 S: 0x748000 V: 0 U: 0
CH[2]: 0x88748000 S: 0x748000 V: 0 U: 0
CH[3]: 0x88748000 S: 0x748000 V: 0 U: 0
Wave Forms
Spatial View
SST
0:423.367.757.013
0:423.456.473.270
0:423.494.518.573
0:423.532.563.875
0:423.570.609
AUX
Link
SST
SST Frame
FRAME_26
FRAME_27
SST Lines
)_521
LINE(1440)_522
LINE(1440)_523
LINE(1440)_524
LINE_0
LINE_1
LINE
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
0:423.488.940.050
0:423.488.984.552
0:423.489.000.218
0:423.489.031
AUX
Link
SST
SST Lines
FRAME 27 LINE_0
SST VBID
SST MSA
SST SDP
SDP_02_2
Symbols
SS
SDP Payload
Lane 0
5C
20
E0
00
0C
70
60
00
01
00
01
44
Phy Lane 0
D+
143/5C K28.2+
25C/3C D28.1- 20
239/E0 D0.7- E0
09E/1E D30.0- 00
19C/DC D28.6- 0C
1EC/EC D12.7- 70
351/01 D1.0+ 60
15A/BA D26.5- 00
299/59 D25.2- 01
223/E3 D3.7+ 00
09D/1D D29.0- 01
372/12 D18.0- 44

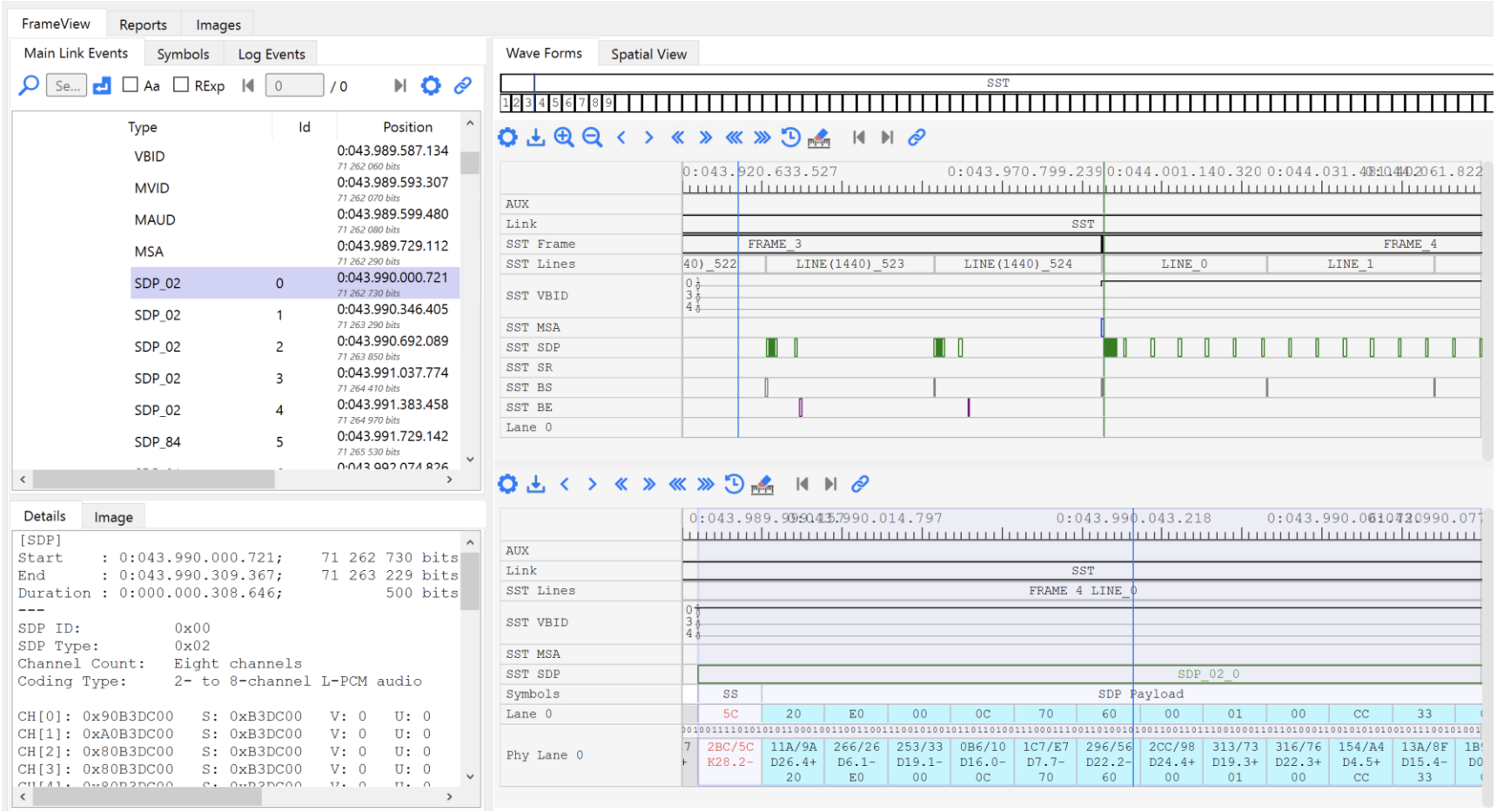
Source #2


FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Aa
RExp
/ 0
Type
Id
Position
FRAME 148 2:437.135.082.161
FRAME 149 2:453.801.727.705
BLANK(37 lines) 2:453.801.727.705
LINE 0 2:453.801.727.705
BS 2:453.801.727.705
VBID 2:453.801.752.396
MVID 2:453.801.758.569
MAUD 2:453.801.764.742
SDP_02 0 2:453.801.832.643
MSA 2:453.808.931.407
Details
Image
[SDP]
Start : 2:453.801.832.643; 3 975 159 590 bits
End : 2:453.803.622.765; 3 975 162 489 bits
Duration : 0:000.001.790.122; 2 900 bits
SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x98AFFD00 S: 0xAFFD00 V: 0 U: 0
CH[1]: 0xA8AFFE00 S: 0xAFFE00 V: 0 U: 0
CH[2]: 0x98AFFD00 S: 0xAFFD00 V: 0 U: 0
CH[3]: 0xA8AFFD00 S: 0xAFFD00 V: 0 U: 0
Wave Forms
Spatial View
SST
AUX
Link
SST Frame
SST Lines
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
FRAME 148
FRAME 149
L512
L513
L514
L515
L516
LINE_0
LINE_1
LINE_2
LINE_3
2:453.641.100.969
2:453.746.358.582
2:453.821.011.881
2:453.801.831.078
2:453.801.856.684
2:453.801.878.000
FRAME 149 LINE_0
SDP_02_0
Symbols
Phy Lane 0
SS
SDP Payload
5C
20
E0
00
0C
70
60
00
01
00
ED
FF
143/5C K28.2+
1B4/D4 D20.6- 20
176/B0 D16.5- E0
0D2/62 D2.3+ 00
26E/21 D1.1- 0C
0A3/03 D3.0+ 70
2E3/83 D3.4- 60
271/31 D17.1- 00
285/4F D15.2+ 01
0E5/65 D5.3- 00
0F4/74 D20.3- ED
1CB/EB D11.7- FF

Source #3


FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Type
Id
Position
SDP_02 0 0:000.494.971.055 801 860 bits
SDP_84 1 0:000.500.946.312 811 540 bits
SDP_01 2 0:000.501.254.952 812 040 bits
SDP_02 3 0:000.501.563.591 812 540 bits
SDP_02 4 0:000.502.538.891 814 120 bits
SDP_02 5 0:000.521.575.765 844 960 bits
SDP_02 6 0:000.522.168.352 845 920 bits
SDP_02 7 0:000.522.760.940 846 880 bits
SDP_02 8 0:000.523.353.527 847 840 bits
LINE 1 0:000.527.020.162 853 780 bits
Details
Image
[SDP]
Start : 0:000.494.971.055; 801 860 bits
End : 0:000.496.020.428; 803 559 bits
Duration : 0:000.001.049.373; 1 700 bits
SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x90592800 S: 0x592800 V: 0 U: 0
CH[1]: 0xA0592800 S: 0x592800 V: 0 U: 0
CH[2]: 0x88592900 S: 0x592900 V: 0 U: 0
CH[3]: 0x88592900 S: 0x592900 V: 0 U: 0
Wave Forms
Spatial View
SST
AUX
Link
SST Frame
SST Lines
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
FRAME(bad)_2
FRAME_3
LINE(1440)_6
LINE(1440)_7
LINE_0
LINE_1
FRAME 3 LINE_0
SDP_02_0
Symbols
SS
SDP Payload
Phy Lane 0

Source #4


FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Se...
Aa
RExp
0
/ 0
Type
Id
Position
VBID
0:043.989.587.134
71 262 060 bits
MVID
0:043.989.593.307
71 262 070 bits
MAUD
0:043.989.599.480
71 262 080 bits
MSA
0:043.989.729.112
71 262 290 bits
SDP_02
0
0:043.990.000.721
71 262 730 bits
SDP_02
1
0:043.990.346.405
71 263 290 bits
SDP_02
2
0:043.990.692.089
71 263 850 bits
SDP_02
3
0:043.991.037.774
71 264 410 bits
SDP_02
4
0:043.991.383.458
71 264 970 bits
SDP_84
5
0:043.991.729.142
71 265 530 bits
Details
Image
[SDP]
Start : 0:043.990.000.721; 71 262 730 bits
End : 0:043.990.309.367; 71 263 229 bits
Duration : 0:000.000.308.646; 500 bits

SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x90B3DC00 S: 0xB3DC00 V: 0 U: 0
CH[1]: 0xA0B3DC00 S: 0xB3DC00 V: 0 U: 0
CH[2]: 0x80B3DC00 S: 0xB3DC00 V: 0 U: 0
CH[3]: 0x80B3DC00 S: 0xB3DC00 V: 0 U: 0
Wave Forms
Spatial View
SST
0:043.920.633.527
0:043.970.799.239
0:044.001.140.320
AUX
Link
SST
SST Frame
FRAME_3
FRAME_4
SST Lines
LINE(1440)_523
LINE(1440)_524
LINE_0
LINE_1
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
0:043.990.014.797
0:043.990.043.218
FRAME 4 LINE_0
SDP_02_0
Symbols
SS
SDP Payload
5C
20
E0
00
0C
70
60
00
01
00
CC
33
Phy Lane 0
2BC/5C K28.2-
11A/9A D26.4+ 20
266/26 D6.1- E0
253/33 D19.1- 00
0B6/10 D16.0- 0C
1C7/E7 D7.7- 70
296/56 D22.2- 60
2CC/98 D24.4+ 00
313/73 D19.3+ 01
316/76 D22.3+ 00
154/A4 D4.5+ CC
13A/8F D15.4- 33

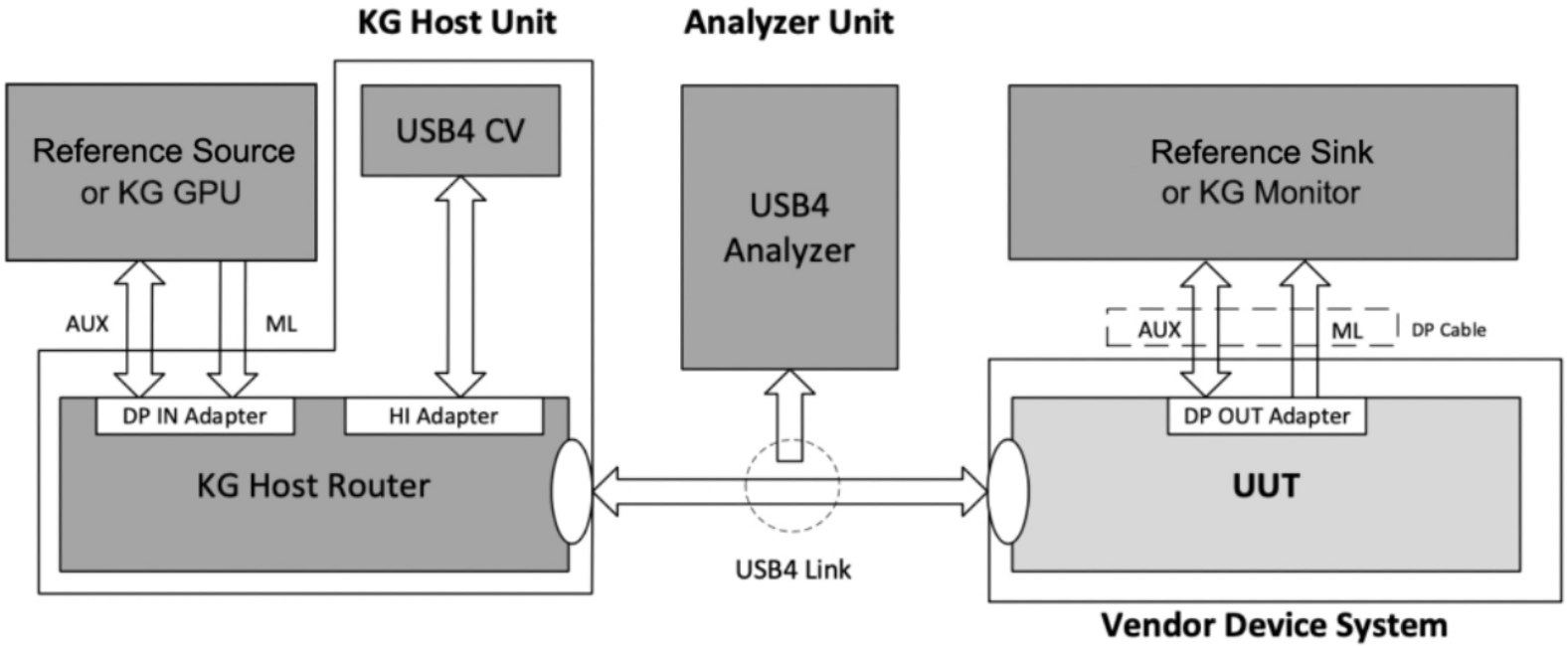
Audio CTS (Conclusions)

- No easy way to upgrade DP 1.4 8b/10b SST Audio CTS to cover DP 2.1 requirements
- Due to test time increase, it is suggested to test Audio at UHBR rates under separate tests. Under discussion
- It is suggested to test Audio at 8b/10b link rates also in MST mode. Not covered yet by SCR under review. To be discussed

USB4 DP Tunneling CTS

- Collaborating closely with USB-IF and ATCs
- Revision 2.2 released in August 2024
- Test procedures for Host, Device and Hub
- Test Setups with Known Good Devices and DisplayPort Test Equipment as Reference Sink/Source.
- For Test Setups with Reference Sink/Source lists DP 2.1 Link Layer tests to be performed
- Work in progress. Looking for a balance between test coverage and test time

USB4 DP Tunneling CTS (continued)



Various updates after revision 1.0 release

- DP 2.1 Link Layer CTS is evolving and improving
- VESA Members actively reviewing and commenting DP 2.1 Link Layer CTS
- Comments are used to draft new tests and update existing test procedures
- Draft 5 of the SCR consolidating such updates is under adoption vote

Source DUT updates

- 4.2.2.13 Native AUX defer retry validation for Source DUT before LT
- 4.2.2.14 Native AUX defer retry validation for Source DUT during LT just after TPS1
- 4.9.1.22 With 1 emulated LTTPR, Successful Link Training at any Lane Counts and Link Speeds
- 4.3.2.5 Lane Count Reduction (Deprecated)

Sink DUT updates

- 5.6.3.7 DSC Validation for max supported pixel rate format at max UHBR Rate
- 5.4.3.3 Entering and Exiting Power Save Mode at UHBR rate
- 5.4.3.4 Resumption of Main-Link Activity after Extended Idle at UHBR rate
- 5.7.14.7 Hblank and Vblank Validation
- Allow Reference Sink to have DSC capability cleared for improving uncompressed Video tests automation at UHBR link rates

LTTPR DUT updates

- 7.1.4.8 With 0 emulated LTTPR, Link Training with UFP fails when DFP not able to do EQ lock at max supported Lane Count and 128b/132b DP Link Speeds in Non-transparent mode
- 7.1.4.9 With 5 emulated LTTPR, Link Training with UFP fails when DFP not able to do EQ lock at max supported Lane Count and 128b/132b DP Link Speeds in Non-transparent mode
- 7.1.4.10 With 5 emulated LTTPR, Link Training with successful link training at max supported Lane Count and 128b/132b DP Link Speeds in Non-transparent mode

Minimal Vblank and Hblank requirements

- *"There are quite a few "high" refresh rate monitors (mainly for a gaming use case) that has a VBLANK period way shorter than 300 uSec, let alone 460 uSec listed as the minimum VBLANK period in VESA CVT Standard"*
- Sinks that do not honor specified minimum Vblank and Hblank periods can have interoperability issues with Source devices that expect these intervals to meet specification limits
- New EDID/DisplayID compliance test for Sink devices is drafted: 5.7.14.7 Hblank and Vblank Validation

Planned updates to DP 2.1 LL CTS

- Introduce MST tests
- Update Branch device tests to DP 2.1 requirements
- Introduce Panel Replay and ALPM tests
- Introduce HBR Audio tests

eDP and DP v 2.1 PHY CTS Overview and Updates

Jim Choate
VESA Compliance Program Manager
10/07/2024

Agenda

- DP2.1a PHY Updates
- DP2.1a Electrical Compliance Test Requirements
- DP2.1a Transmitter Test
- DP2.1a Receiver Test
- eDP PHY Electrical Conformance Testing

DP2.1a PHY Updates

DP2.1 to DP2.1a Electrical Updates

- No changes in 8b/10b electrical compliance testing
- DP54 cable certification replaced DP40
  - Provides 13.5G sources and sinks with longer length cable options
- New DP54 Cable model for UHBR10 and UHBR13.5 Source testing
- Test Limit changes in Source and Sink testing

- UHBR10
  - DPTX TP2
    - Total Jitter =380 mUI
    - Data-Dependent Jitter =160 mUI
    - Eye Width = 600 mUI
    - Eye Height = 242 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 185 mV
  - DPTX TP3_EQ
    - Total Jitter =450 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 115 mV
  - DPRX TP3_EQ
    - Total Jitter =485 mUI
    - Data-Dependent Jitter =240 mUI
    - Eye Width = 540 mUI
    - Eye Height = 112 mV
- UHBR20
  - DPTX TP2
    - Total Jitter =435 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 240 mV
  - DPTX TP3_EQ
    - Total Jitter =455 mUI
    - Data-Dependent Jitter =210 mUI
    - Eye Width = 560 mUI
    - Eye Height = 100 mV
  - DPRX TP3_EQ
    - Data-Dependent Jitter =255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV

- UHBR10
  - DPTX TP2
    - Total Jitter =440 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 550 mUI
    - Eye Height = 162 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 200 mV
  - DPTX TP3_EQ
    - Total Jitter =515 mUI
    - Data-Dependent Jitter =245 mUI
    - Eye Width = 520 mUI
    - Eye Height = 80 mV
  - DPRX TP3_EQ
    - Total Jitter =530 mUI
    - Data-Dependent Jitter =260 mUI
    - Eye Width = 520 mUI
    - Eye Height = 73 mV
- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI

DP2.1a Electrical Compliance Test Requirement

DisplayPort Interface

Main Link

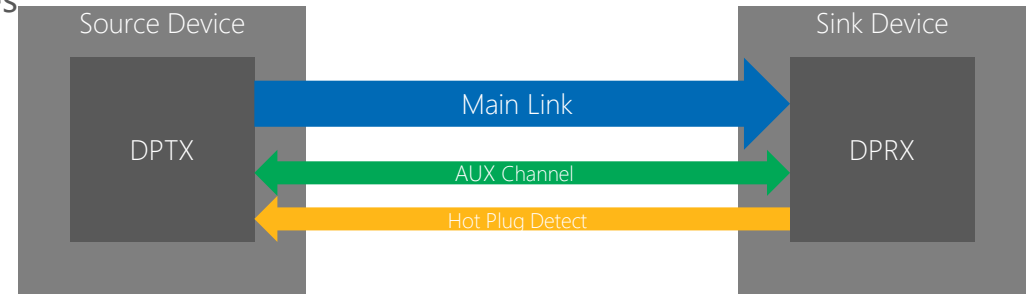
- Display data transfer
- 4 unidirectional high-speed lanes
- Multiple bitrates supported

AUX Channel

- Link management
- Test mode control
- 1 bidirectional low-speed lane

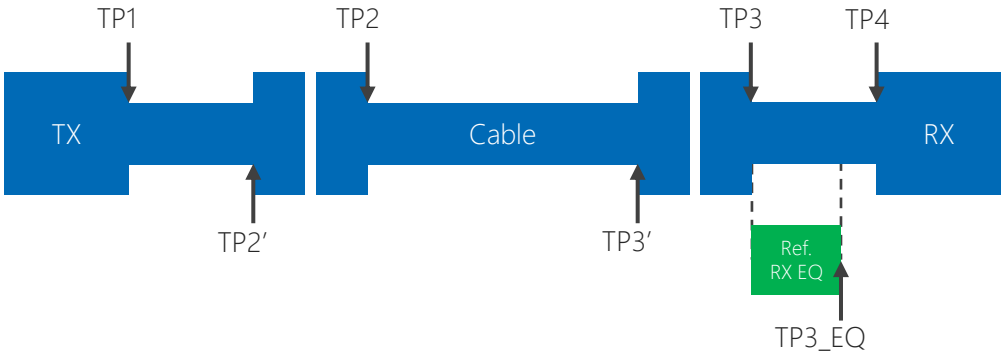
Hot Plug Detect

- Source detects presence of sink
- Sink notifies of status changes via IRQ



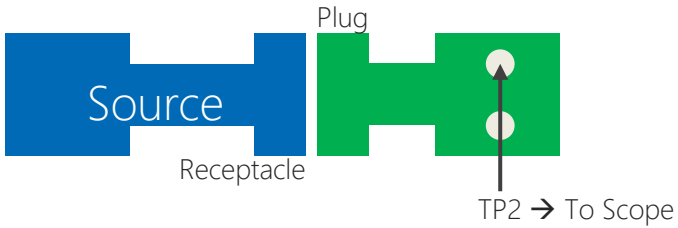
Test Points

Test Point	Definition
TP1	Source transmitter pins.
TP2	Test interface of a TPA, next to mated connection to a DP source.
TP2’	RX JTOL signal injection point for DUTs with plug.
TP2_CTLE	RX JTOL calibration and test point for DUTs with plug.
TP3	Test interface of a TPA, next to mated connection to a DP sink.
TP3’	Signal injection point to a DP sink.
TP3_EQ	TP3 using a defined cable model with equalization applied.’
TP3_CTLE	TP3 using a defined HBR3 cable model with CTLE applied.
TP3_DFE	TP3 using a defined HBR3 cable model with CTLE and DFE applied.
TP4	Sink receiver pins.

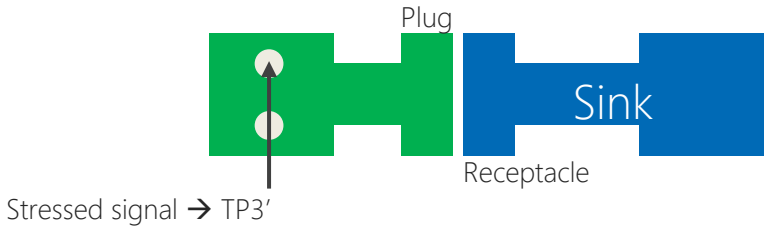


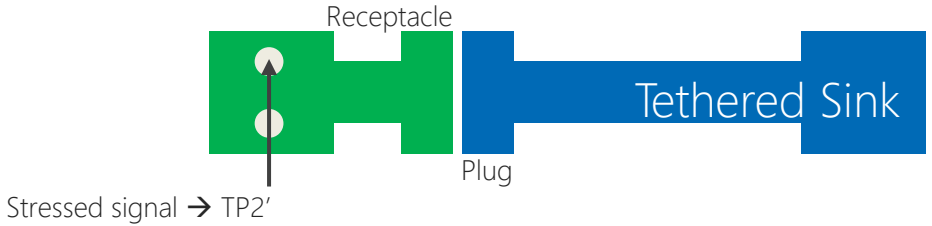
Test Point Access Examples

DPTX Testing



DPRX Testing





How to test the PHY layer?

Source

- Configure the source to output test patterns with certain drive settings → **AUX controller**
- Embed worst-case channels, apply equalization on the oscilloscope
- Run measurements

Sink

- Generate the stress signal with a pattern generator
- Guide the sink through Link Training → **AUX controller**
- Read built-in error counter → **AUX controller**

DP2.1a Transmitter Test

Electrical Transmitter Tests

Item	Name	Normative/ Informative
3.1	Eye Diagram Test	Normative
3.2	HBR/RBR Non-PE Level Verification Test	Normative
3.3	HBR/RBR PE Level Verification and Maximum Differential Peak-to-Peak Voltage Test	Normative
3.4	HBR3/HBR2 PE Level and Equalization Verification Test	Normative
3.5	HBR3/HBR2 $V_{TX\_DIFFp\text{-}p\_MAX}$ Test	Normative
3.6	Inter-pair Skew Test	Informative
3.7	Intra-pair Skew Test	Informative
3.8	AC Common Mode Noise Test	Informative
3.9	Non-ISI Jitter Measurement Test	Normative
3.10	HBR3 TX Differential RL Test	Informative
3.11	TJ/RJ/DJ Measurement Tests	Normative
3.12	Main-Link Frequency Compliance Test	Normative
3.13	Spread-spectrum Modulation Frequency Test	Normative
3.14	Spread-spectrum Modulation Deviation Test	Normative
3.15	dF/dT Spread-spectrum Deviation High-frequency Variation Test	Informative

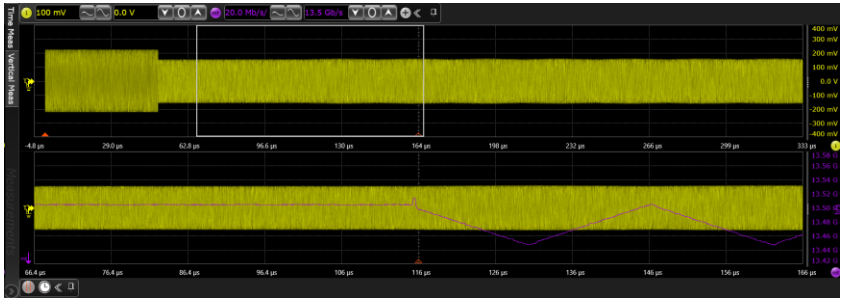
8b/10b

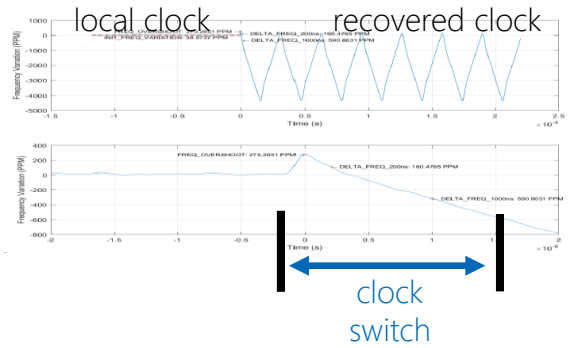
Item	Name	Normative/ Informative
4.2	Preset and CTLE-DFE Declaration	Normative
4.3	UHBR Source Transmitter Equalization	Normative
4.4	UHBR Bit Rate	Normative
4.4	UHBR Unit Interval	Informative
4.5	UHBR SSC Down Spread Range, Rate, Phase Deviation, and Slew Rate	Normative
4.6	UHBR Embedded Re-timer Frequency Variation	Normative
4.7	UHBR TP2 Eye at 1E-6 BER	Normative
4.8	UHBR TP2 Jitter at 1E-9 BER	Normative
4.9	UHBR AC Common Mode Nosie Test	Informative
4.10	UHBR TP3_EQ Eye at 1E-6	Normative
4.11	UHBR TP3_CTLE Jitter at 1E-9	Informative
4.12	UHBR Transmitter Return Loss	Informative

128b/132b

LTTPR Frequency Variation Test

- LTTPRs are needed as total channel loss increases with the PHY rate
  - Longer channel
  - More complex link training
- LTTPR Re-timer Clock Switch Test Mode
  - DPCD 0x0010B – 0x0010Eh [7] =1
- Initial Test Challenges
  - Entering Clock Switch test mode
  - Triggering on LTTPR local clock event





DP TX testing challenges

- The test time for DP TX is significant
- DP Source not supporting PHY Test Automation
  - DP Source does not transmit the compliance pattern

DP2.1a Receiver Test

Electrical Receiver Tests

Item	Name	Normative/ Informative
5.1	8b/10b DP Sink JTOL Test	Normative

Item	Name	Normative/ Informative
6.1	128b/132b DP UHBR Sink JTOL Test	Normative

Item	Calibration Point	Name
5.1.3.1.1	TP1-TP3	HBR3 Jitter Calibration
5.1.3.1.2	TP1-TP3	HBR2 Jitter Calibration
5.1.3.1.3	TP1-TP3	HBR Jitter Calibration
5.1.3.1.4	TP2/TP3	HBR3 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR2 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR Eye Height and Total Jitter Calibration
5.1.3.1.5	TP1/TP3	HBR3/HBR2/HBR Crosstalk Calibration
5.1.3.2	TP2/TP3	RBR Jitter Calibration
5.1.3.2	TP3	RBR Eye Height Calibration
5.1.3.2.1	TP3	RBR Crosstalk Calibration

Item	Calibration Point	Name
6.1.3.1.4.1	TP1	AC Common-Mode Interference Calibration
6.1.3.1.4.2	TP1	Random Jitter Calibration
6.1.3.1.4.3	TP1	Periodic Jitter Calibration
6.1.3.1.4.4	TP1	Total Jitter Calibration
6.1.3.1.4.5	TP1	Eye Height Calibration
6.1.3.1.5	TP3	Insertion Loss Calibration
6.1.3.1.6	TP3	Eye Diagram Calibration

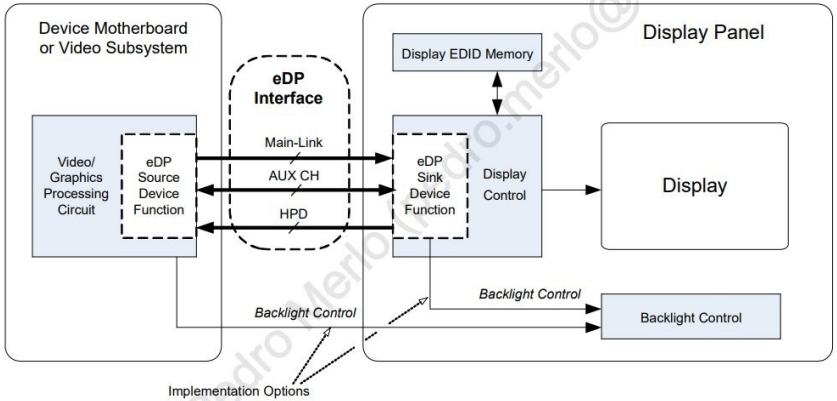
DP RX testing challenges

- DP Sink does not enable error count registers
- DP RX Preset calibration to be required – impacts TE correlation results
- Calibrations take a significant amount of time
  - Different setup needs for 8b/10b and 128b/132b

Embedded DisplayPort

eDP

- Standardized features and interoperability guidelines
  - Feature set determined by the system integrator
- Current specification is eDP2.0
  - Extended and updated from DP1.5
- No compliance program = Conformance Test!!



Key Differences eDP vs DP2.1a 8b/10b rates

Required

- DPCD registers for eDP
- Reduced AUX timing
- Enhanced framing
- Fast link training (sink)
- eDP-specific sink noise/jitter budget, reference EQ

Optional

- Low AUX voltage swing
- Source detection by way of AUX CH
- STREAM_STATUS_CHANGED bits support
- GUID registers support
- Fast link training (host)
- Reduced main-link voltage swing level
- EDID
- HPD pin on sink device

Recommended

- Fewest number of lanes possible

AUX Channel Differences

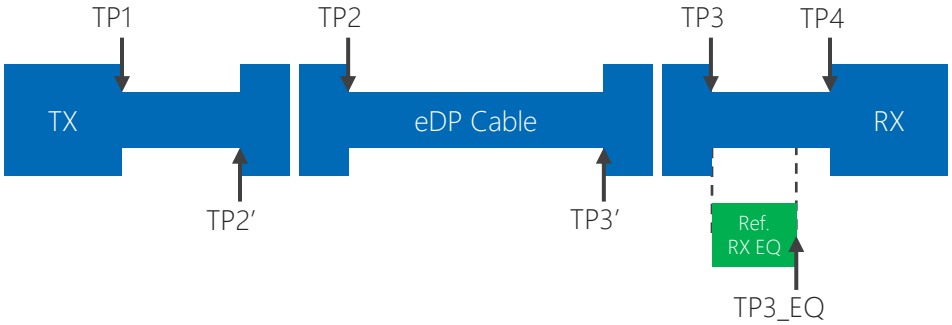
- No AC-coupling capacitors on Sink device side
- No pull-up/-down resistors
- Why?
  - The Sink device does not monitor the common mode voltage on AUX_CH_P and AUX_CH_N for Source device Hot Plug/Unplug and powered/unpowered detection

eDP Electrical Specification

- Low voltage swing levels
- Framework to apply optional customized voltage swings
- Reduced RX differential voltage sensitivity
- New transfer rates
- Framework to apply jitter specifications to optional customized frequencies
- Same Link Training procedures and voltage swing tables like DP, but with lower signal voltages

eDP Transmitter Test

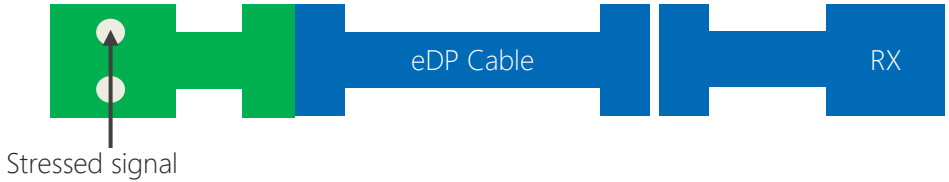
- Test Point/Fixture

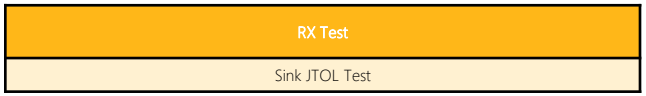


Recommended Source Main-Link TX Electrical Specification
Link Rate
Unit Interval
Total Jitter
Residual ISI
Non-ISI
Eye Diagram

eDP Receiver Test

- Test Point/Fixture





Calibration Point	RX Calibration
TP1	Sinusoidal Jitter Calibration
TP1	Random Jitter Calibration
TP3	Residual ISI
TP3	Eye Diagram
TP3	Crosstalk

eDP2.0 Update

- eDP2.0 published on September 19, 2024
- Supports 128b/132b encoding
- Supports UHBR data rates
  - UHBR10, UHBR13.5 and UHBR20
- Leverages worst-case end-to-end link budget from DP2.1a

Thank You!

DP Alt Mode v 2.1 Overview and Updates

Tim Wei– Senior Application Engineer
Ellisys
October 7, 2024

Ellisys USB Test and Analysis Solutions

USB Explorer™ 350

Multi-function USB Type-C®, USB 3.2, and Power Delivery Protocol Test Platform

VESA-Approved Tester for DisplayPort ALT Mode

Type-C Tracker™

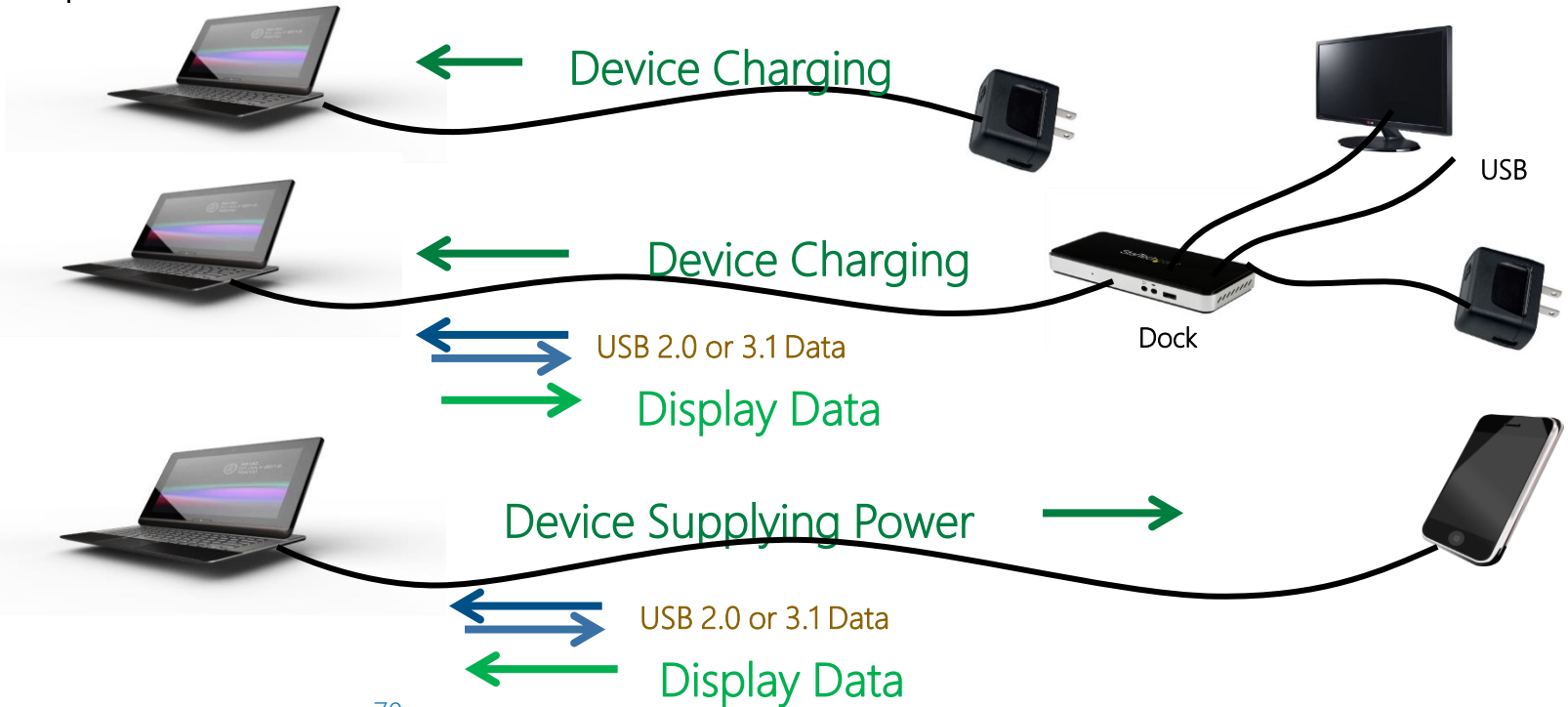
Protocol and Electrical Analysis Tool for USB Type-C® Standards

Includes DP AUX and DP ALT Support

ellisys
Better Analysis

Example USB Type-C Configurations

Either end can serve as USB Host, USB-PD Power Consumer, and DisplayPort Video Source (these services are independent of each other



DP Alt Mode over USB-C Ecosystem is Mainstream


USB-C Tablets


USB-C Laptops


USB-C Displays


Multi Function Adapters

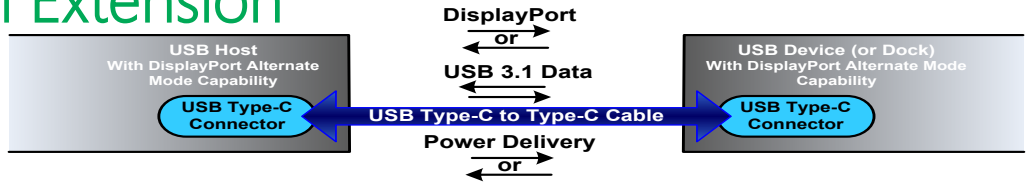
All types of certified adapters available

- C to DP adapters, Multifunction docks
- Type C protocol converters (HDMI, VGA, DVI) using DP Alt Mode

More are certified every week

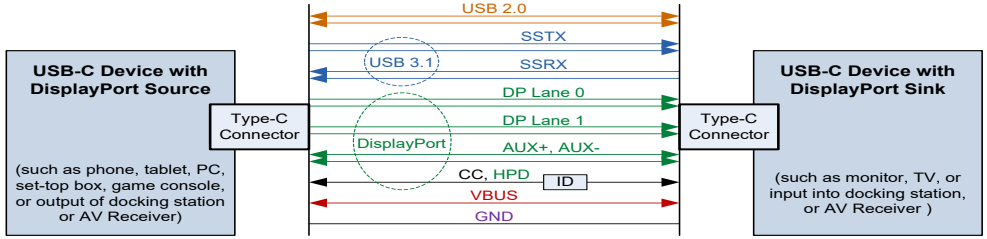
- Major PC OEMs continue to launch new products with DP Alt Mode over USB-C
- Major Display OEMs continue to add USB-C inputs to their products

USB-C Connector Functional Extension DP Alt Mode



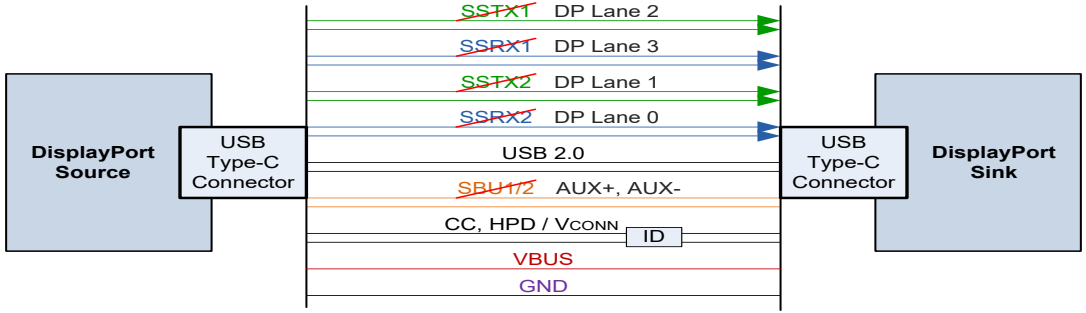
- A passive Full Feature USB Type-C to Type-C cable can carry up to four DisplayPort lanes
  - Same performance and features as a standard DisplayPort connection
  - Allows DisplayPort data rates to increase in the future, since the USB Type-C connector has very high data rate capability
- DisplayPort can be combined with USB 3.2 operation over the same USB Type-C cable
- USB 2.0 and USB Power Delivery is available in all configurations

2xDisplayPort and USB 3.2 over a Standard USB-C Cable



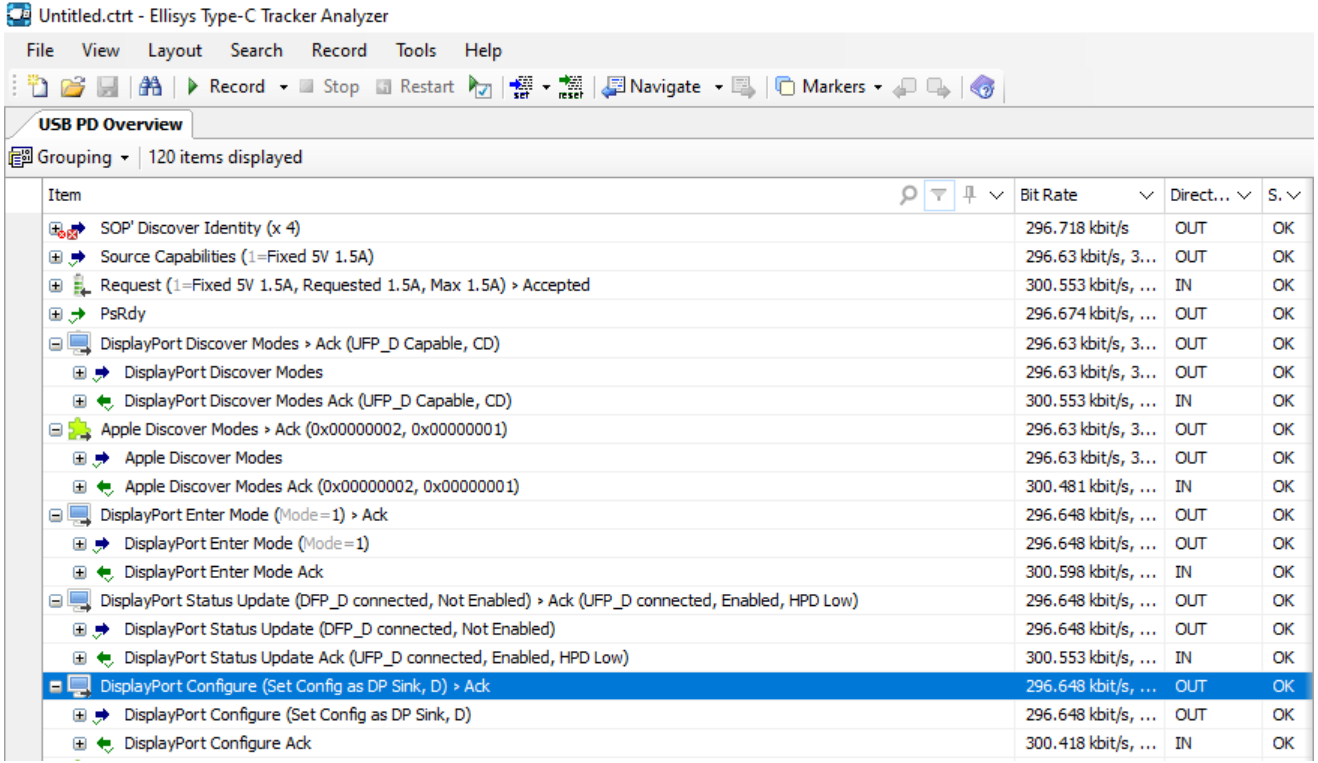
- Uses a standard "Full Feature" USB-C to USB-C cable which is designed to include DisplayPort
- The above configuration uses two high-speed lanes each for DisplayPort and USB 3.2
  - Ideal for docking stations, or for displays or TVs that include USB 3.2 functions
- DisplayPort performance provided by two lanes
  - HBR3: 4K(3840x2160)@60fps 24bpp
  - UHBR20: 8K (7680x4320)@30fps 30bpp

4xDP Over a USB Type-C to USB Type-C Full Feature Passive Cable



- Utilizes optional DP Alt Mode capability of USB Type-C connector
- DisplayPort can use all four high speed lanes to deliver full DisplayPort performance
- The DisplayPort AUX Channel uses the SBU pins
- The DisplayPort HPD / IRQ is transmitted over the CC pin using the USB-PD protocol
- USB 2.0 and USB Power Delivery always available
- DisplayPort performance provided by four lanes
  - HBR3: 5K (5120x2800)@60fps 24bpp
  - UHBR20: 10K (10240x4320)@60fps 24bpp

Typical DisplayPort Alternate Mode Flow



DisplayPort Alternate Mode 2.1 Update

- SVDM Header Update (by USB PD Spec)
- Cable DP Capabilities VDO update to support UHBR20 and UHBR13.5
  - Both passive and active cables
- SOP' Active Cable DisplayPort Configurations VDO update
- DP Capabilities VDO Update (DPAM Version field)
- SOP DisplayPort Configurations VDO Update
  - Cable information
  - DPAM Version
- DisplayPort Status Update VDO Update

SVDM Header Update

12:11	**Structured VDM Version (Minor)[a]**	Version number (Minor) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier 01b = Version 2.1 All other values are RESERVED.
14:13	**Structured VDM Version (Major)[a]**	Version number (Major) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier. 01b = Version 2.x. (x indicates SVDM minor version) All other values are RESERVED.

12:11 was reserved

Cable DP Capabilities VDO update

Table 4-5: SOP' Cable DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)[a]

Bit(s)	Description	Values
1:0	**RESERVED**	RESERVED (always 00b).
5:2	**Signaling for Transport of DisplayPort Protocol[b]**	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[c]
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**DP Source Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported. 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
23:16	**DP Sink Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
25:24	**RESERVED**	RESERVED (always 00b).
26[d]	**UHBR13.5**	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[c]
27	**RESERVED**	RESERVED (always 0).
29:28[d]	**Active Component**	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30	**DPAM Version**	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 4-2: Active Cable DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)

Bit(s)	Description	Values
1:0	RESERVED	RESERVED (always 00b).
5:2	Signaling for Transport of DisplayPort Protocol[a]	XXX1b = Supports *DP* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	DP Source Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported. All other values are RESERVED.
23:16	DP Sink Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). All other values are RESERVED.
31:24	RESERVED	RESERVED (always 00h).

a. "X" value indicates "Don't Care."

Active Cable DisplayPort Configurations VDO update

Table 4-7: SOP' Active Cable DisplayPort Configurations

Bit(s)	Description	Values
1:0	**Select Configuration**	00b = Set configuration for *USB*.[a] 01b = Set configuration for active cable as a *DP* Source device (UFP_U is a *DP* Source device).[b] 10b = Set configuration for active cable as a *DP* Sink device (UFP_U is a *DP* Sink device).[b] 11b = RESERVED.
5:2	**Signaling for Transport of DisplayPort Protocol**	0h = Bit rate is unspecified (used only when the Select Configuration field is programmed for USB Configuration). 1h = Select *DP* bit rates and electrical settings. All other values are RESERVED.
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**Configure Active Cable Pin Assignment**	00h = Deselect pin assignment. 04h = Select Pin Assignment C.[c] 08h = Select Pin Assignment D.[d] 10h = Select Pin Assignment E.[e] All other values are RESERVED.
31:16	**RESERVED**	RESERVED (always 0000h).

Table 4-3: Active Cable *DisplayPort Status Update*

Bit(s)	Description	Values
2:0	RESERVED	RESERVED (always 00b).
3	Enabled	0 = Active cable *DP* functionality is disabled. 1 = Active cable *DP* functionality is enabled and operational.
31:4	RESERVED	RESERVED (always 0000000h).

DP Capabilities VDO Update

Table 5-6: DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	**Port Capability**	00b = RESERVED. 01b = *DP* Sink Device Capable (including *DP* Branch device). 10b = *DP* Source Device Capable (including *DP* Branch device). 11b = Both *DP* Source and Sink Device Capable.
5:2	**Signaling for Transport of DisplayPort Protocol**	XXX1b = Supports *DP* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	**Receptacle Indication**	0 = *DP* interface is presented on a *USB-C* plug. 1 = *DP* interface is presented on a *USB-C* receptacle.
7	**USB 2.0 Signaling Not Used**	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	**DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)**	00000000b = *DP* Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	**DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)**	00000000b = *DP* Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
29:24	**RESERVED**	RESERVED (always 00h).
31:30	**DPAM Version[i]**	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 5-5: DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED. 01b = *DP* Sink device-capable (including *DP* Branch device). 10b = *DP* Source device-capable (including *DP* Branch device). 11b = Both *DP* Source and Sink device-capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = *DP* interface is presented on a *USB-C* plug. 1 = *DP* interface is presented on a *USB-C* receptacle.
7	USB 2.0 Signaling Not Used	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	DP Source Device Pin Assignments Supported (reported by a *DP* Source device receptacle or *DP* Sink device (direct-attach) plug)	00000000b = *DP* Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a *DP* Sink device receptacle or *DP* Source device (direct-attach) plug)	00000000b = *DP* Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
31:24	RESERVED	RESERVED (always 00h).

If SVDM Version is 2.1 or higher, DPAM Version field is applicable else this field shall be set to 00b.

A Bit More Background

From DisplayPort Alt Mode 2.0 Spec

Future versions of this Standard may describe other modes associated with the DP_SID. Such modes shall be identified by having a non-zero value in bits 31:24 of the VDO. The DFP_U shall examine the list of modes returned until it finds 0s in bits 31:24 of the VDO and a non-zero value in bits 23:0 of the VDO (i.e., DP Capabilities). The DFP_U and UFP_U shall use the corresponding offset (indexed from 1) as the Object Position in the following commands:

SOP DisplayPort Configurations VDO Update

Table 5-13: SOP DisplayPort Configurations

Bit(s)	Description	Values
1:0	**Select Configuration**	00b = Set configuration for *USB*.[a] 01b = Set configuration for UFP_U as a *DP* Source device.[b] 10b = Set configuration for UFP_U as a *DP* Sink device.[b] 11b = RESERVED.
5:2[c]	**Signaling for Cable Information Transport of DisplayPort Protocol**	XXX1b = Supports all defined *DP* bit rates up to HBR3 -or- capability is unknown XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[d]
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**Configure UFP_U Pin Assignment**	00h = Deselect pin assignment. 04h = Select Pin Assignment C.[e] 08h = Select Pin Assignment D.[f] 10h = Select Pin Assignment E.[g] All other values are RESERVED.
25:16	**RESERVED**	RESERVED (always 0000000000b).
26[h]	**Cable UHBR13.5 Support**	0 = Not supported.[i] ~~-or- capability is unknown~~ 1 = Supported.
27	**RESERVED**	RESERVED (always 0).
29:28[h]	**Cable Active Component**	00b = Passive -or- cable type is unknown 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30[j]	**DPAM Version**	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 5-8: DisplayPort Configurations

Bit(s)	Description	Values
1:0	Select Configuration	00b = Set configuration for *USB*.[a] 01b = Set configuration for UFP_U as a *DP* Source device.[b] 10b = Set configuration for UFP_U as a *DP* Sink device.[b] 11b = RESERVED.
5:2	Signaling for Transport of DisplayPort Protocol	0h = Bit rate is unspecified (used only when the Select Configuration field is programmed for USB Configuration). 1h = Select *DP* bit rates and electrical settings. All other values are RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	Configure UFP_U Pin Assignment	00h = De-select pin assignment. 04h = Select Pin Assignment C.[c] 08h = Select Pin Assignment D.[d] 10h = Select Pin Assignment E.[e] All other values are RESERVED.
31:16	RESERVED	RESERVED (always 0000h).

- This is the most challenging part for DPAM 2.1 DFP_U

DisplayPort Status Update VDO Update

Table 5-7: DisplayPort Status Update

Bit(s)	Description	Values
1:0	**DP Source/Sink Device Connected**	00b = Neither a *DP* Source device nor *DP* Sink device is connected, –or– the adapter is disabled. 01b = *DP* Source device is connected. 10b = *DP* Sink device is connected.[a] 11b = Both a *DP* Source and Sink device are connected.
2[b]	**Power Low**	0 = Adapter is not in low power state ~~is functioning normally or is disabled~~. 1 = Adapter has detected low power ~~and disabled *DP* support~~.
3[b]	**Enabled**	0 = Adapter *DP* functionality is disabled. 1 = Adapter *DP* functionality is enabled and operational.
4[d]	**Multifunction Preferred**	0 = No preference for multifunction. 1 = Multifunction is preferred.
5[c]	**DisplayPort/ USB Configuration Request**	0 = Request change to DisplayPort Configuration (if currently in USB Configuration). 1 = Request change to USB Configuration (if currently in DisplayPort Configuration).
6[c]	**Exit DisplayPort Alt Mode Request**	0 = Maintain the current mode. 1 = Request exit from DisplayPort Alt Mode (if currently in DisplayPort Alt Mode).
7[d]	**HPD State**	0 = HPD_Low. 1 = HPD_High.[e]
8[d]	**IRQ_HPD**	0 = IRQ_HPD has not been issued since the last status Message. 1 = IRQ_HPD.[f]
9[g]	**NO_DPAM_SUSPEND**	0 = UFP_U/ DP Sink device has no preference for entry into low power state. 1 = UFP_U/ DP Sink device prefers not to enter low power state.
31:10	**RESERVED**	RESERVED (always 0000000h).

Table 5-6: *DisplayPort Status Update*

Bit(s)	Description	Values
1:0	DP Source/Sink Device Connected	00b = Neither a *DP* Source device nor *DP* Sink device is connected, –or– the adapter is disabled. 01b = *DP* Source device is connected. 10b = *DP* Sink device is connected.[a] 11b = Both a *DP* Source and Sink device are connected.
2[b]	Power Low	0 = Adapter is functioning normally or is disabled. 1 = Adapter has detected low power and disabled *DP* support.
3[b]	Enabled	0 = Adapter *DP* functionality is disabled. 1 = Adapter *DP* functionality is enabled and operational.
4[b]	Multi-function Preferred	0 = No preference for multi-function. 1 = Multi-function is preferred.
5[b]	DisplayPort/ USB Configuration Request	0 = Request change to DisplayPort Configuration (if currently in USB Configuration). 1 = Request change to USB Configuration (if currently in DisplayPort Configuration).
6[b]	Exit DisplayPort Alt Mode Request	0 = Maintain the current mode. 1 = Request exit from DisplayPort Alt Mode (if currently in DisplayPort Alt Mode).
7[c]	HPD State	0 = HPD_Low. 1 = HPD_High.[d]
8[c]	IRQ_HPD	0 = IRQ_HPD has not been issued since the last status Message. 1 = IRQ_HPD.[e]
31:9	RESERVED	RESERVED (always 0000000h).

Three New timers:

- tAttentionSpacing min 10ms
- tHpdConvertPd max 5ms
- tAttentionToDPConfigure max 500ms

DPAM Version Resolution

Table 5-5: DPAM Version Resolution

DFP_U, Cable and UFP_U with DP SID	DFP_U	Cable	UFP_U	DPAM Version Resolution
DPAM Version	2.0 or earlier	2.0 or earlier	2.0 or earlier	2.0 or earlier[ab]
	2.1 or higher	2.0 or earlier	2.0 or earlier	2.0 or earlier[ab]
	2.0 or earlier	2.1 or higher	2.0 or earlier	2.0 or earlier[ab]
	2.0 or earlier	2.0 or earlier	2.1 or higher	2.0 or earlier[ab]
	2.1 or higher	2.1 or higher	2.0 or earlier	2.0 or earlier[ab]
	2.0 or earlier	2.1 or higher	2.1 or higher	2.0 or earlier[ab]
	2.1 or higher	2.0 or earlier	2.1 or higher	DPAM 2.1 or higher[c]
	2.1 or higher	2.1 or higher	2.1 or higher	2.1 or higher[d] (Shall support DPAM 2.1 or higher)

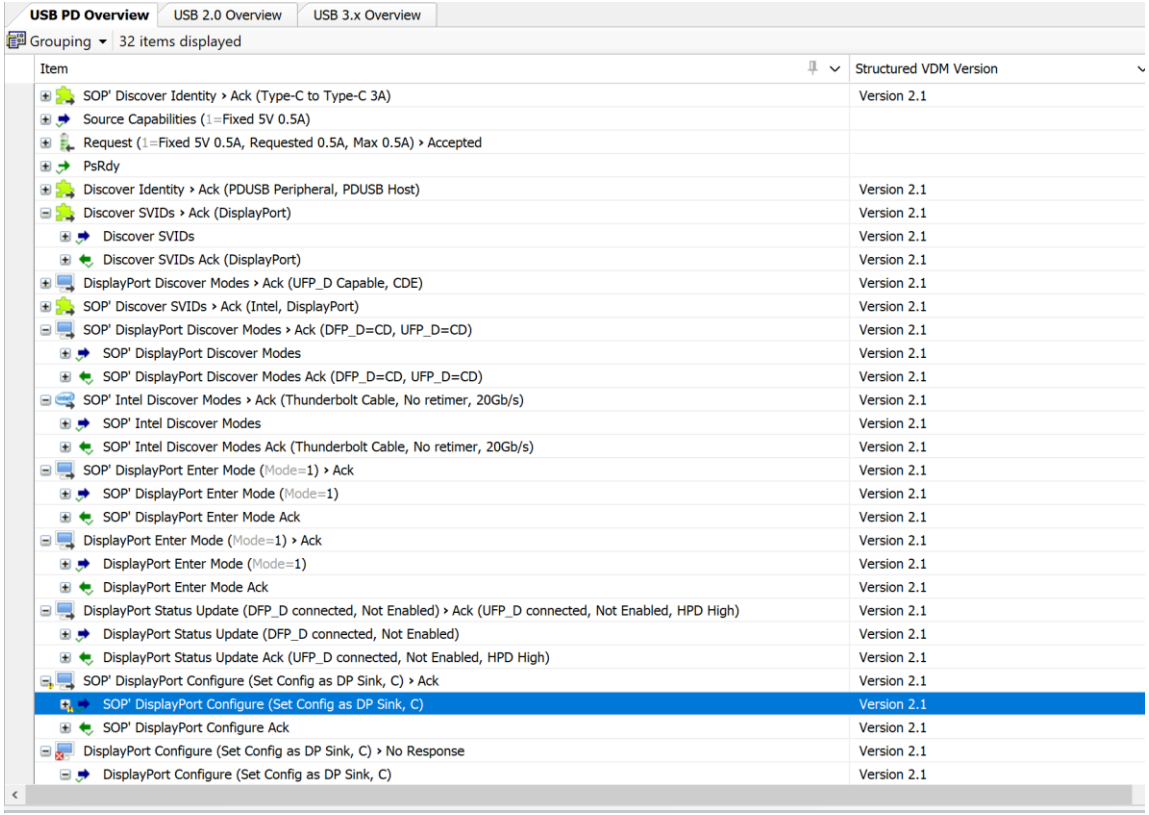
a. *If Initiator and Responder support SVDM Version 2.0 or earlier and if DisplayPort Alternate Mode is supported all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.0 or earlier.*

b. *If Initiator and Responder both support SVDM Version 2.1 or higher and if either Initiator or Responder supports DPAM Version 2.0 or earlier, then all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.0 or earlier.*

c. *When DPAM 2.1 or higher DFP_U and DPAM 2.1 or higher UFP_U are connected with a legacy active DPAM 2.0 cable, then the system shall exchange all DP Capabilities as per DisplayPort Alt Mode on USB Type-C specification 2.1 or higher but support HBR3 rates.*

d. *If Initiator and Responder both support SVDM Version 2.1 or higher and DPAM Version 2.1 all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.1 or higher.*

Typical DPAM 2.1 Flow



USB PD Overview | USB 2.0 Overview | USB 3.x Overview

Grouping | 32 items displayed

Item	Structured VDM Version
SOP' Discover Identity › Ack (Type-C to Type-C 3A)	Version 2.1
Source Capabilities (1=Fixed 5V 0.5A)	
Request (1=Fixed 5V 0.5A, Requested 0.5A, Max 0.5A) › Accepted	
PsRdy	
Discover Identity › Ack (PDUSB Peripheral, PDUSB Host)	Version 2.1
Discover SVIDs › Ack (DisplayPort)	Version 2.1
Discover SVIDs	Version 2.1
Discover SVIDs Ack (DisplayPort)	Version 2.1
DisplayPort Discover Modes › Ack (UFP_D Capable, CDE)	Version 2.1
SOP' Discover SVIDs › Ack (Intel, DisplayPort)	Version 2.1
SOP' DisplayPort Discover Modes › Ack (DFP_D=CD, UFP_D=CD)	Version 2.1
SOP' DisplayPort Discover Modes	Version 2.1
SOP' DisplayPort Discover Modes Ack (DFP_D=CD, UFP_D=CD)	Version 2.1
SOP' Intel Discover Modes › Ack (Thunderbolt Cable, No retimer, 20Gb/s)	Version 2.1
SOP' Intel Discover Modes	Version 2.1
SOP' Intel Discover Modes Ack (Thunderbolt Cable, No retimer, 20Gb/s)	Version 2.1
SOP' DisplayPort Enter Mode (Mode=1) › Ack	Version 2.1
SOP' DisplayPort Enter Mode (Mode=1)	Version 2.1
SOP' DisplayPort Enter Mode Ack	Version 2.1
DisplayPort Enter Mode (Mode=1) › Ack	Version 2.1
DisplayPort Enter Mode (Mode=1)	Version 2.1
DisplayPort Enter Mode Ack	Version 2.1
DisplayPort Status Update (DFP_D connected, Not Enabled) › Ack (UFP_D connected, Not Enabled, HPD High)	Version 2.1
DisplayPort Status Update (DFP_D connected, Not Enabled)	Version 2.1
DisplayPort Status Update Ack (UFP_D connected, Not Enabled, HPD High)	Version 2.1
SOP' DisplayPort Configure (Set Config as DP Sink, C) › Ack	Version 2.1
SOP' DisplayPort Configure (Set Config as DP Sink, C)	Version 2.1
SOP' DisplayPort Configure Ack	Version 2.1
DisplayPort Configure (Set Config as DP Sink, C) › No Response	Version 2.1
DisplayPort Configure (Set Config as DP Sink, C)	Version 2.1

DPAM 2.1 CTS Update - 1

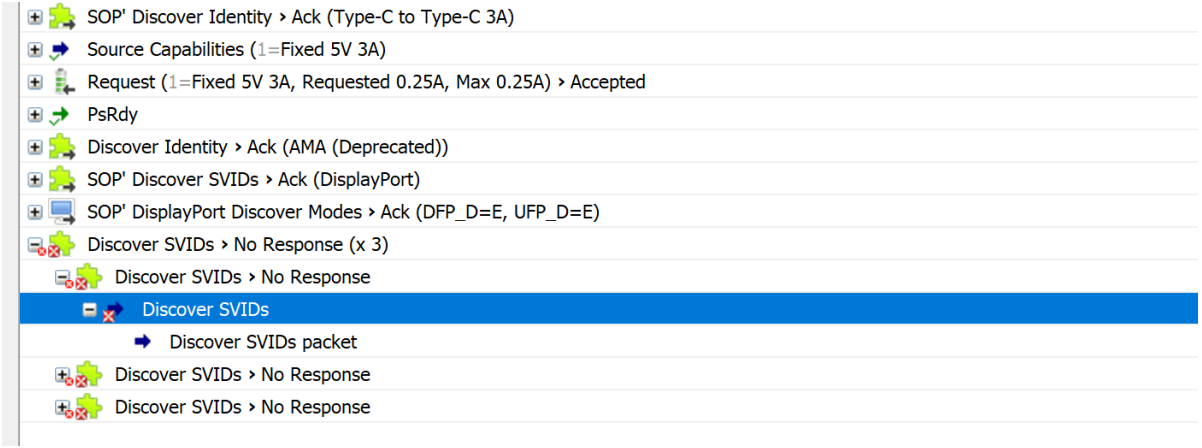
- 10.3.2 DPAM2.1 Entry with USB-C to USB-C non-emarked cable
- 10.3.3 DPAM2.1 Entry with USB-C to USB-C Passive TBT3 cable
- 10.3.4 DPAM2.1 Entry with Passive E-Marked USB-C to USB-C
- 10.3.5 DPAM2.1 Entry with USB-C to USB-C DP2.0 LRD Cable
- 10.3.6 DPAM2.1 Entry with USB-C to USB-C DP2.0 Active Retimer cable
- 10.3.7 DPAM2.1 Entry with USB-C to USB-C DP2.1 LRD cable
- 10.3.8 DPAM2.1 Entry with USB-C to USB-C Active Non-DP cable
- 10.3.9 DPAM2.1 Entry with USB-C to USB-C USB2.0 cable
- 10.3.10 DPAM2.1 Entry with USB-C to DP2.1 cable

- Make sure the DFP_U set correct cable information in DisplayPort Configurations VDO
- 10.3.5 and 10.3.6 Using TBT info is now optional (was mandatory)

DPAM 2.1 CTS Update - 2

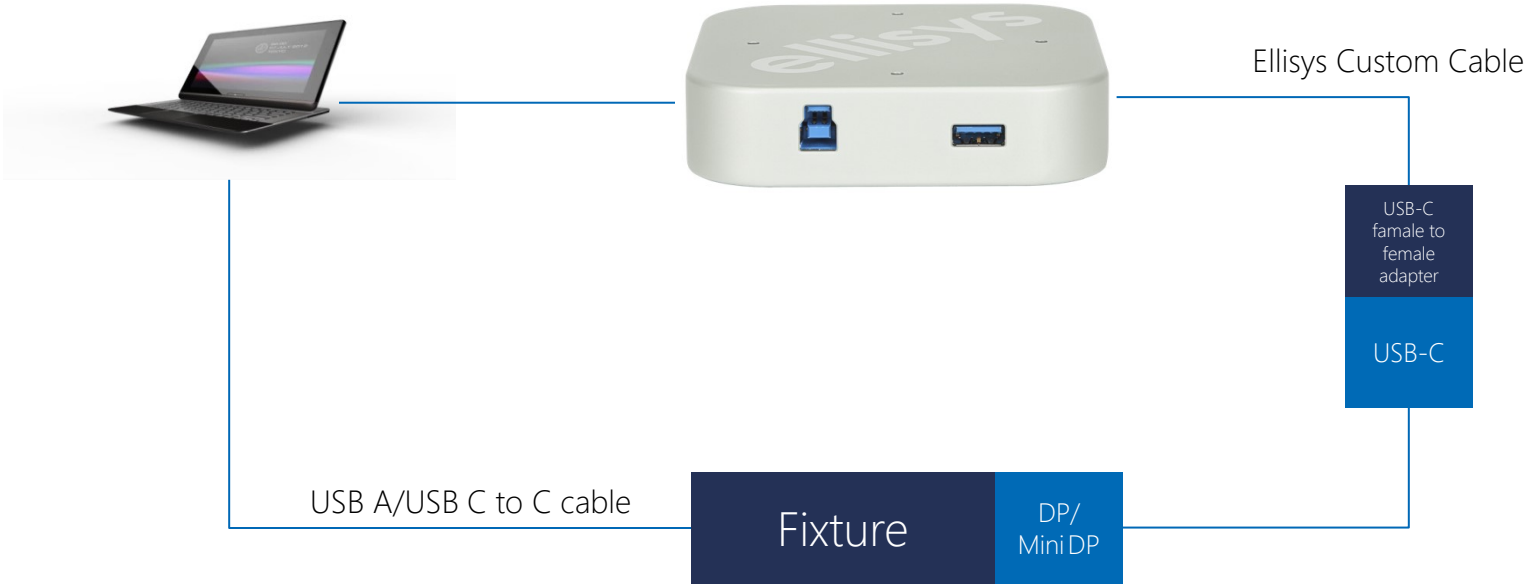
- **DPAM Version Resolution Tests**
  - **10.3.23 DPAM Version 2.1 DFP_U Connected to DPAM Version 2.0 or 2.1 UFP_U**
  - **10.4.3 DPAM Version 2.1 Cable Connected to DPAM Version 2.0 or 2.1 DFP_U**
  - **10.2.8 DPAM Version 2.1 UFP_U Connected to DPAM Version 2.0 or 2.1 DFP_U**

- **10.2.9 DPAM Discovery Interoperability Flow for UFPs**



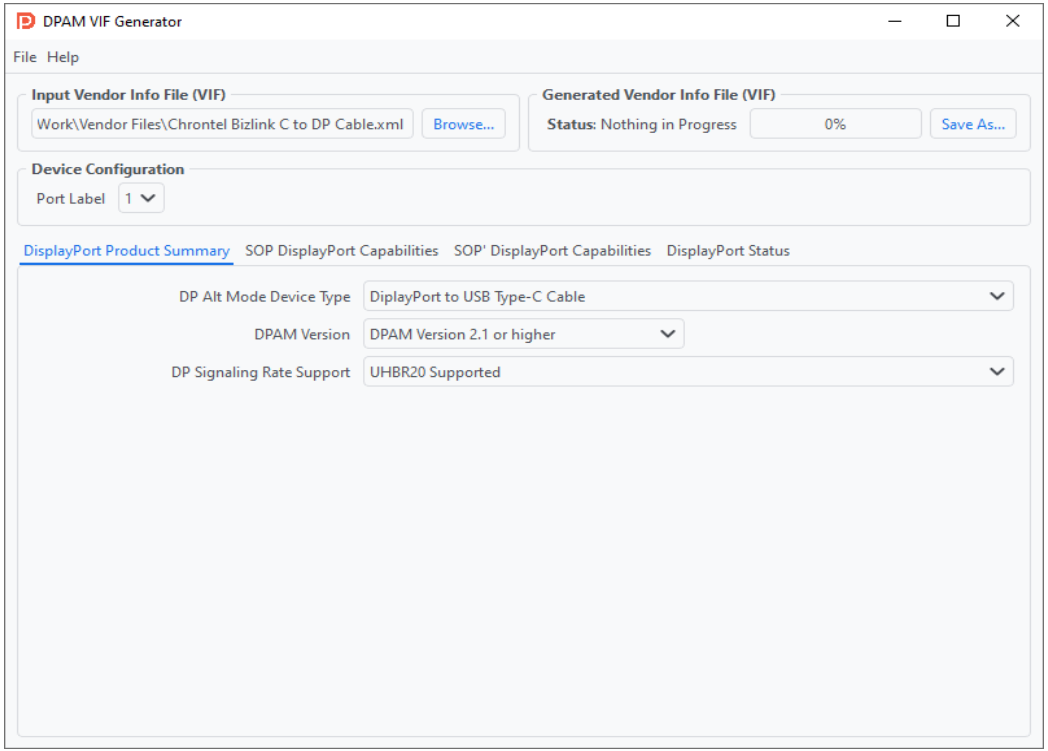
DPAM 2.1 CTS Update - 3

- **C to DP Adapter tests automation**



DPAM 2.1 CTS Update - 4

- **VESA VIF TOOL**



Questions?


DisplayPort over USB-C
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VESA DisplayHDR Specification Overview and Test

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LG Electronics, Inc.
07 Oct 2024

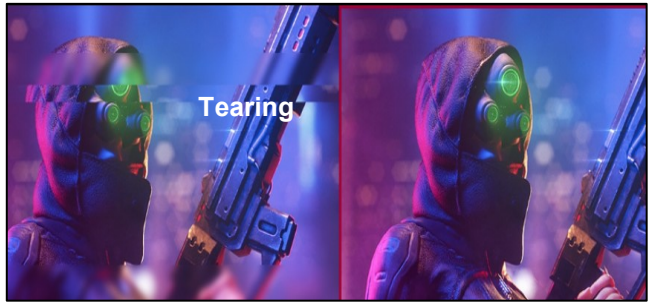
Agenda

- VESA DisplayHDR
- DisplayHDR CTS1.2 Overview
- DisplayHDR CTS1.2 Test

VESA Display Logo

VESA CERTIFIED
DisplayHDR™
Performance for HDR

VESA CERTIFIED
AdaptiveSync
Performance for variable frequency



VESA CERTIFIED
ClearMR
Performance for Motion

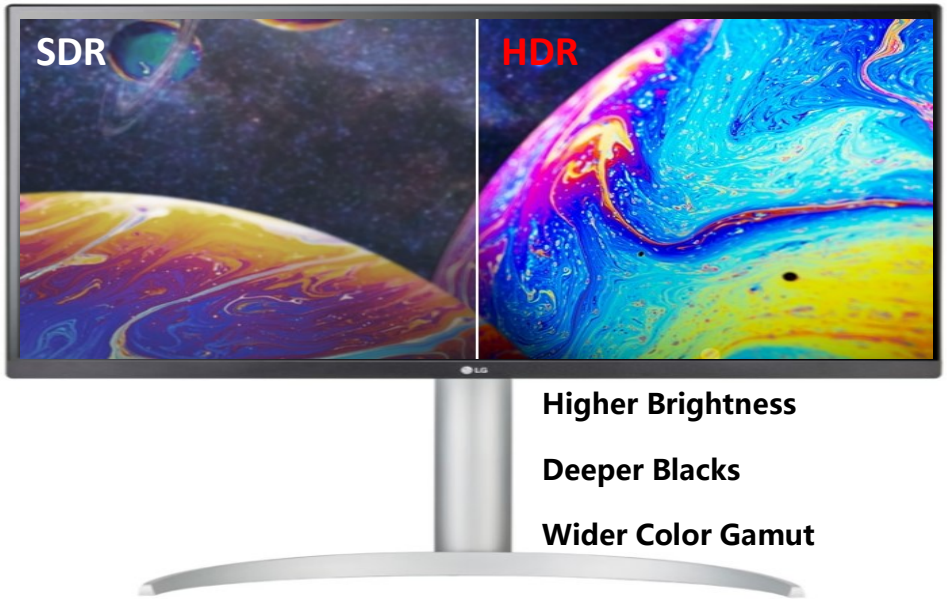
Image Source: https://www.lge.co.kr/

DisplayHDR

High Dynamic Range

- Display Performance Measurement Standard for HDR (Industry)

Image Source: https://www.lge.co.kr/

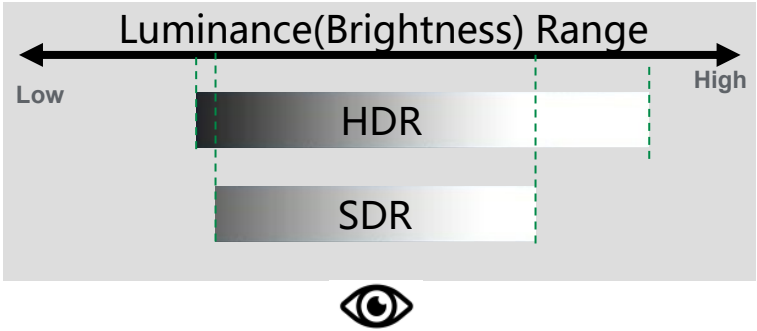


Higher Brightness

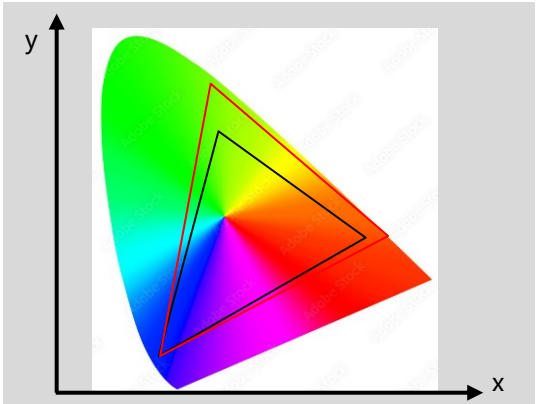
Deeper Blacks

Wider Color Gamut

- Enhanced Brightness and Contrast



- Color Gamut/Space



HDR Main Parameter

Data Byte number	Contents	Group
Data Byte 3	display_primaries_x[0], LSB	1
Data Byte 4	display_primaries_x[0], MSB	
Data Byte 5	display_primaries_y[0], LSB	
Data Byte 6	display_primaries_y[0], MSB	
Data Byte 7	display_primaries_x[1], LSB	
Data Byte 8	display_primaries_x[1], MSB	
Data Byte 9	display_primaries_y[1], LSB	
Data Byte 10	display_primaries_y[1], MSB	
Data Byte11	display_primaries_x[2], LSB	
Data Byte 12	display_primaries_x[2], MSB	
Data Byte 13	display_primaries_y[2], LSB	
Data Byte 14	display_primaries_y[2], MSB	
Data Byte 15	white_point_x, LSB	2
Data Byte 16	white_point_x, MSB	
Data Byte 17	white_point_y, LSB	
Data Byte 18	white_point_y, MSB	
Data Byte 19	max_display_mastering_luminance, LSB	3
Data Byte 20	max_display_mastering_luminance, MSB	
Data Byte 21	min_display_mastering_luminance, LSB	4
Data Byte 22	min_display_mastering_luminance, MSB	
Data Byte 23	Maximum Content Light Level, LSB	5
Data Byte 24	Maximum Content Light Level, MSB	
Data Byte 25	Maximum Frame-average Light Level, LSB	6
Data Byte 26	Maximum Frame-average Light Level, MSB	

HDR Static Metadata Descriptor Type 1(CTA-861)

ST.2086 Container(HDR10)

Mastering Luminance
: Maximum and Minimum Luminance of a 10% Patch Used in Mastering Display

MaxCLL
: Maximum Luminance Level per Single Pixel

MaxFall
: Average Value of All Pixel Values in a Single Frame

Tone Mapping

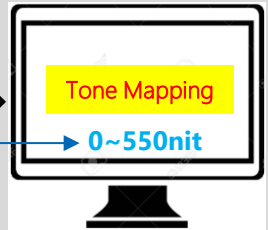
Sink Tone Mapping

Editing from Master Display

Video Stream
0~4000nit

Source

Video Stream
0~4000nit



Sink

No information about Display Luminance

Source Tone Mapping

Editing from Master Display

Video Stream
0~4000nit

Source

Video Stream
0~550nit

Sink

Reading Sink Display Information from EDID
0~550nit

HDR Rendering

Original Scene → Camera → Editing from Master Display → Source → Sink

The original creator determines the values
for HDR Main Parameter value during video editing.

- **Movies, Dramas**: The creator determines the color tones of characters and Master Luminance through a Master Display

- **Games, PC OS:** Metadata is generated directly from the source

DisplayHDR CTS

- Logo/Tier

Ex) #1

VESA CERTIFIED DisplayHDR™

Ex) #2

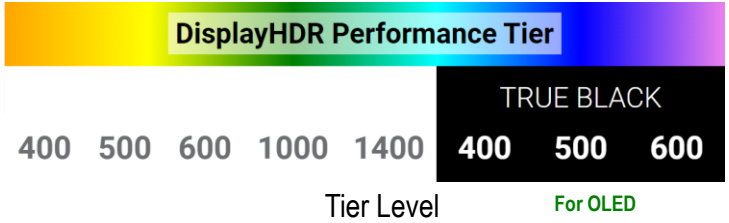
VESA CERTIFIED DisplayHDR™ 400

Tier Level

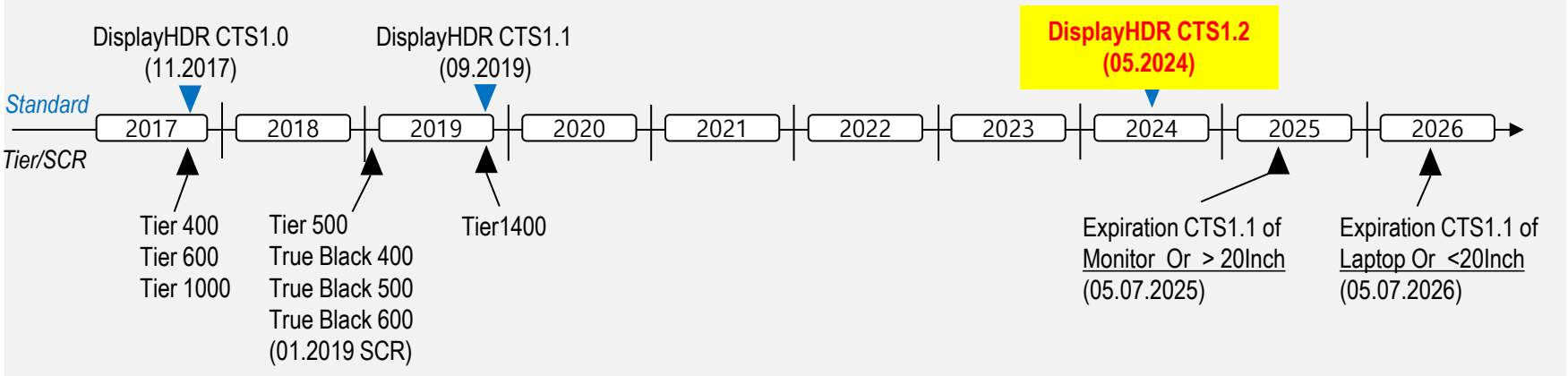
Ex) #3

VESA CERTIFIED DisplayHDR™ TRUE BLACK 400

Tier Level



- History



Certificated Products(09.2024)

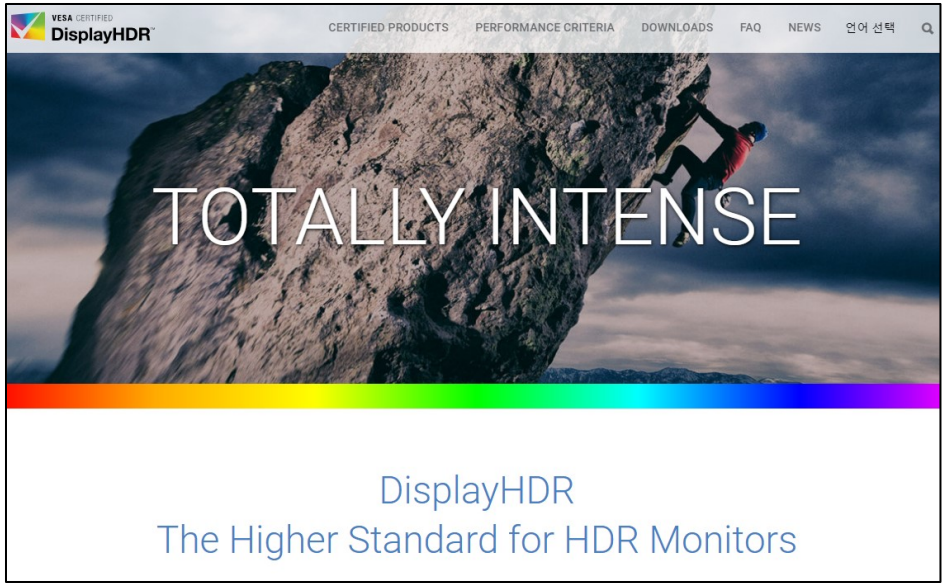
Reference date

(2024. 9)

Tier	Number
DisplayHDR 400	714
DisplayHDR 500	18
DisplayHDR 600	101
DisplayHDR 1000	126
DisplayHDR 1400	12
DisplayHDR True Black 400	89
DisplayHDR True Black 500	194
DisplayHDR True Black 600	65

Including Family models, 3000 display have been certified to the DisplayHDR standard

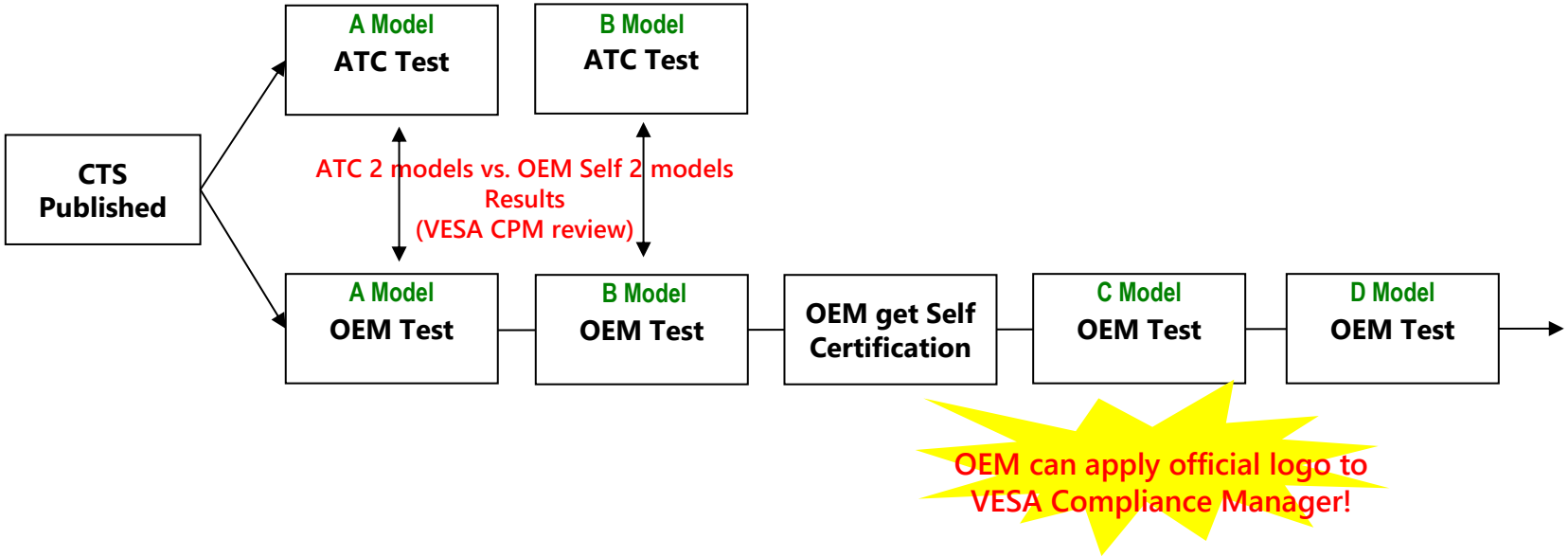
Excluding Family models



https://displayhdr.org/

Self Certification

- Compared the ATC and OEM Self-Test results for two models. If the OEM results for both models match the ATC results, the OEM can get Self Certification from the VESA Compliance Project Manager(CPM)

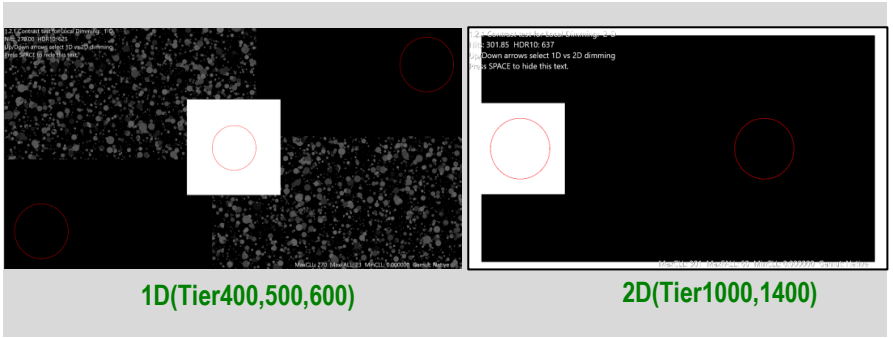


Agenda

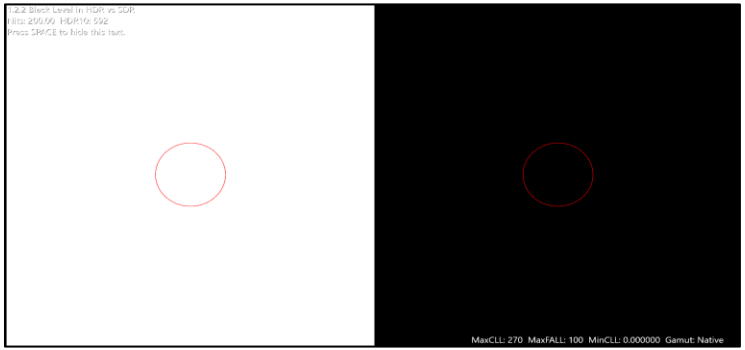
- HDR Technology
- DisplayHDR CTS1.2 Overview
- DisplayHDR CTS1.2 Test

New Tests

- Static contrast ratio

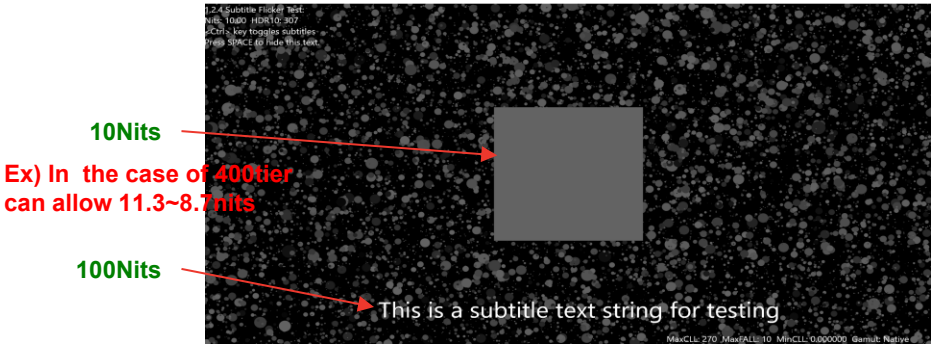


- HDR vs. SDR Black Level



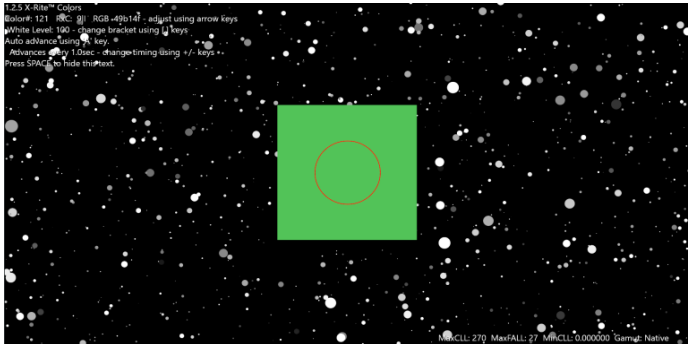
- Black Crush

- Subtitle flicker



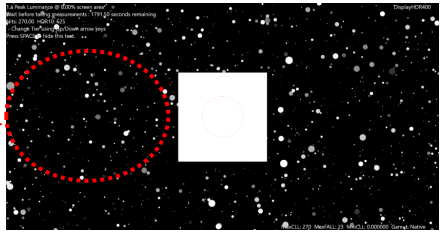
New Tests

- Xrite Color Square



Enhanced requirements

- Luminance
  - Added Noise Pattern



  - Tighter performance of White Point Accuracy and Added Noise Pattern

Test/Specification			DisplayHDR Tier					DisplayHDR True Black		
			400	500	600	1000	1400	400	500	600
White Point Accuracy (Added Noise Pattern)	Delta-ITP Error	≤ 5cd/m2	20	20	20	20	20	20	20	20
		15 cd/m2	~~10~~→15	~~10~~→15	~~10~~→15	~~10~~→15	~~10~~→15	~~10~~→15	~~10~~→15	~~10~~→15
		50,100, 200 cd/m2 50%, 100% tier level	10	10	10	10	10	10	10	10

- Color gamut - Tighter performance

Test/Specification		DisplayHDR Tier					DisplayHDR True Black		
		400	500	600	1000	1400	400	500	600
Color Gamut	ITU-R BT.709 - 10% and Full screen	~~95~~→99%	99%	99%	99%	99%	99%	99%	99%
	DCI-P3 CIE D65 - 10% and Full screen	90%	~~90~~→95%	~~90~~→95%	~~90~~→95%	~~90~~→95%	~~90~~→95%	~~90~~→95%	~~90~~→95%

Enhanced requirements

- Bit depth - Tighter performance and Added Noise Pattern

Test/Specification			DisplayHDR Tier					DisplayHDR True Black		
			400	500	600	1000	1400	400	500	600
White Point Accuracy (Added Noise Pattern)	Delta-ITP Error	≤ 5cd/m2	20	20	20	20	20	20	20	20
		15 cd/m2	~~10→15~~	~~10→15~~	~~10→15~~	~~10→15~~	~~10→15~~	~~10→15~~	~~10→15~~	~~10→15~~
		50,100, 200 cd/m2 50%, 100% tier level	10	10	10	10	10	10	10	10

DisplayHDR CTS1.2 Spec

Blue : Changed to CTS1.2

Red : Added to CTS1.2

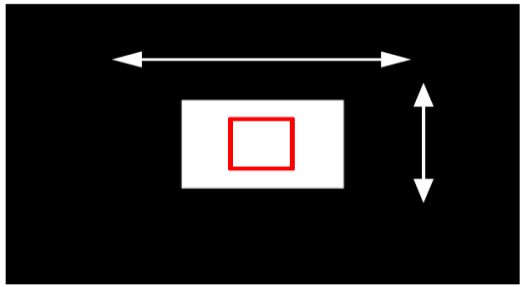
Test/Specification			DisplayHDR Tier					DisplayHDR True Black		
			400	500	600	1000	1400	400	500	600
Minimum White Luminance (Added Noise Pattern)	10%→8% Center Patch	Min (cd/m2)	400	500	600	1000	1400	400	500	600
		Min –Max Delta	10%	10%	10%	10%	10%	10%	10%	10%
	Full screen Flash Test	Min (cd/m2)	400	500	600	1000	1400	250	300	350
	Full screen Long duration	Min (cd/m2)	320	320	350	600	900	250	300	350
Dual Corner Box	Screen Center	Max (cd/m2)	0.4	0.1	0.1	0.05	0.02	0.0005	0.0005	0.0005
	Both White Corners	Min (cd/m2)	300	375	450	750	1050	300	375	450
Active dimming - CheckerBoard	Log(8%patch white/ 5nit Black)/Log10_2		11	11.6	12	13	13.5	-	-	-
	Log_{10}(8%patch white/ 50nit Black)/Log10_2		12	12.6	13	14	14.5	-	-	-
	CheckerBoard Max EDID Luminance black(White Luminance < 500 cd/m2)		-	-	-	-	-	0.0005	0.0005	0.0005
Color Gamut	ITU-R BT.709 - 10% and Full screen		95→99%	99%	99%	99%	99%	99%	99%	99%
	DCI-P3 CIE D65 - 10% and Full screen		90%	90→95%	90→95%	90→95%	90→95%	90→95%	90→95%	90→95%
	Combined Color Luminance - 10%		400	500	600	1000	1400	400	500	600
	Combined Color Luminance – Full screen		320	320	350	600	900	250	300	350
Minimum Bit-depth	10-bit Video Signal, per Channel		✓	✓	✓	✓	✓	✓	✓	✓
	Temporal or Spatial Dithering		8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC
	Minimum 8-bit Digital-to-analog		✓	✓	✓	✓	✓	✓	✓	✓
	Backlight Control 8-bit Accuracy		✓	✓	✓	✓	✓	✓	✓	✓
Rise-time	60Hz Luminance 10%→90% Response Time		8 Frame	8 Frame	8 Frame	8 Frame	8 Frame	2 Frame	2 Frame	2 Frame

DisplayHDR CTS1.2 Spec

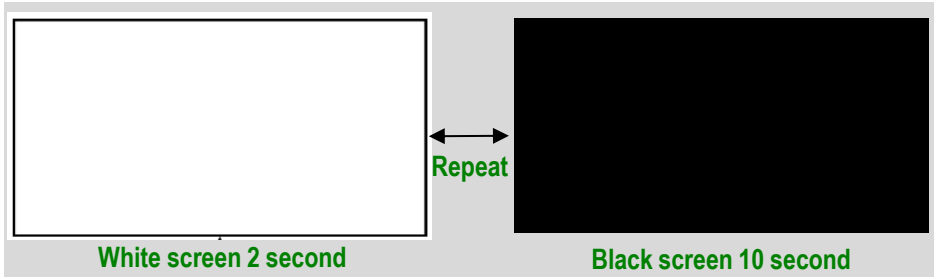
Blue : Changed to CTS1.2

Test/Specification			DisplayHDR Tier					DisplayHDR True Black		
			400	500	600	1000	1400	400	500	600
White Point Accuracy (Added Noise Pattern)	Delta-ITP Error	≤ 5cd/m2	20	20	20	20	20	20	20	20
		15 cd/m2	~~10~~→15	~~10~~→15	~~10~~→15	~~10~~→15	~~10~~→15	~~10~~→15	~~10~~→15	~~10~~→15
		50,100, 200 cd/m2 50%, 100% tier level	10	10	10	10	10	10	10	10
Static Contrast Ratio	1D Test Pattern		1300:1	7000:1	8000:1	-	-	1300:1	7000:1	8000:1
	2D Test Pattern		-	-	-	30K:1	50K:1			
Black HDR vs SDR	HDR Contrast Ratio>SDR Contrast Ratio x 0.9 (If the SDR CR value is higher than the Static Contrast Ratio Requirement, it passes)		>90%	>90%	>90%	>90%	>90%	>90%	>90%	>90%
Black Level Crush	Numbers of distinct shadow level		5	5	5	5	5	5	5	5
Subtitle Flicker	The 10 cd/m² Box luminance depending on subtitle On/Off		13%	13%	13%	10%	10%	10%	10%	10%
X-Rite Color 96 Delta-TP	50 cd/m2		8	8	8	6	6	8	8	8
	100 cd/m2		8	8	8	6	6	8	8	8
	50% Luminance of DisplayHDR Logo Tier		8	8	8	6	6	8	8	8

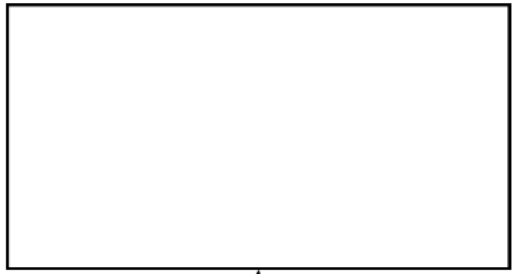
DisplayHDR1.1 Test Pattern



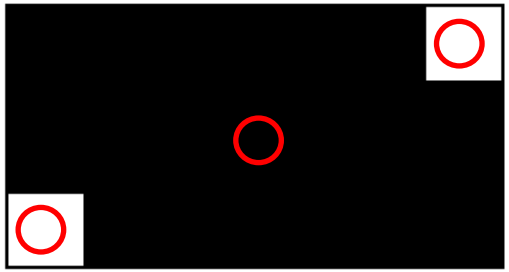
10% Center patch



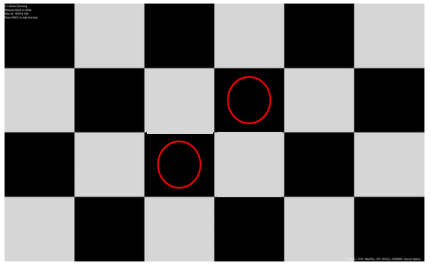
Full-screen Flash Test



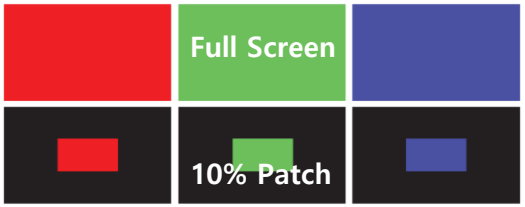
Full-screen Long-duration Test



Dual Corner Box

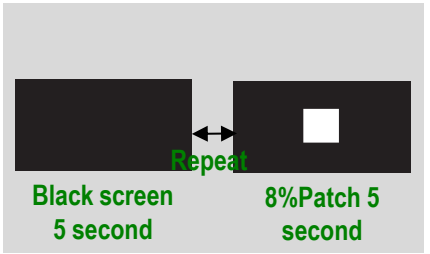


Checker board



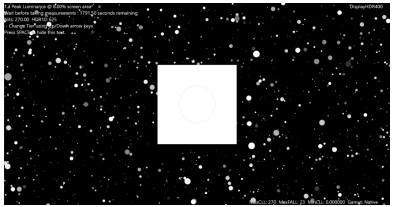
Color Gamut

Delta-ITP

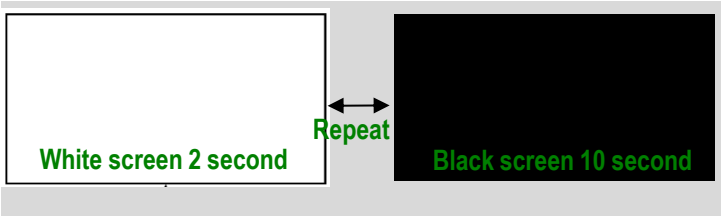


Rise-time Sequence

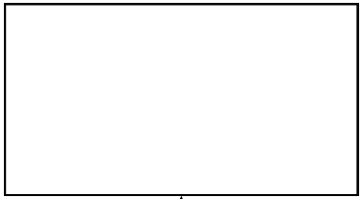
DisplayHDR1.2 Test Pattern



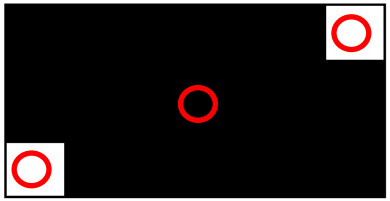
8% Patch



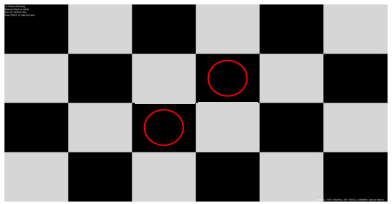
Full-screen Flash



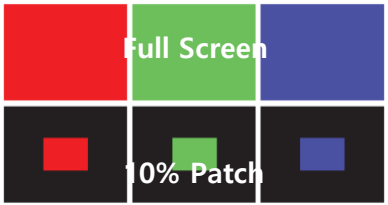
Full-screen Long-duration



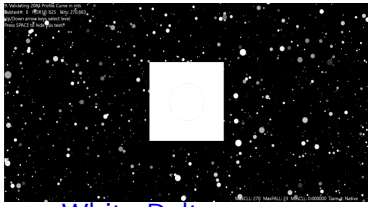
Dual Corner



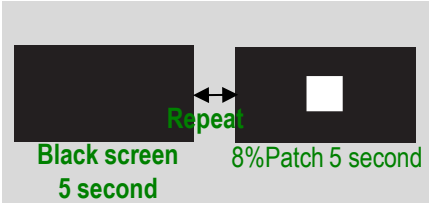
Checker board



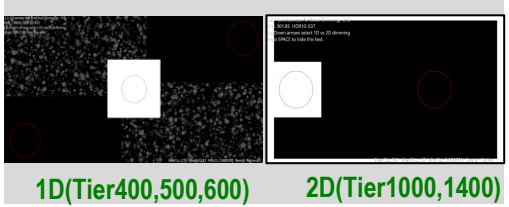
Color Gamut



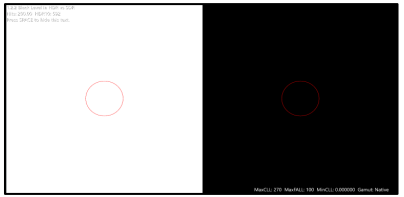
White Delta accuracy



Rise-time Sequence

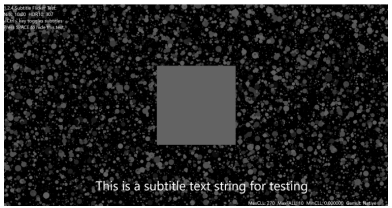


Static Contrast Ratio

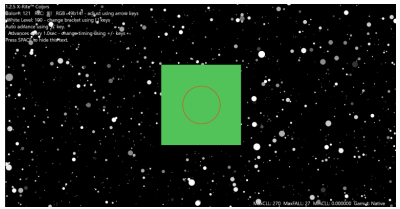


HDR vs. SDR Black Level Test

Black Level Crush



Subtitle Flicker



Color patch

Black : CTS1.1
Blue : Changed to CTS1.2
Red : Added to CTS1.2

Agenda

- HDR Technology
- DisplayHDR CTS1.2 Overview
- DisplayHDR CTS1.2 Test

Test Environment

- Colormeter
  - Black Level Luminance Range
    - DisplayHDR → 0.05 to 4 cd/m2 ± 4%
    - DisplayHDR True Black → 0.0005 to 4 cd/m2 ± 4%
  - White Level Luminance Range → 400 to 1,400+ cd/m2 ± 2%
  - Color accuracy – 0.003 x, y

Certification Level	Manufacturer (Family)	Model Numbers
DisplayHDR	Konica-Minolta™	CA-310[a], CA-410 family of products, CA-P427, CA-VP427, and CS-2000
	Photo Research SpectraDuo®	PR-670 and PR-680
	Gamma Scientific	GS-1220
	Topcon TechnoHouse	SR-UL1R
DisplayHDR **True Black**[b]	Konica-Minolta	CS-2000A, CS-3000, and CS-3000HDR
	Photo Research SpectraDuo®	PR-680 and PR-680L
	Photo Research SpectraScan®	PR-740, PR-745, PR-788, and PR-1050
	Topcon TechnoHouse	SR-UL2

CA-VP427

CA-2000A

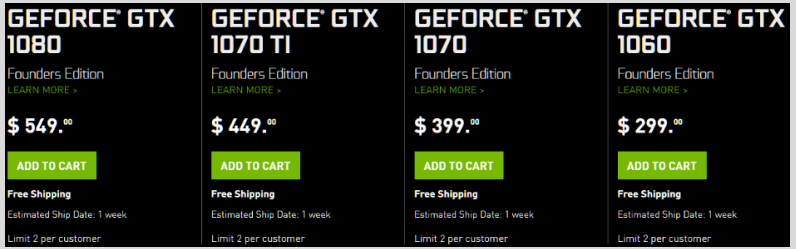
Test Environment

- CTS Test Tool for H/W,S/W requirement
  - Hardware(Minimum requirements)
    - Intel®
      - 7th Generation Core™ processors or later, with 620 graphics or higher
    - AMD®
      - Radeon Rx 5xx series and Radeon Rx Vega or later
    - NVIDIA®
      - GeForce GTX 10-Series graphics cards or later
  - Software
    - Windows 11

      Changed in the CTS1.2

AMD RX 5xx

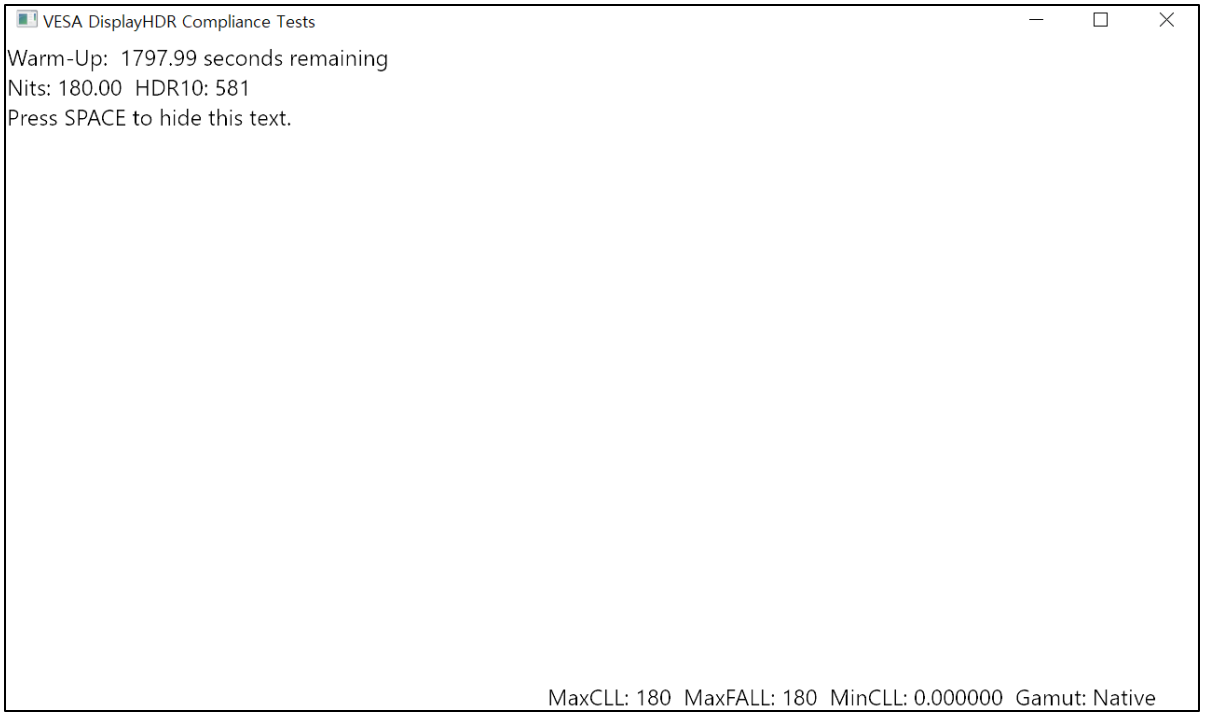
Intel® 7th



NVIDIA® GeForce GTX 10-Series

Measurement setting

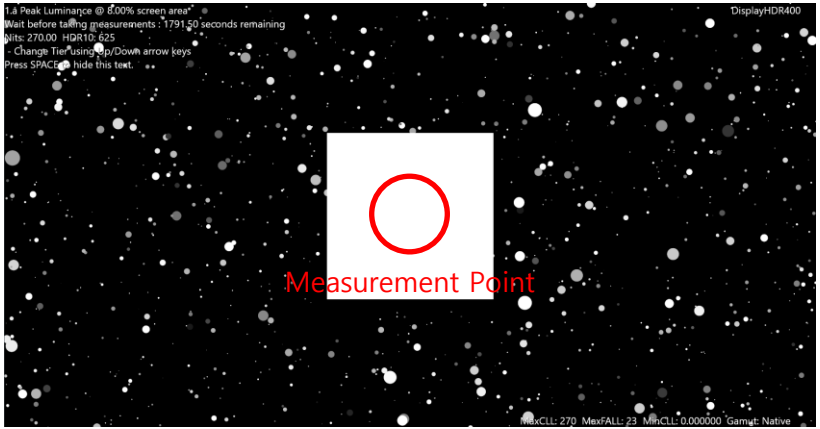
- Warm-Up 30minutes
  - Luminance : 180nit (PQ-Code value : 581)



8% Center Patch Noise Pattern

Section5.1.1

- Test Pattern Information
  - White : 8% APL[1)] center square at MaxLuminance pixel value.
  - Background : 2% APL of the DisplayHDR performance tier APL
    - Max Luminance of Noise Patterns is 100 cd/m2
- How to Measure
  - Black screen for a 1-minute cool-down reset(C key)
  - Luminance is measured at the screen's center once per minute for 30 minutes
    - First measurement shall be obtained within 5 seconds
- Specifications



8% Center Patch

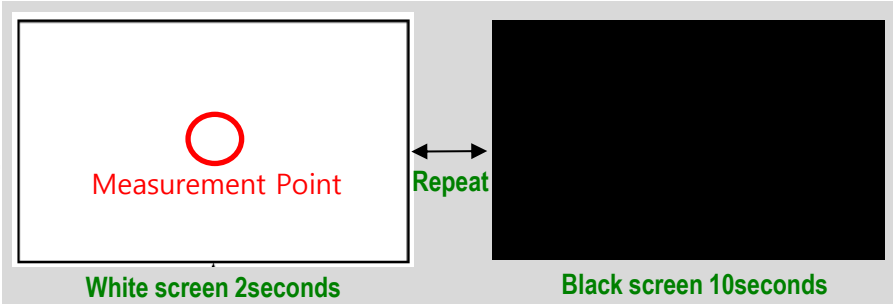
Test/Specification			DisplayHDR Tier					DisplayHDR True Black		
			400	500	600	1000	1400	400	500	600
Minimum White Luminance	8% Center Patch	Min (cd/m2)	400	500	600	1000	1400	400	500	600
		Delta of Max/Min Luminance	10%	10%	10%	10%	10%	10%	10%	10%

1) APL : Average Picture Level

Full-screen Flash Test

Section5.1.2

- Test Pattern Information
  - White : EDID Max Luminance value
  - White Screen 2seconds→Black Screen 10seconds(Repeat)
- How to Measure
  - Black screen for a 1-minute cool-down reset(C key)
  - Luminance is measured at the screen's center once per iteration, for five iterations
- Specifications



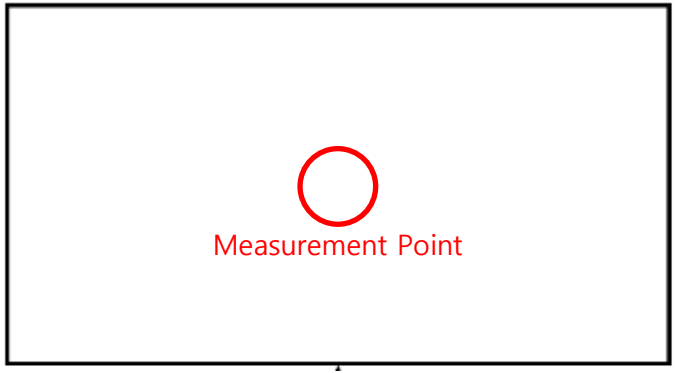
Full-screen Flash Test

Test/Specification			DisplayHDR Tier					DisplayHDR True Black		
			400	500	600	1000	1400	400	500	600
Minimum White Luminance	Full screen Flash Test	Min (cd/m2)	400	500	600	1000	1400	250	300	350

Full-screen Long-duration Test

Section5.1.3

- Test Pattern Information
  - White : EDID Max Luminance value
- How to Measure
  - Black screen for a 1-minute cool-down reset(C key)
  - Luminance is measured at the screen's center once per minute for 30 minutes
    - First measurement shall be obtained within 5 seconds
- Specifications



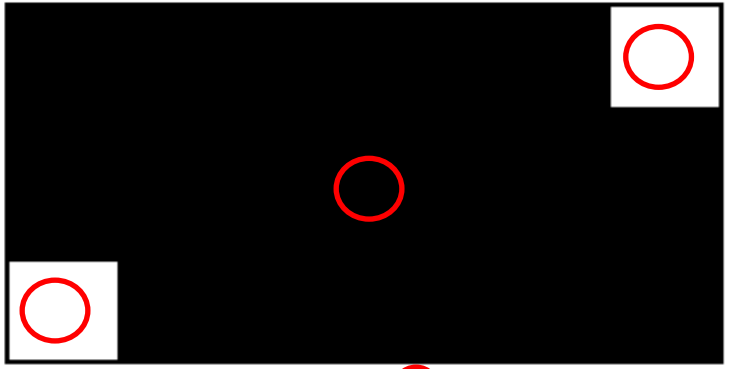
Full screen Long duration

Test/Specification			DisplayHDR Tier					DisplayHDR True Black		
			400	500	600	1000	1400	400	500	600
Minimum White Luminance	Full screen Long duration	Min (cd/m2)	320	320	350	600	900	250	300	350

VESA
Section5.2.1

Dual Corner Box

- Test Pattern Information
  - White : 5% corner squares use the MaxLuminance value
- How to Measure
  - Black screen for a 1-minute cool-down reset(C key)
  - Luminance is measured at the screen's center and both white corner squares
    - Measurements shall be obtained within 10 seconds
- Specifications



Dual Corner Box Measurement Point

Test/Specification			DisplayHDR Tier					DisplayHDR True Black		
			400	500	600	1000	1400	400	500	600
Dual Corner Box	Screen Center	Max (cd/m2)	0.4	0.1	0.1	0.05	0.02	0.0005	0.0005	0.0005
	Both White Corners	Min (cd/m2)	300	375	450	750	1050	300	375	450

Checkerboard(1/2)

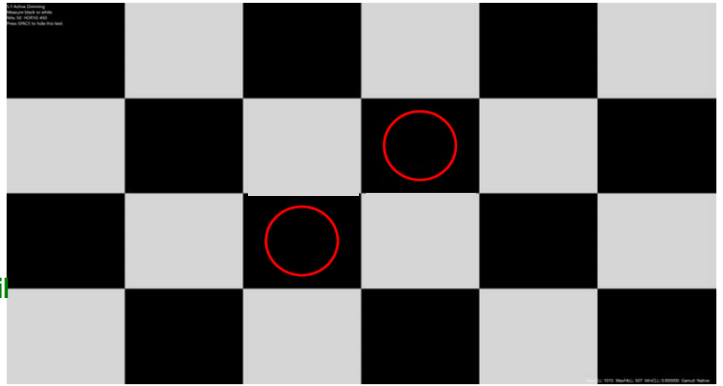
VESA
Section5.2.2

- Test Pattern Information
  - DisplayHDR
    - White : 5cd/m2 – EOTF code value : 253
    - White : 50cd/m2 – EOTF code value : 450

Continue to Adjust the input code values until the average of the white center squares greater than or equal to 5 cd/m2, 50 cd/m2

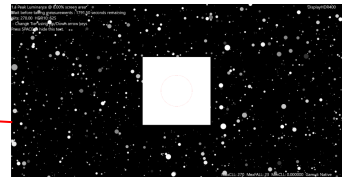
  - DisplayHDR True Black
    - EDID Max Luminance white Or White Luminance < 500 cd/m2

If found to exceed 500 cd/m2, the applied digital code value shall be reduced until the luminance is just above 500 cd/m2



Checker board Measurement Point

- How to Measure
  - Black screen for a 1-minute cool-down reset(C key)
  - Luminance is measured at the screen's average of two center black squares
    - Each of the four measurements on each Checkerboard luminance test shall be measured within 10 seconds



White 8% patch 30 times measured average value

8% Center patch

- Specifications
  - DisplayHDR Tier : Active Dimming = Log_{10} (MaximumWhite / average (Black1, Black2)) / $Log_{10}2$
  - DisplayHDR True Black Tier: 0.0005 ≥ Black Area 2Point Average

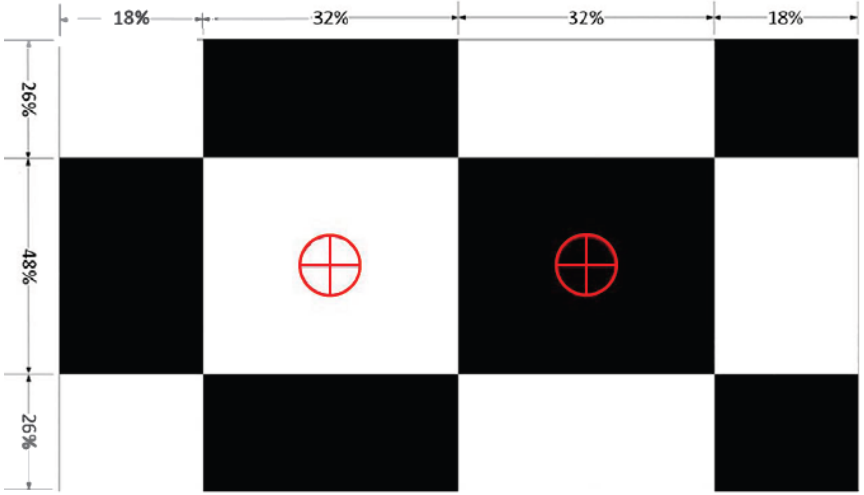
Test/Specification		DisplayHDR Tier					DisplayHDR True Black		
		400	500	600	1000	1400	400	500	600
Active dimming - CheckerBoard	Log_{10}(8%patch white/ 5nit Black)/$Log_{10}2$	11	11.6	12	13	13.5	-	-	-
	Log_{10}(8%patch white/ 50nit Black)/$Log_{10}2$	12	12.6	13	14	14.5	-	-	-
	Black of CheckerBoard EDID Max white Luminance (Or White Luminance < 500 cd/m2)	-	-	-	-	-	0.0005	0.0005	0.0005

Checkerboard(2/2)

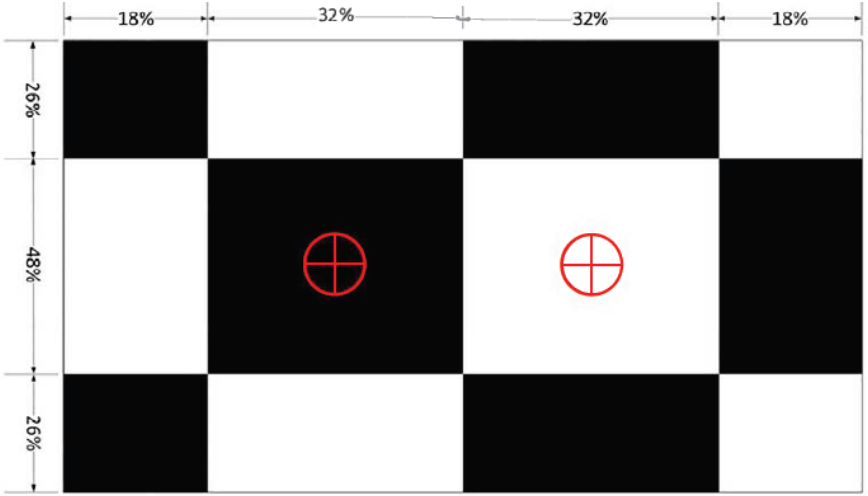
VESA
Section5.2.2

- In case of Panel Size < 20Inch, Possible to test the 4 × 3 checkerboard
  - When the 4 × 3 checkerboard test, this Specification mandates that this test records the Black/White luminance of the Black/White check near the center(Both patterns)

For more details, Please see DisplayHDR1.2 Spec.



Measurement Point



Measurement Point

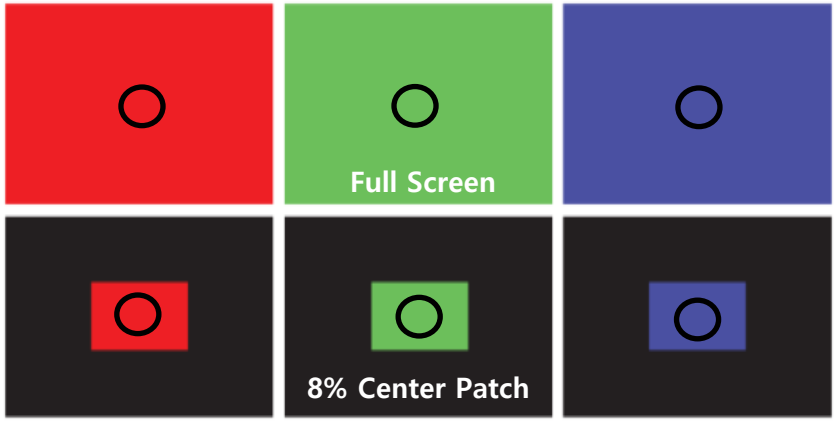
- Test Result Form

5.2.2	5.x	Checkerboard tests			Top White	Bottom White	Top Black	Bottom Black	Screen Size	Test Type
	N/A	N/A - No 50cd/m2 or 5 cd/m2 test for TrueBlack							10	4x3 Pattern
		N/A - No 50cd/m2 or 5 cd/m2 Test for TrueBlack	N/A	N/A	N/A					6x4 Pattern
	5.2	Full Luminance Checkerboard or >=500 for TrueBlac			0	0	0	0		4x3 Pattern

VESA
Section6

Color Gamut(1/2)

- Test Pattern Information
  - MaxLuminance and RGB primary color values in the DisplayID (or legacy EDID)
  - Six separate tests(Red, Green, and Blue)
    - Full-screen
    - 8% center square
- How to Measure
  - CIE 1931 x, y, Y values are measured at the screen's center
- Specifications
  - Color gamut shall be calculated for actual coverage of the target gamut
  - The Red, Green, and Blue luminance sum for each 8% center square and full-screen color test shall meet or exceed the white-level luminance specifications



Color Gamut

Measurement Point

Test/Specification		DisplayHDR Tier					DisplayHDR True Black		
		400	500	600	1000	1400	400	500	600
Color Gamut	ITU-R BT.709 - 10% and Full screen	99%	99%	99%	99%	99%	99%	99%	99%
	DCI-P3 CIE D65 - 10% and Full screen	90%	95%	95%	95%	95%	95%	95%	95%
	Combined Color Luminance - 10%	400	500	600	1000	1400	400	500	600
	Combined Color Luminance – Full screen	320	320	350	600	900	250	300	350

Color Gamut(2/2)

Section6

- Test Result Form(e.g. DisplayHDR400)

①Enter measurement data

6.1	6a & 6b	Color Gamut & Luminance Test			Luminance	x	y	Luminance	x	y
		Patch Test Size 8% and Full Screen			8% Patch Size Color Test			Full Screen Patch Size Color Test		
		Red			100	0.7	0.3	100	0.7	0.3
		Green			350	0.25	0.65	350	0.25	0.65
		Blue			32	0.15	0.05	32	0.15	0.05
		Calculated EDID Color, u'v'			Luminance	u'	v'	Luminance	u'	v'
		Red				0.53846	0.51923		0.53846	0.51923
		Green			482	0.09709	0.56796	482	0.09709	0.56796
		Blue				0.18182	0.13636		0.18182	0.13636
		8% Patch Color Luminance Sum Requirement	400	Pass						
		sRGB Coverage u'v' for the 8% Patch	99%	Pass	100.00%					
		DCI-P3 Coverage u'v' for the 8% Patch	90%	Pass	97.40%					
		Full Screen Color Luminance Sum Requirement	320	Pass						
		sRGB Coverage u'v' for Full Screen	99%	Pass	100.00%					
		DCI-P3 Coverage u'v' for Full Screen	90%	Pass	97.32%					

Press this button to calculate the color gamut

②Click the Press Button included in the template to check the result.

Bit Depth

- Test Pattern Information
  - Showing five rows across the screen

Row	Description
1	Ramp bar is truncated to 6-bit precision
2	Ramp bar uses native display capability
3	Ramp bar is truncated to 8-bit precision.
4	Ramp bar uses native display capability (same as Row 2)
5	Ramp bar is truncated to 10-bit precision

Bit Depth

- How to Measure
  - Patterns can be distinguished the 6, 8, 10 bit depth

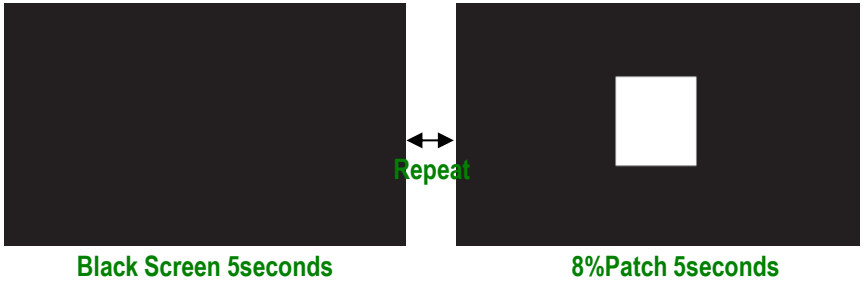
- Specifications

Test/Specification		DisplayHDR Tier					DisplayHDR True Black		
		400	500	600	1000	1400	400	500	600
Minimum Bit-depth	10-bit Video Signal, per Channel	✓	✓	✓	✓	✓	✓	✓	✓
	Temporal or Spatial Dithering	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC
	Minimum 8-bit Digital-to-analog	✓	✓	✓	✓	✓	✓	✓	✓
	Backlight Control 8-bit Accuracy	✓	✓	✓	✓	✓	✓	✓	✓

VESA
Section8

Rise-time

- Test Pattern Information
  - White : 8% APL center square at MaxLuminance pixel value
- How to Measure
  - Rise time is measured from the 10 to 90% luminance levels



- Specifications

Bit Depth

Panel Type	Display Refresh Rate	Maximum Number of Frames for Rise from Black to Maximum Luminance		Time (ms)	
LCD	24	8	Recommended	333	Recommended
	60	8	Mandatory	133	Mandatory
	144	8	Recommended	56	Recommended
	200	8	Recommended	40	Recommended
OLED	60	2	Mandatory	33	Mandatory

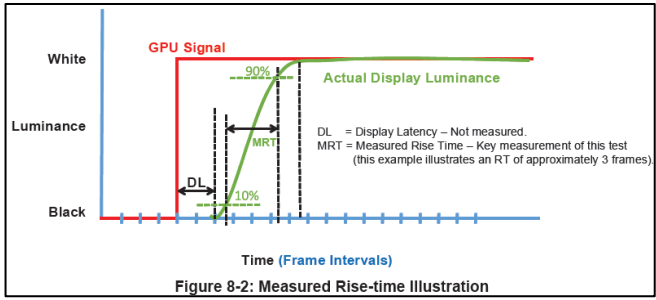


Figure 8-2: Measured Rise-time Illustration

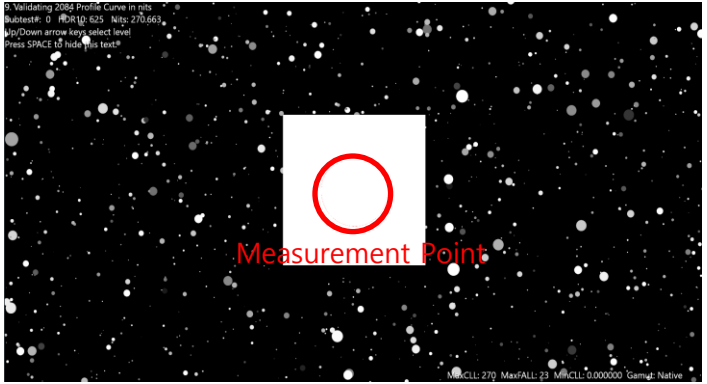
Luminance and White Point Accuracy

Section9

- Test Pattern Information
  - White : Center square comprising 8% of the screen's area
    - Possible to change the 8% of the screen's luminance area
      - 1.0509, 5.172, 14.958, 50.825, 100.23, 199.15 cd/m2
      - 50% of DisplayHDR Tier
      - 100% of DisplayHDR Tier - Least three 10-bit code values below the tier

To avoid testing displays at what may potentially be their absolute limit of luminance

  - Background : Max Luminance of Noise Patterns is 100 cd/m2
    - Limiting 2% APL of the DisplayHDR performance tier



White Accuracy Pattern

- How to Measure
  - CIE 1931 x, y, Y values are measured at the screen's center
    - Measurement shall be initiated at the screen's center within 5 seconds
    - The tests shall be measured in sequentially increasing luminance levels

- Specifications

Test/Specification			DisplayHDR Tier					DisplayHDR True Black		
			400	500	600	1000	1400	400	500	600
White Point Accuracy	Delta-ITP Error	≤ 5cd/m2	20	20	20	20	20	20	20	20
		15 cd/m2	15	15	15	15	15	15	15	15
		50,100, 200 cd/m2 50%, 100%[1] tier	10	10	10	10	10	10	10	10

1) Generally, this results in a test luminance level within the range of 95 to 98% of the performance tier rather than a true 100% of the performance tier, but for naming simplicity this is called the 100% level test.

Luminance and White Point Accuracy

Section9

- Test Result Form(e.g. DisplayHDR400)

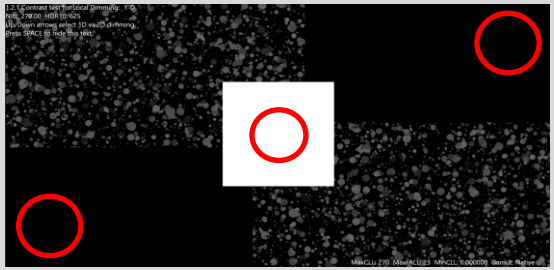
① Enter measurement data (Automatically calculate Delta-ITP)

						Measured		
		Maximum of any sample (8 frames i.e. 133ms at 60H	133	Pass	16			
9		**Delta-ITP**			**Delta-ITP**	x	y	Y
9.3	9.10	Delta-ITP at 1.0509 cd/m2	20	Pass	1.83	0.31271	0.32902	1
	9.11	Delta-ITP at 5.172 cd/m2	20	Pass	1.73	0.31271	0.32902	5
	9.12	Delta-ITP at 14.958 cd/m2	15	Pass	0.17	0.31271	0.32902	15
	9.14	Delta-ITP at 50.825 cd/m2	10	Pass	1.12	0.31271	0.32902	50
	9.16	Delta-ITP at 100.23 cd/m2	10	Pass	0.17	0.31271	0.32902	100
	9.17	Delta-ITP at 199.15 cd/m2	10	Pass	0.32	0.31271	0.32902	200
	9.18/19/24/28	Delta-ITP 50% of Tier: 199.15 cd/m2	10					
	9.21/23/26/32/3	Delta-ITP near Tier: 387.13 cd/m2	10	Pass	0.03	0.31271	0.32902	387

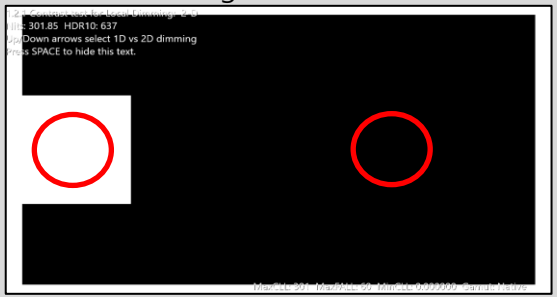
② Check the results

1D and 2D Local Dimming

- Test Pattern Information
  - 1D : DisplayHDR 400, 500, 600 tier(Including True black tier)
    - White : 8% APL center square at MaxLuminance pixel value
    - Background : Upper left, Lower right corners: 30% of Screen size and <10nit Star
  - 2D : DisplayHDR 1000, 1400 tier
    - White : 8% APL left square at MaxLuminance pixel value
    - Background : MaxLuminance on all four sides of the image, 3% of width each
- How to Measure
  - Luminance is measured at the screen's O Points



1D Local Dimming Pattern



2D Local Dimming Pattern

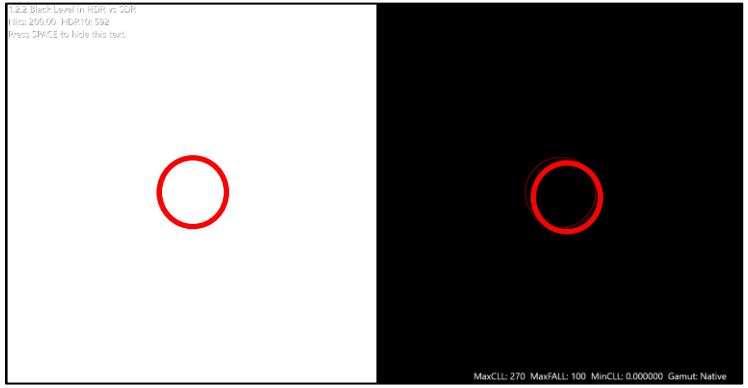
O Measurement Point

- Specifications

Test/Specification		DisplayHDR Tier					DisplayHDR True Black		
		400	500	600	1000	1400	400	500	600
Static Contrast Ratio	1D Pattern	1300:1	7000:1	8000:1	-	-	1300:1	7000:1	8000:1
	2D Pattern	-	-	-	30,000:1	50,000:1			

HDR vs. SDR Black Level Test

- Test Pattern Information
  - White : PQ code value 592(199.15cd/m2)
- How to Measure
  - Check the Contrast Ratio in both SDR and HDR Modes
  - Measure the White O and Black O points and calculate the Contrast Ratio for each mode
- Specifications
  - Verify if $CR_{HDR} \geq CR_{SDR} \times 0.9$
    - If the CR_{SDR} is higher than Ratio of 1D and 2D Local Dimming Test(Section10), it passes



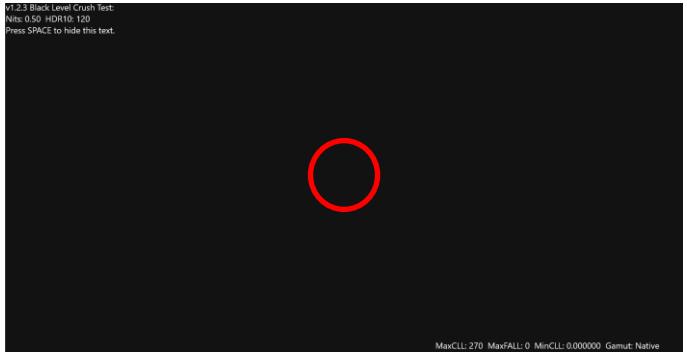
HDR vs. SDR Pattern Measurement Point

Test/Specification		DisplayHDR Tier					DisplayHDR True Black		
		400	500	600	1000	1400	400	500	600
Black HDR vs SDR	HDR Contrast Ratio>SDR Contrast Ratio x 0.9 (If the SDR CR value is higher than the Static Contrast Ratio Requirement, it passes)	>90%	>90%	>90%	>90%	>90%	>90%	>90%	>90%

VESA
Section12

Black Crush Test

- Test Pattern Information
  - 5 types of luminance
    - 0 cd/m2(PQ : 0)
    - 0.05 cd/m2(PQ : 47)
    - 0.1 cd/m(PQ : 64)
    - 0.3 cd/m(PQ : 99)
    - 0.5 cd/m2(PQ : 120)



Black Crush Pattern ○ Measurement Point

- How to Measure
  - If different values are measured at each of the 5 luminance levels, it passes

- Specifications

Test/Specification		DisplayHDR Tier					DisplayHDR True Black		
		400	500	600	1000	1400	400	500	600
Black Level Crush	Required number of distinct shadow levels	5	5	5	5	5	5	5	5

Subtitle Luminance Flicker Test

- Test Pattern Information
  - White
    - APL 8% gray square at 10 cd/m2
    - Subtitle : 100 cd/m2
  - Background : <10nit Stars

Subtitle Luminance Flicker Pattern ○ Measurement Point

- How to Measure
  - Luminance is measured the gray square's minimum and maximum range as the subtitles ON/OFF
    - The CTRL botton can control the subtitles ON/OFF

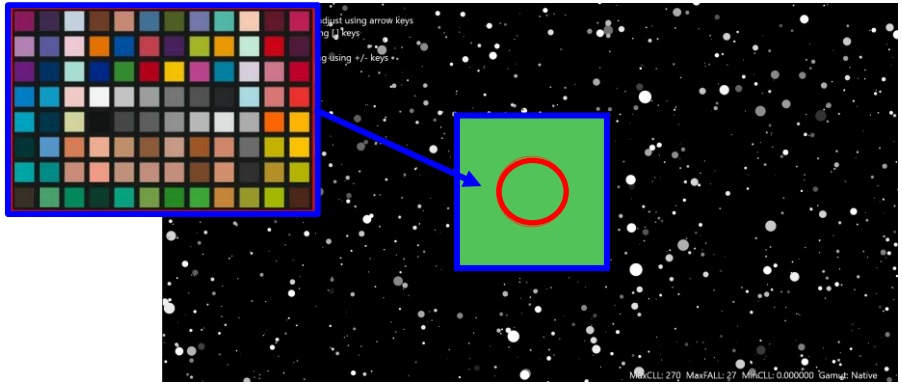
- Specifications
  - Maximum Luminance/ minimum Luminance x100

Test/Specification		DisplayHDR Tier					DisplayHDR True Black		
		400	500	600	1000	1400	400	500	600
Subtitle Flicker	The 10 cd/m^2 Box luminance depending on subtitle On/Off	13%	13%	13%	10%	10%	10%	10%	10%

VESA
Section14

XRite Color Square Test

- Test Pattern Information
  - X-Rite Color 96types of 8% center square
    - The colors are tested at three different luminance levels
      - 50 cd/m2
      - 100 cd/m2
      - 50% of DisplayHDR Compliance Logo level
  - Background : <100nit Stars



XRite Color Square Pattern

Measurement Point

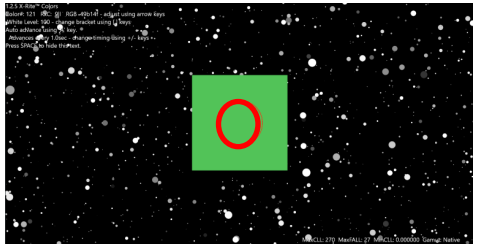
- How to Measure
  - 96 color Delta-TP are measured at the screen's O point
    - Three tests are run, one at each luminance level, and each test includes 96 color test squares
    - This test focuses purely on color, not luminance, and thus uses a Delta-TP, Not Delta-ITP

- Specifications

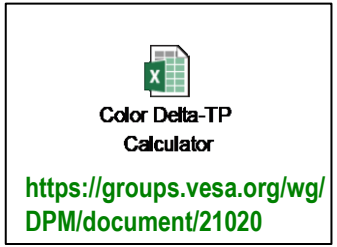
Test/Specification		DisplayHDR Tier					DisplayHDR True Black		
		400	500	600	1000	1400	400	500	600
X-Rite Color 96 Delta-TP	50 cd/m2	8	8	8	6	6	8	8	8
	100 cd/m2	8	8	8	6	6	8	8	8
	50% of DisplayHDR Logo	8	8	8	6	6	8	8	8

XRite Color Square Test

- Test procedure



① Set the luminance levels and Measure the 96 color Delta-TP



② Download and Open the Delta-TP Color Patch Calculator

RGB for Lum Target:		50
R	G	B
0.4315341	0.4322815	0.4301258
0.306711	0.3068675	0.3071609
0.1951589	0.1949144	0.1944453
0.3016082	0.2196962	0.2770536
0.2334271	0.2140811	0.2542263

③ Input the RGB Luminance

Measured Values			Delta-ITP	Delta-TP	Luminance Error
X	Y	Z			
86.172	91.763	98.4	0.99	0.96	-0.3
19.565	20.513	22.632	3.93	0.27	1.3
3.4797	3.6113	4.0109	10.76	1.57	0.9
11.56	7.5736	12.083	20.84	7.52	3.1
6.1162	5.2144	9.9653	15.10	4.24	1.7
57.238	61.038	78.14	6.33	2.47	5.3
8.5755	7.6934	5.019	18.08	0.25	2.9
29.896	27.448	19.722	15.40	1.33	7.3
14.263	14.993	28.79	14.26	1.97	4.0
7.9662	10.23	5.1425	17.19	0.85	3.5
20.756	19.458	38.389	11.44	2.88	3.8
25.899	35.159	38.02	12.90	1.00	7.5
58.248	58.207	46.465	10.05	1.31	8.9
6.7257	5.0673	4.7988	17.95	0.95	2.1
17.223	10.556	9.9451	22.50	6.84	4.6
31.336	26.162	43.964	13.37	3.50	5.9
14.271	12.067	31.279	16.77	3.92	3.9
64.24	61.355	67.237	6.05	1.27	5.5
26.753	21.709	4.5928	23.49	3.76	9.4
10.5	8.6996	31.231	20.04	2.94	3.7
19.87	13.603	9.751	20.62	5.20	5.3
6.3774	4.8422	11.754	18.50	5.37	2.0
24.971	33.479	8.6296	19.62	2.25	11.3
31.476	29.92	5.3272	22.55	1.96	12.1
58.316	69.296	66.575	6.80	1.69	6.7
18.195	10.992	3.9527	23.76	6.54	5.2
5.8153	4.4966	6.8859	17.49	5.26	1.8
10.371	6.4744	20.876	21.82	6.79	3.0
4.9269	4.7471	13.109	19.11	1.83	2.1
49.336	59.235	66	8.94	2.65	7.7
6.016	4.5097	20.759	20.27	2.34	2.2
11.217	17.922	7.6543	17.79	1.68	5.9
14.001	8.3427	3.883	23.23	7.61	3.9
39.034	42.076	6.3153	23.03	1.50	16.8
22.064	14.587	23.892	19.63	5.31	5.3
11.222	14.57	30.392	21.05	3.24	6.0
62.971	64.227	79.454	3.73	2.44	2.7
31.12	25.02	26.447	14.68	2.89	6.2
15.869	9.4934	5.2344	23.73	6.61	4.6
14.889	15.939	46.294	20.64	2.47	6.4
21.398	24.427	49.652	17.56	2.60	7.7
62.238	60.972	58.039	7.07	1.46	6.3
53.973	56.739	62.505	1.68	0.66	1.3
33.789	35.623	39.664	2.74	0.52	1.5
10.219	10.681	11.971	7.65	1.41	1.5
4.6133	4.8259	5.5722	9.06	1.17	0.9
50.718	58.036	74.526	9.37	2.42	8.1

④ Measure each of the 96 colors and Input the X, Y, and Z values

11.88	11.39	4.0919	20.62	3.09	4.7
9.6269	11.872	3.6052	20.78	1.54	4.9
12.171	16.248	3.32	21.40	1.66	6.7
2.4935	2.3018	1.5514	18.71	5.27	1.1

	Delta-ITP	Delta-TP	Lum Error
Average	15.77	2.92	3.25
Maximum	24.18	9.44	9.48

⑤ Check the Delta TP

- Color Delta-TP Calculator_DP1_50nit.xlsx
- Color Delta-TP Calculator_DP1_100nit.xlsx.xlsx
- Color Delta-TP Calculator_DP1_200nit.xlsx
- Color Delta-TP Calculator_HDMI1_50nit.xlsx.xlsx
- Color Delta-TP Calculator_HDMI1_100nit.xlsx
- Color Delta-TP Calculator_HDMI1_200nit.xlsx
- Color Delta-TP Calculator_HDMI2_50nit.xlsx
- Color Delta-TP Calculator_HDMI2_100nit.xlsx
- Color Delta-TP Calculator_HDMI2_200nit.xlsx

⑥ Save the data according to luminance and submit it to the VESA Compliance Manager with Test Result

ClearMR™ *v1.1*

: Specifications and Compliance Testing Overview

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Samsung Display Co. Ltd.

Oct. 7. 2024

ClearMR™

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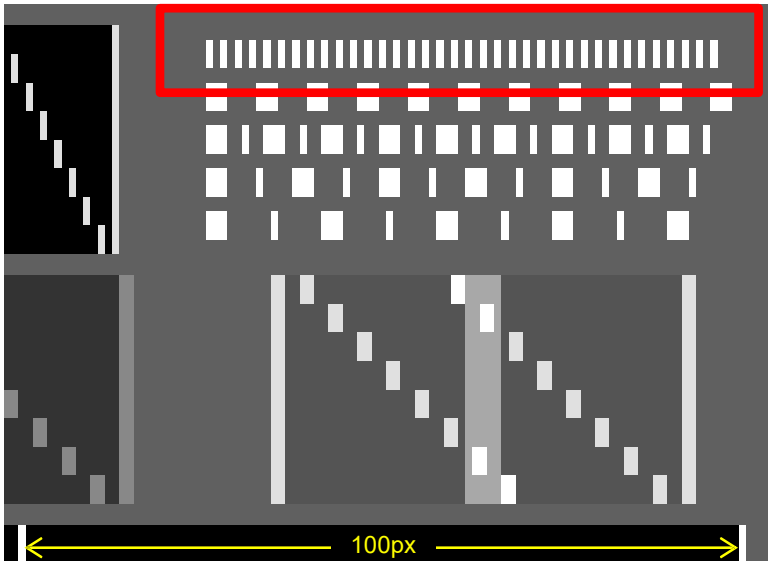
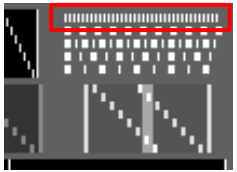
Blur beyond recognition



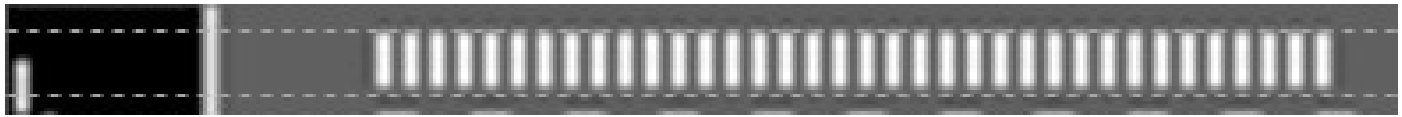
still frame of the actual pattern

motion composite showing blur similar to what humans might see

Blur beyond recognition



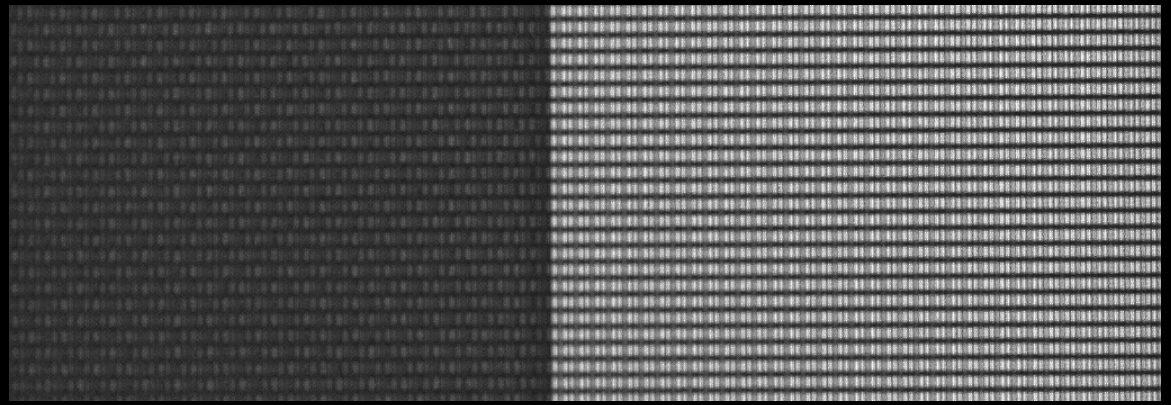
Actually, vertical lines 2 pixels wide, 2 pixels apart



Horizontal lines?

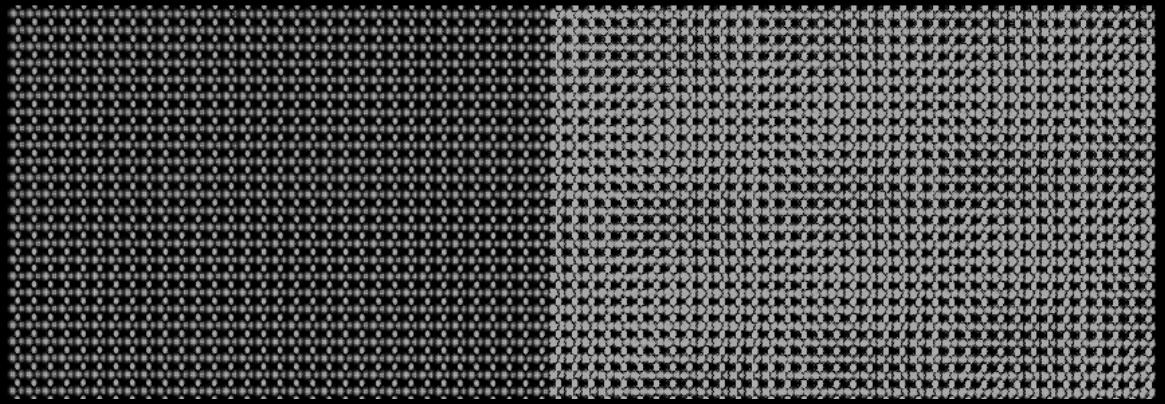
Product A
240Hz

10000 / 240 = 41.67



Product B
175Hz

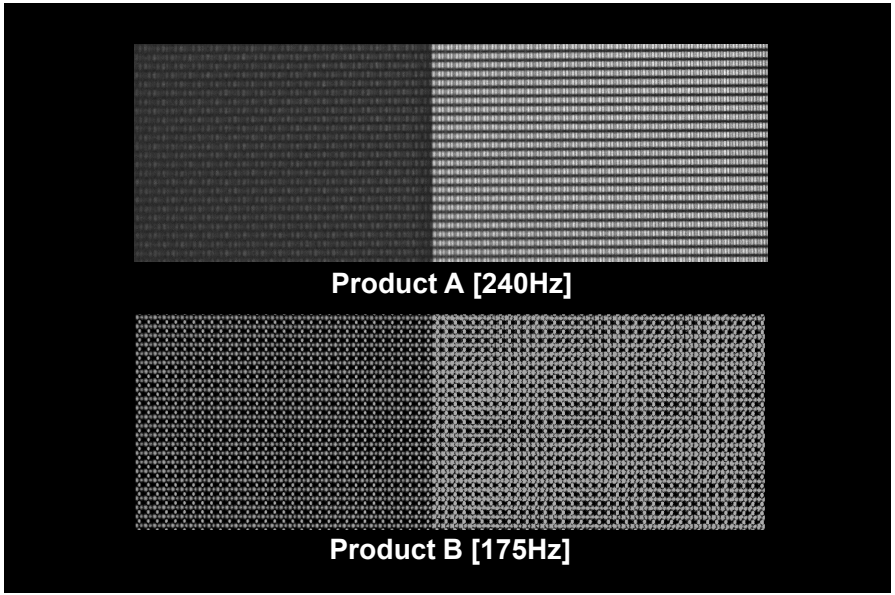
10000 / 175 = 57.14



* 1 frame Captured by High-Speed Camera(10,000 fps)

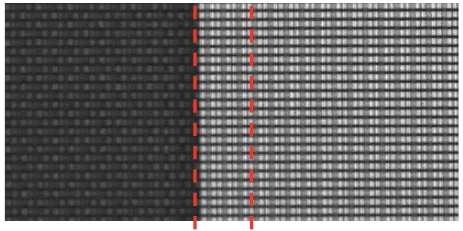
The problem statement

- **How blurry is the picture**
- Is blur by Product A the same as blur by Product B?
- What metric/method is best for quantifying blur?
  - Hertz (Hz)
  - milliseconds (ms)
  - G2G? MPRT?

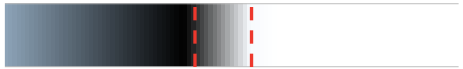


Blur profile

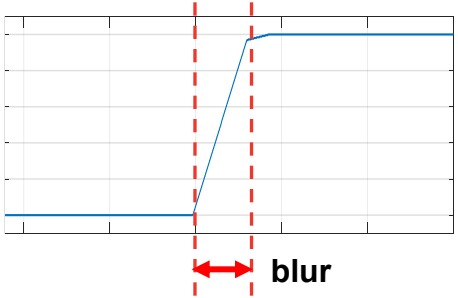
Motion picture



Blur image



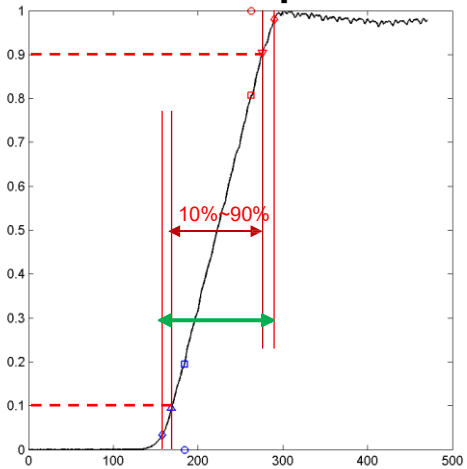
Blur profile



Blur vs. MPRT(Moving Picture Response Time)

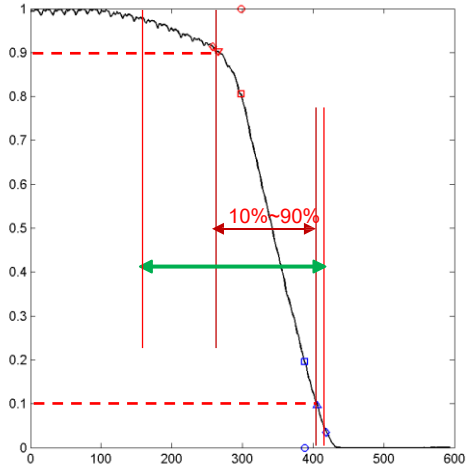
- **MPRT [ms]**
  - only analyzes 80% of light
  - Incorrectly assumes linearity outside of 10% and 90%

Linear blur profile



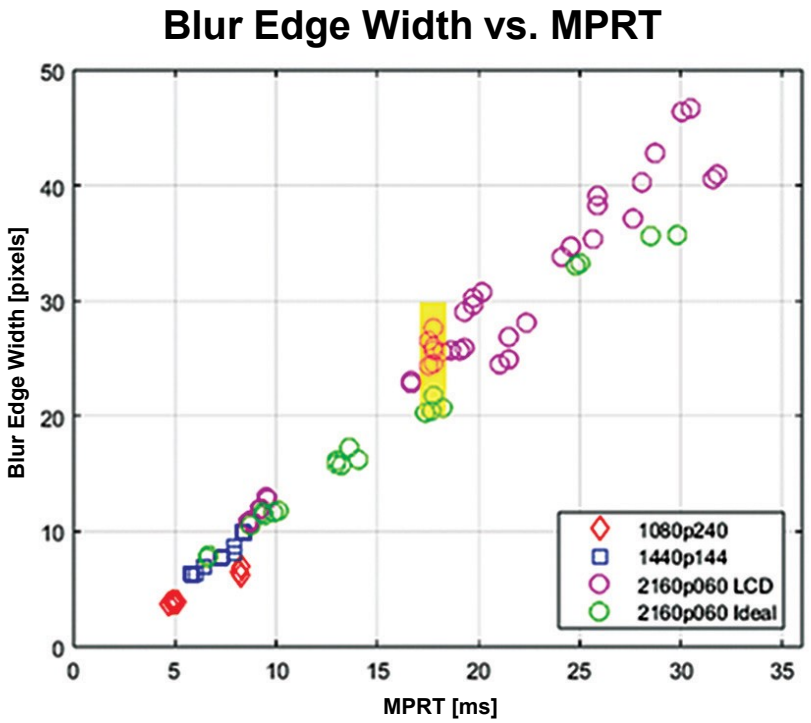
$$blur\ profile \sim k_{scale} \times MPRT$$

Non-linear blur profile



$$blur\ profile \neq k_{scale} \times MPRT$$

Blur vs. MPRT(Moving Picture Response Time)



A new metric : Clear Motion Ratio (CMR)

- **No objective blur description**
  - Gray-to-gray is a step response, do not explain the full picture
  - MPRT only analyzes 80% of light
- **A new metric must:**
  - Capture all the display light output
  - Be suitable for high density displays > 300 ppi
  - Be repeatable
  - Make fair points of comparison (eg. Limit overdrive to eliminate ghosts)

√ ClearMR uses the new metric, Clear Motion Ratio (CMR) for a *better* and *fairer* measure of display blur.

ClearMR™

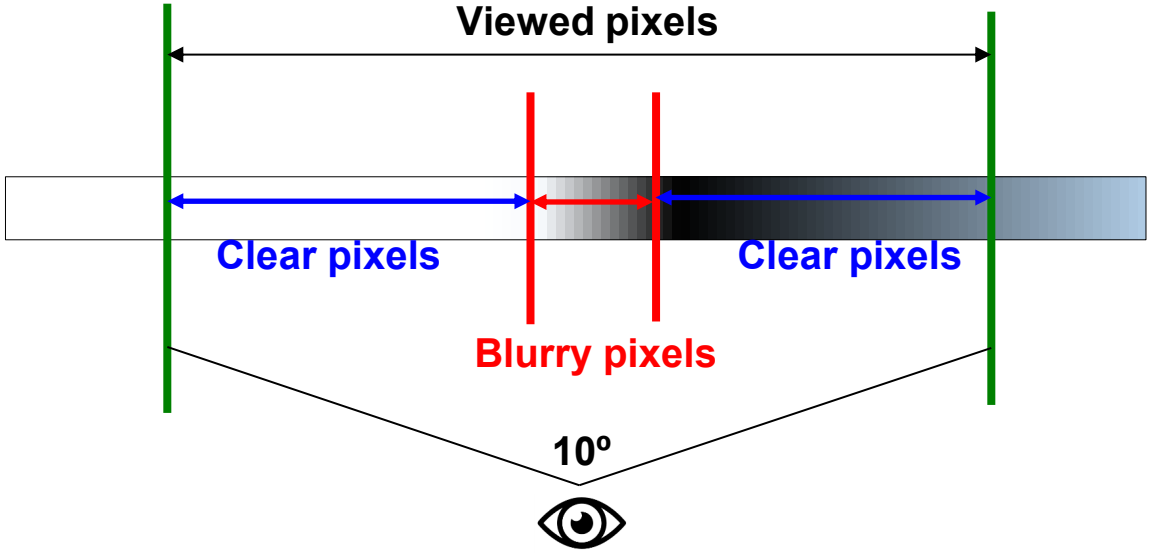
Methods

01 Problem statement

02 Clear Motion Ratio design

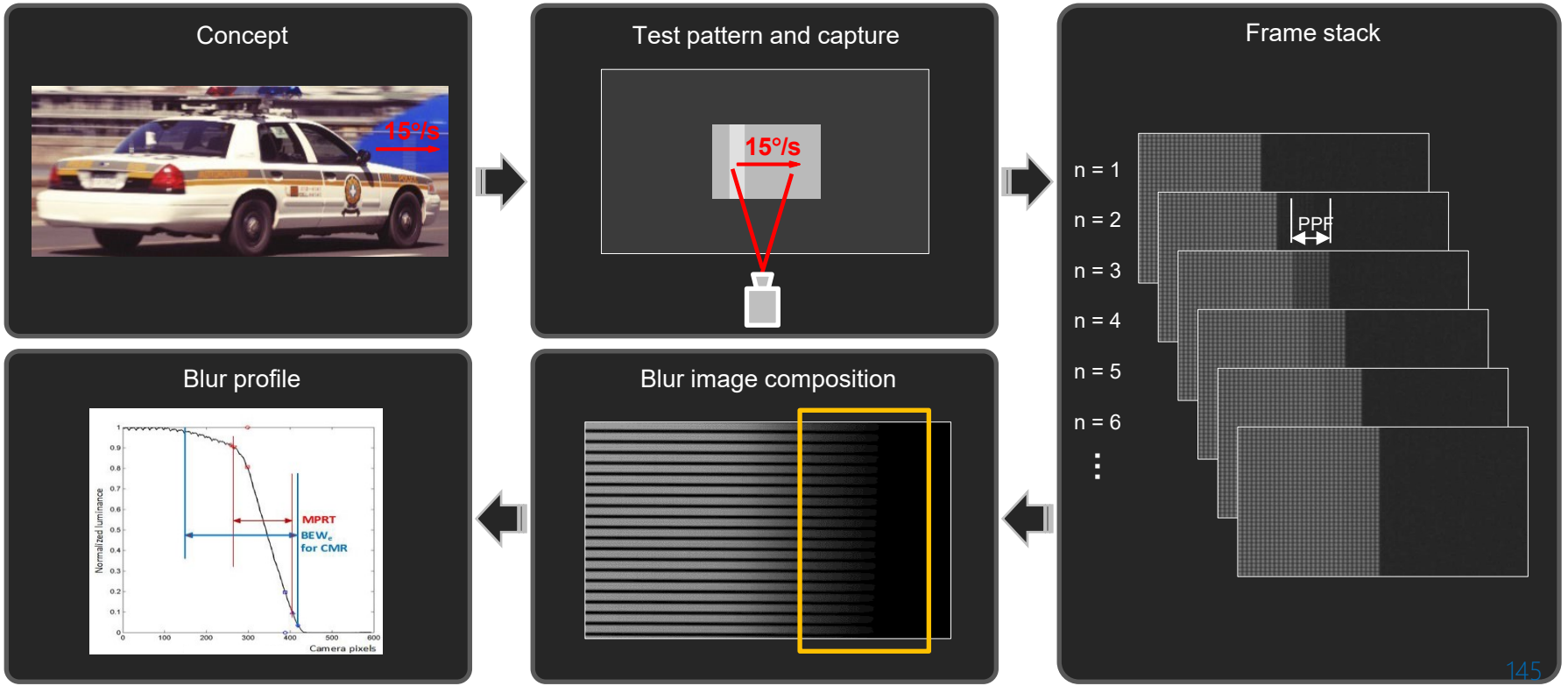
03 Seeing is believing

ClearMR index : CMR

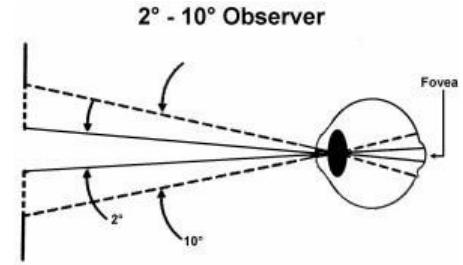


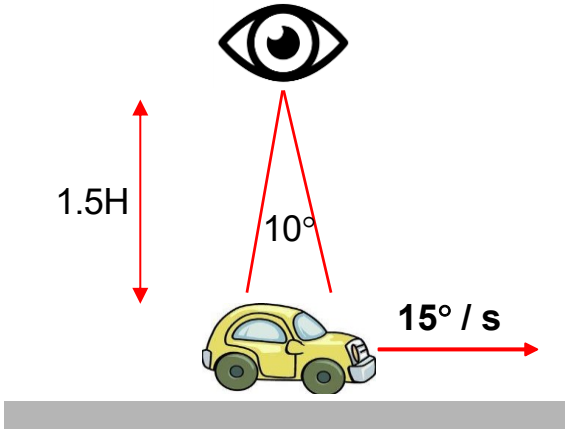
$$\mathrm{CMR} = \frac{\textit{Clear pixels}}{\textit{Blurry pixels}}$$

ClearMR : Theory of Operation



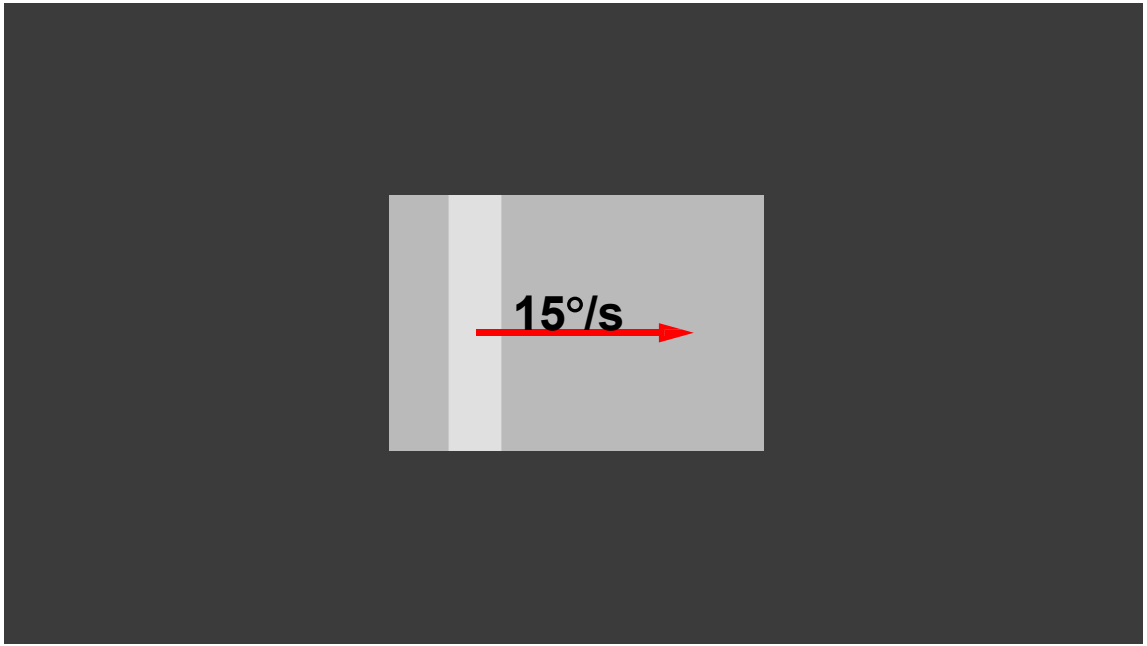
Concept



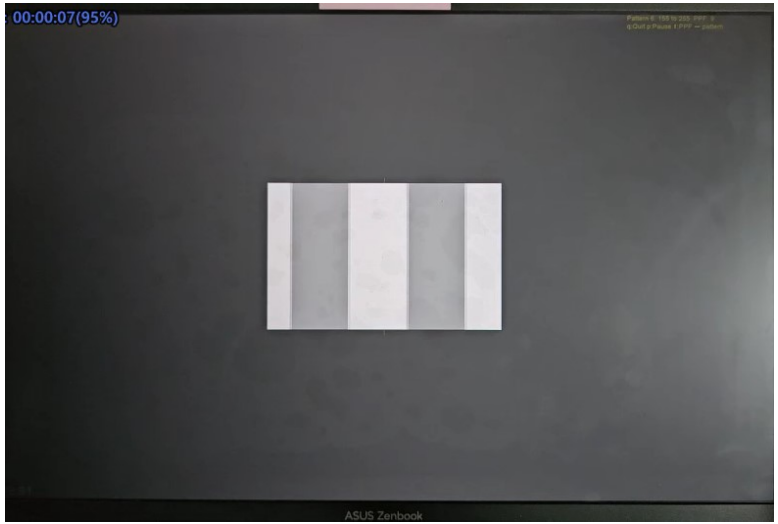


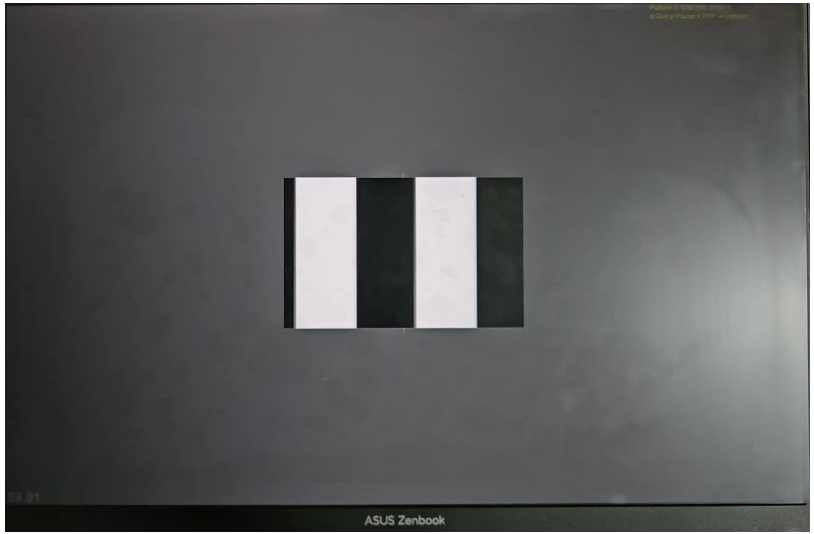
- **Determine pixels viewed when eye tracking**
  - Use a focus area similar to the CIE Standard Observer
    - **10 °** field of view good for motion
    - 2 ° model would apply to fixed objects
  - Viewing distance at **1.5H**(height)
  - Fast motion but does not exceed human tracking capability
    - **15°/s** angular velocity (v_θ)
    - ~4s to cross a 16:9 screen (61.3 °)

Test pattern



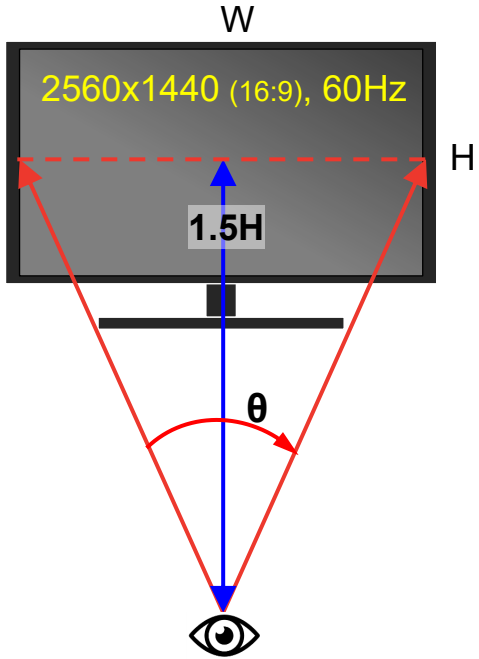
Test pattern





Patten speed : PPF

- 15°/s → PPF (pixel per frame)



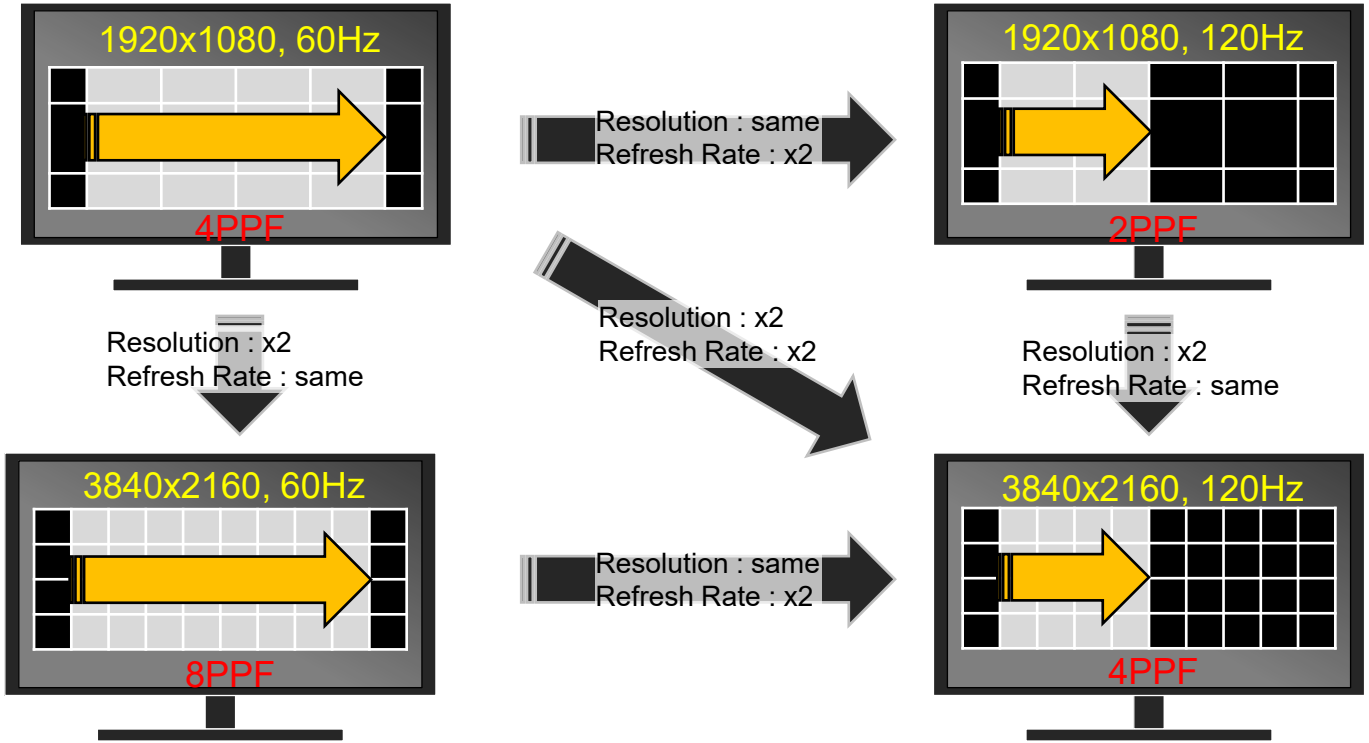
- $\tan(\frac{\theta}{2}) = \frac{W/2}{1.5H} = \frac{\frac{16}{9}H}{3H} = \frac{16}{27}$

→ $\tan^{-1}\left(\frac{16}{27}\right) = \frac{\theta}{2}$

→ $\theta = 2 \cdot \tan^{-1}\left(\frac{16}{27}\right) = 61.3°$

- $\frac{\text{Horizontal pixels}}{\theta} = \frac{2560_{px}}{61.3°} = 41.76 px/°$
- $\frac{\text{Angular velocity}}{\text{FPS}} = \frac{15°/s}{60 frame/s} = 0.25°/frame$
- $41.76 px/° \times 0.25°/frame = 10.44 px/frame$

Patten speed : PPF



Patten speed : PPF

FPS [Hz]	hres [pixels]	vres [pixels]	PPF(REAL) [pixels/frame]
60	1920	1080	7.830
60	3840	2160	15.660
120	1920	1080	3.915
120	3840	2160	7.830

1920x1080, 60Hz
4PPF

1920x1080, 120Hz
2PPF

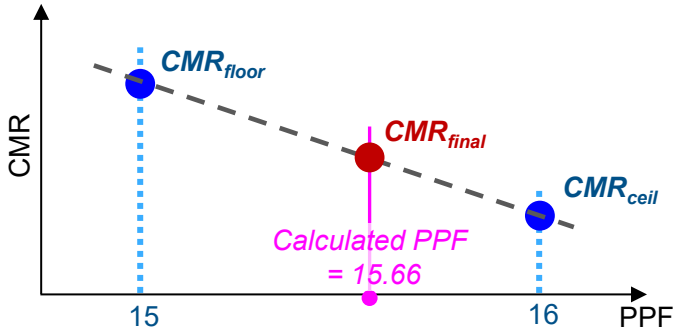
3840x2160, 60Hz
8PPF

3840x2160, 120Hz
4PPF

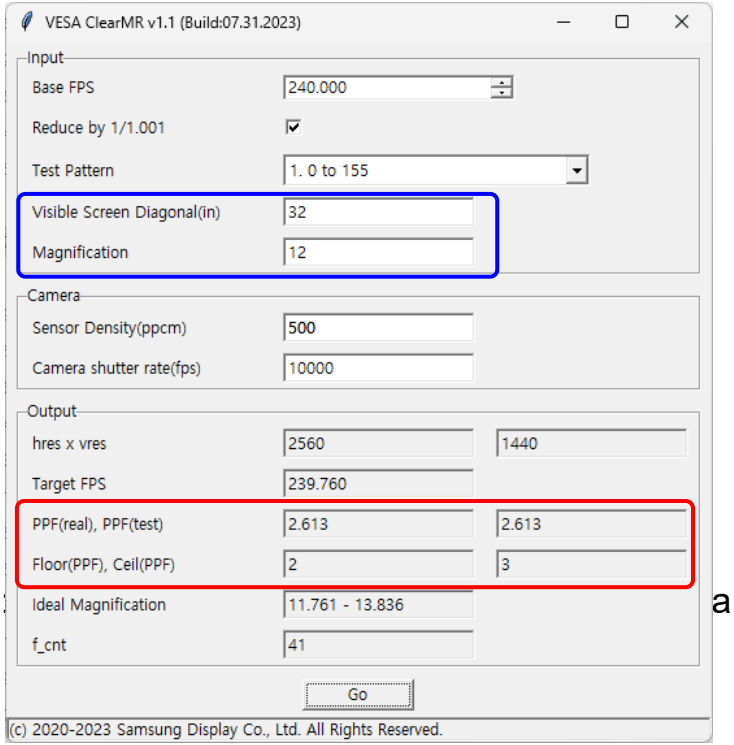
- Calculated PPF is Real number

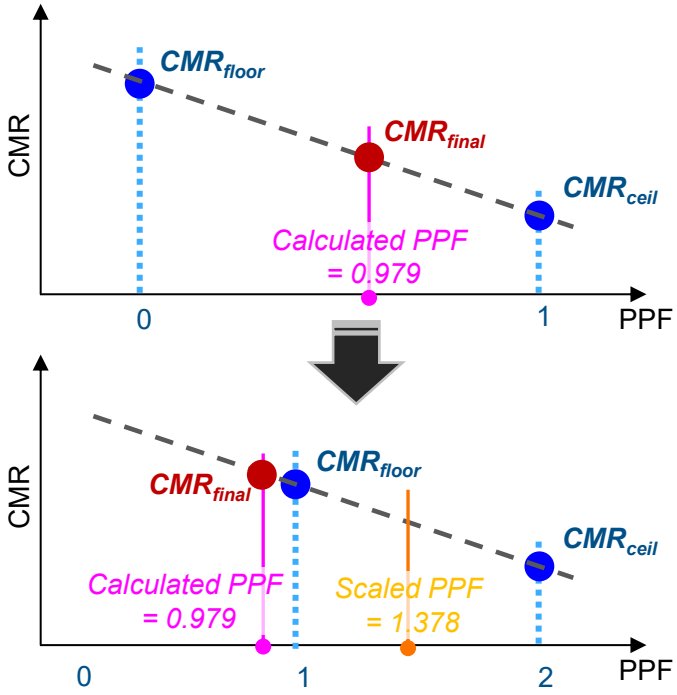
→ **flooring & ceiling**

→ **Logarithmic Interpolation**



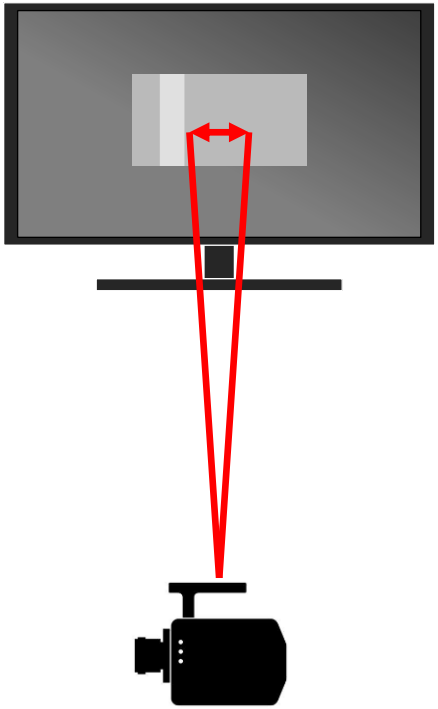
Patten speed : scaled PPF (New in v1.1)



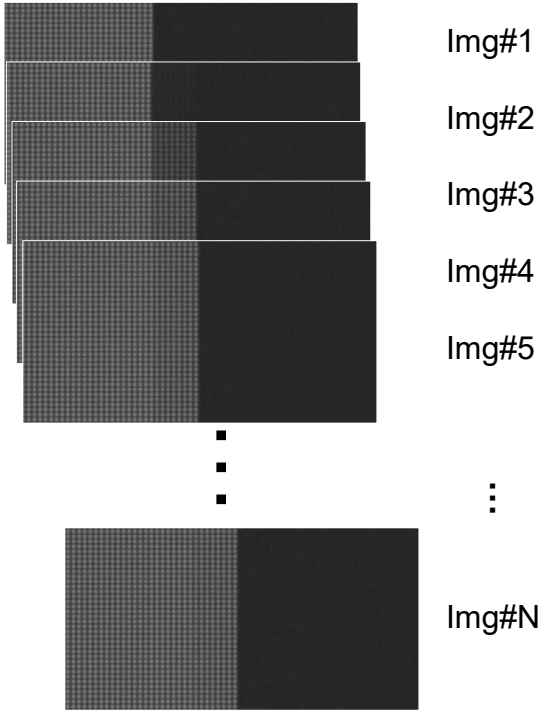


√ *Read the Information Display article for the update details*

Image captured by high-speed camera



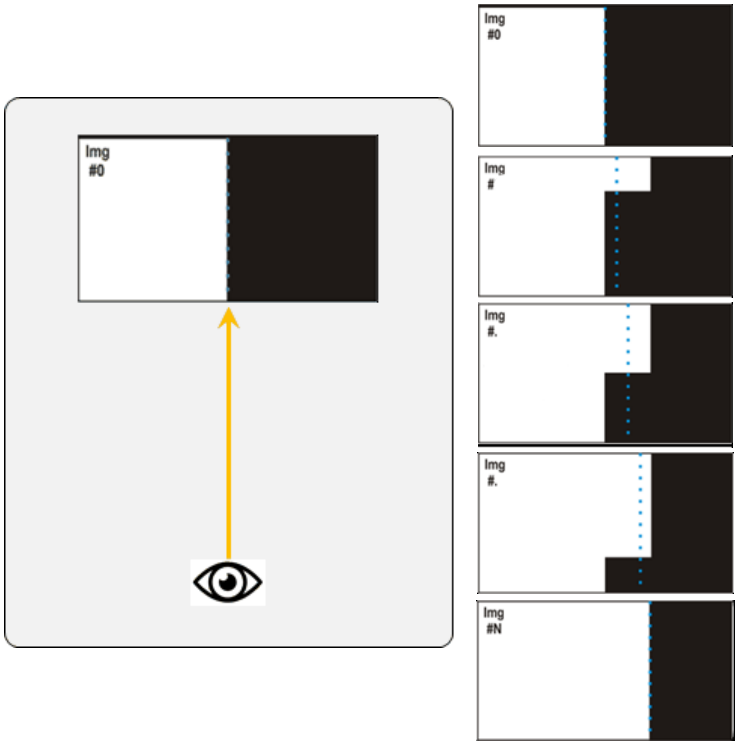
High-speed Camera

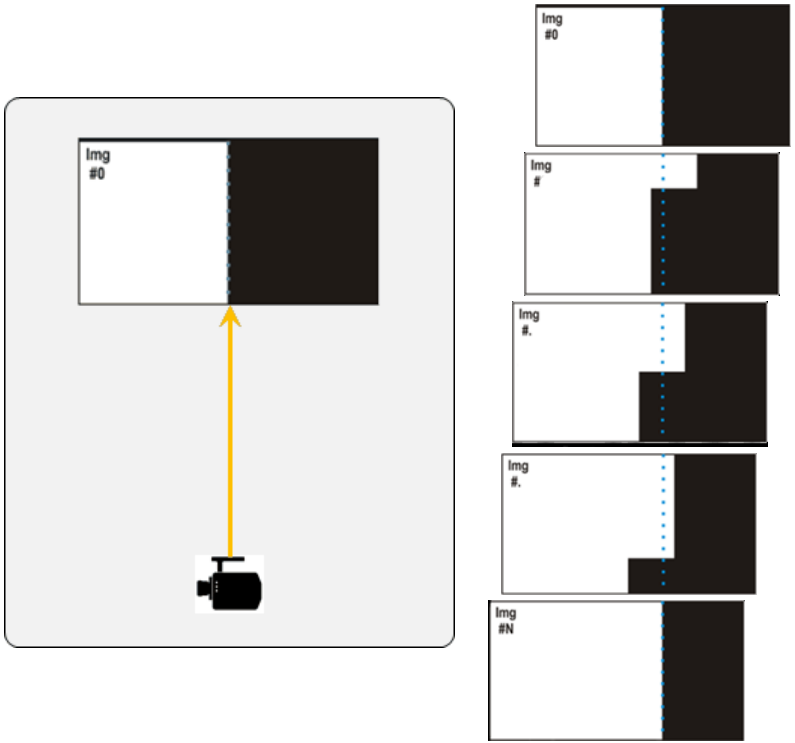


1 frame captured by high-speed camera

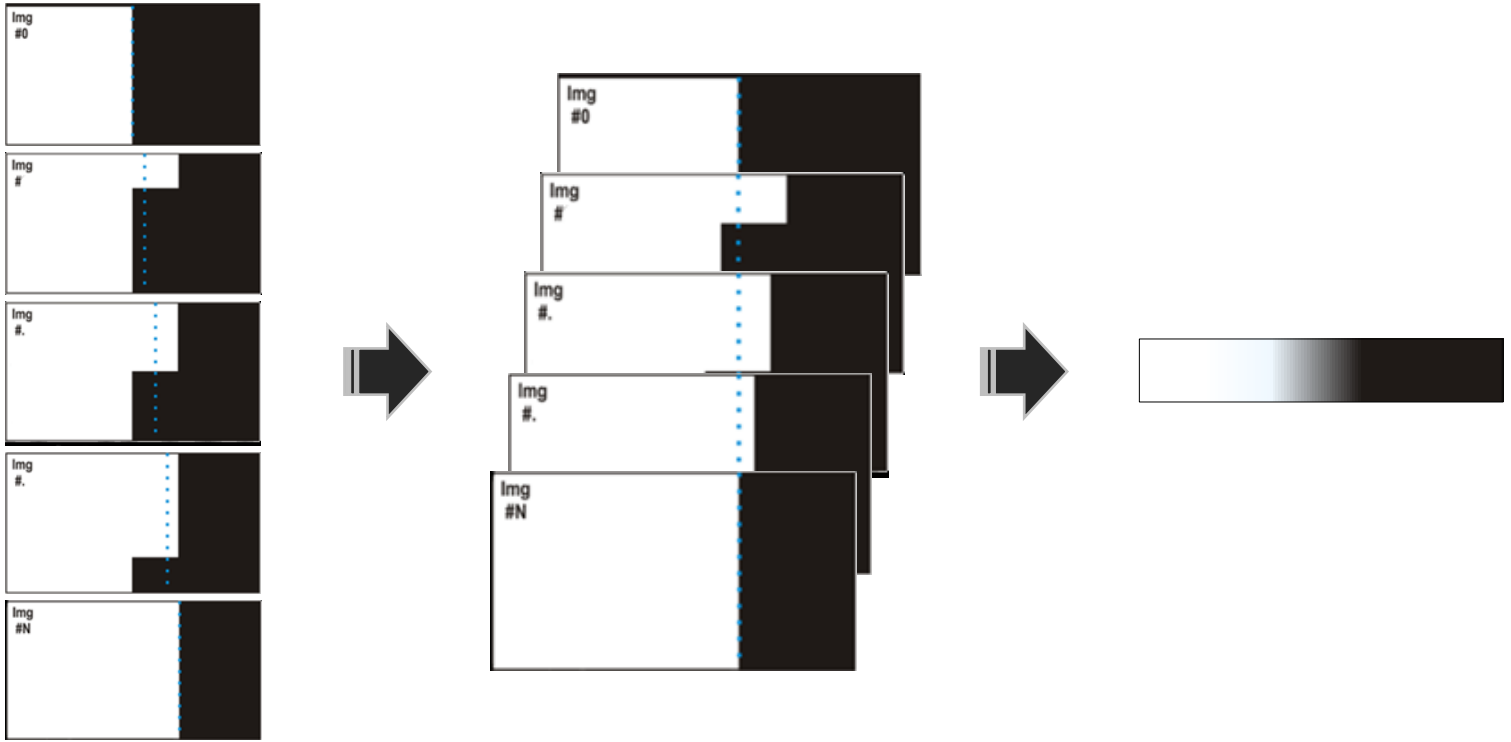
ex) 240Hz monitor with 10,000fps camera → N = 10000/240 = 41.67

Blur image composition

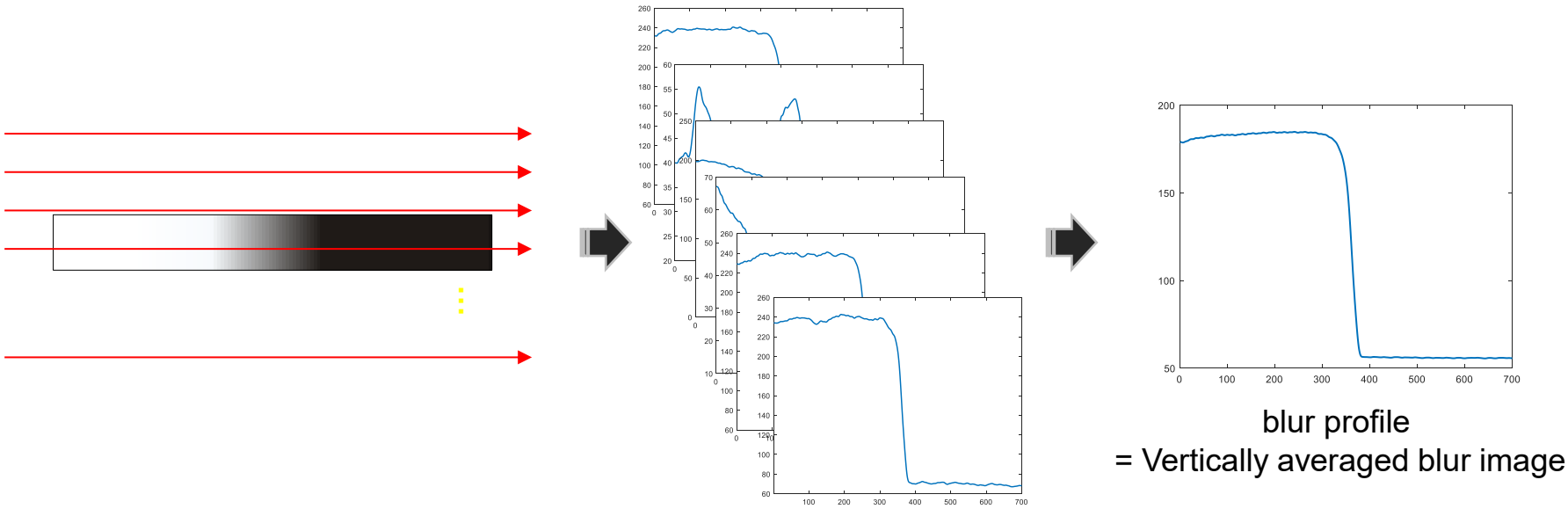




Blur image composition

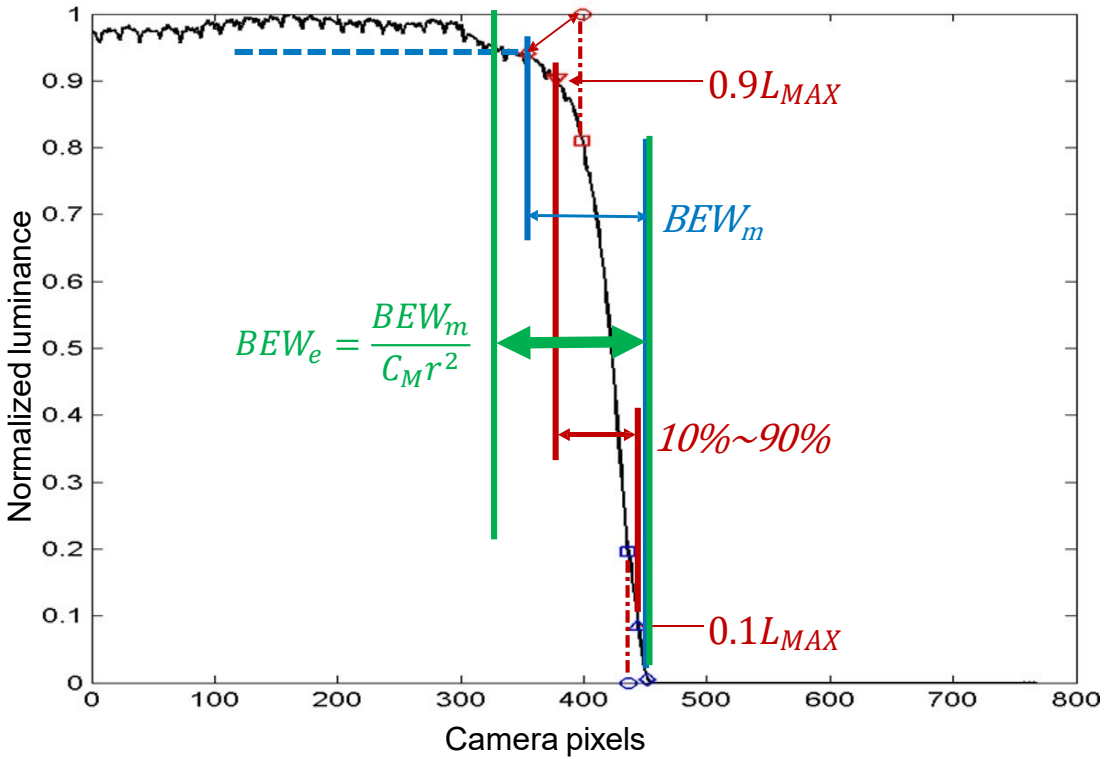


Blur profile



blur profile
= Vertically averaged blur image

Profile identifies the Blur Edge Width (BEW)



- Accounts for non-linearity
- Accounts for light outside of BEW_m
- Challenge: calculation should include all luminance change
- BEW_m is between the knees (◊) of the profile
- BEW_e corrects for non-linearity of the profile locus outside of BEW_m

* BEW_m : measured BEW

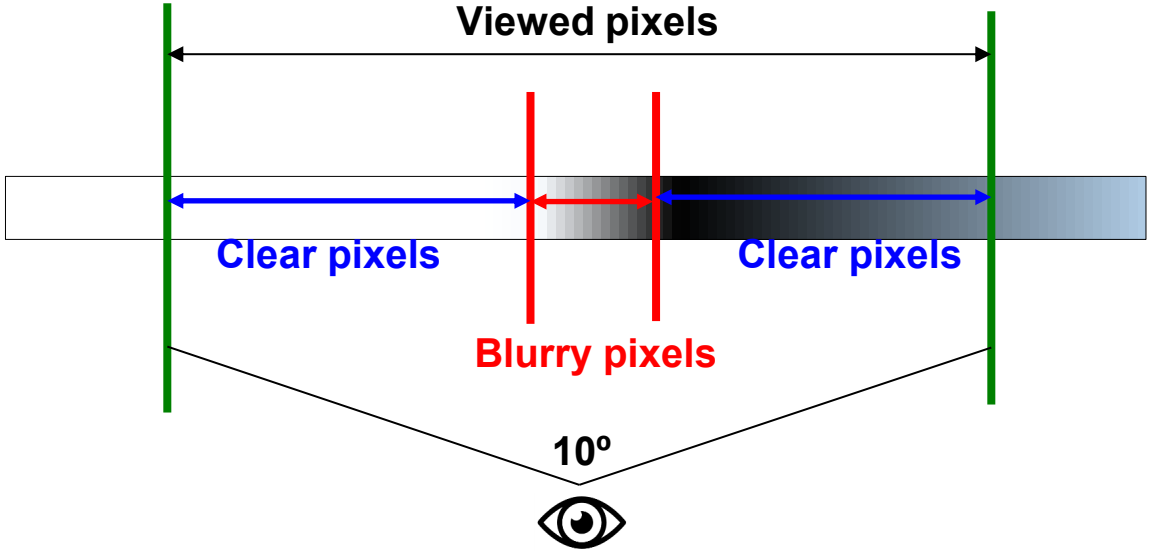
* BEW_e : effective BEW

* C_m : contrast modulation

* r^2 : coefficient of determination

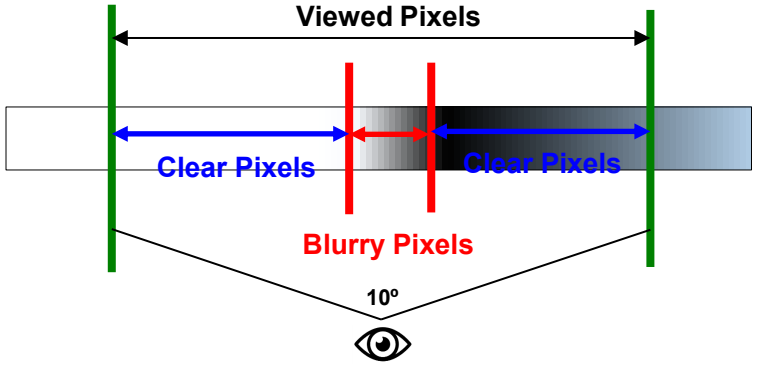
CMR(Clear Motion Ratio)

Clear Motion Ratio : Ratio of *Blurry pixels* and *Clear pixels* in a *10°* FOV with Viewing distance at *1.5H*



$$\mathbf{CMR} = \frac{\boldsymbol{Clear\ pixels}}{\boldsymbol{Blurry\ pixels}}$$

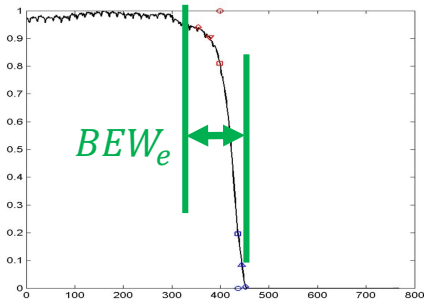
CMR(Clear Motion Ratio)



$$\text{CMR} = \frac{\textit{Clear pixels}}{\textit{Blurry pixels}}$$

$$\textit{Viewed pixels} = 2 d_v v_{res} \tan\left(\frac{arc}{2}\right)$$

$$d_v = 1.5H$$
$$v_{res} = \textit{Display Vertical Resolution}$$
$$arc = 10°$$



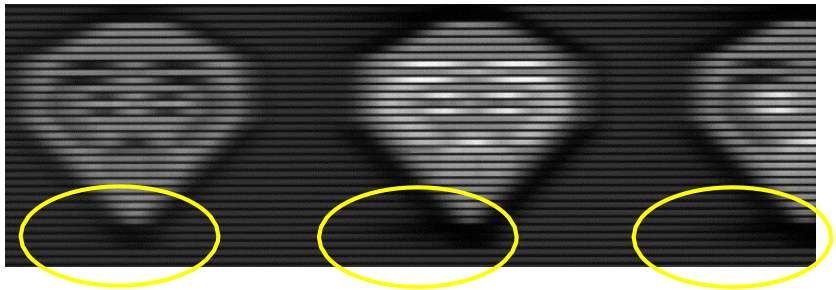
Camera pixels

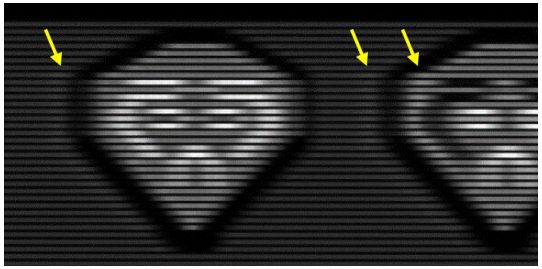
$$\textit{Blurry Pixels} = BEW_e$$

$$\textit{display pixels} = \textit{camera pixels} \times \frac{\textit{display pixel density}}{\textit{camera pixel density}}$$

Ghosts and Coronas

- **Ghosts**
  - Uneven transitions
  - Trailing artifact
  - Usually, a dark trail
- **Coronas**
  - Inverse of ghosts
  - Over-shooting the final pixel value
  - A trailing glow

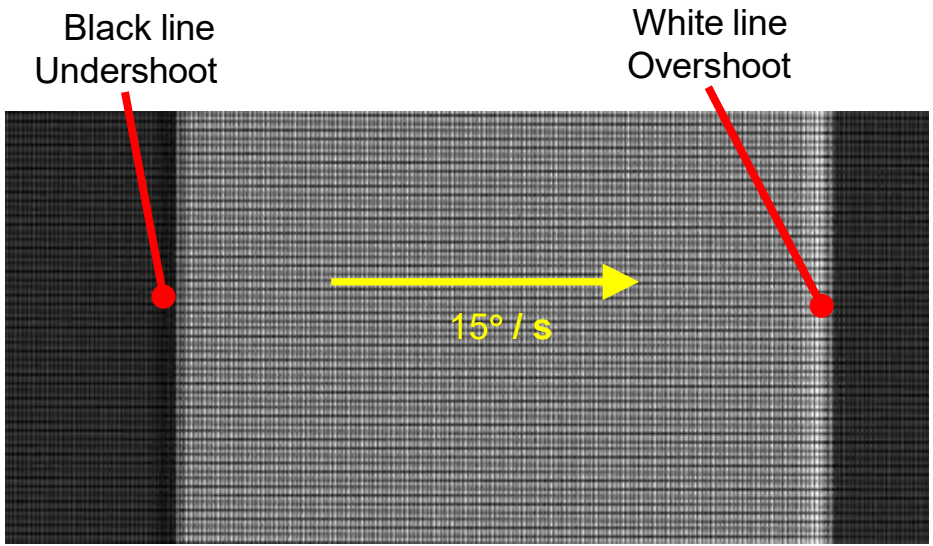


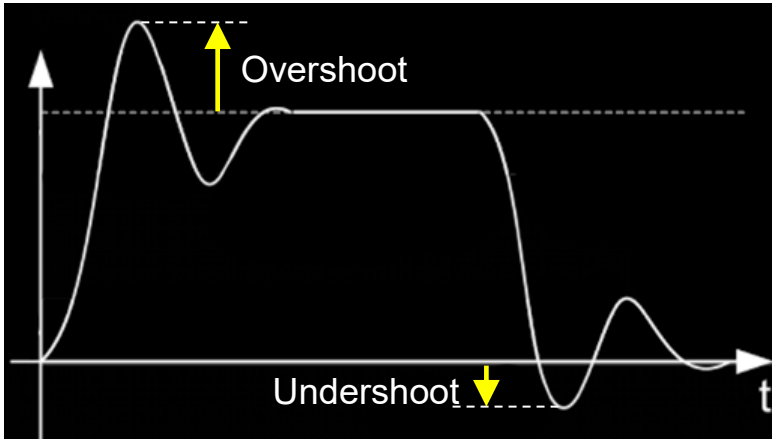


Working definitions by Mark Rejhon (2021)[1]…

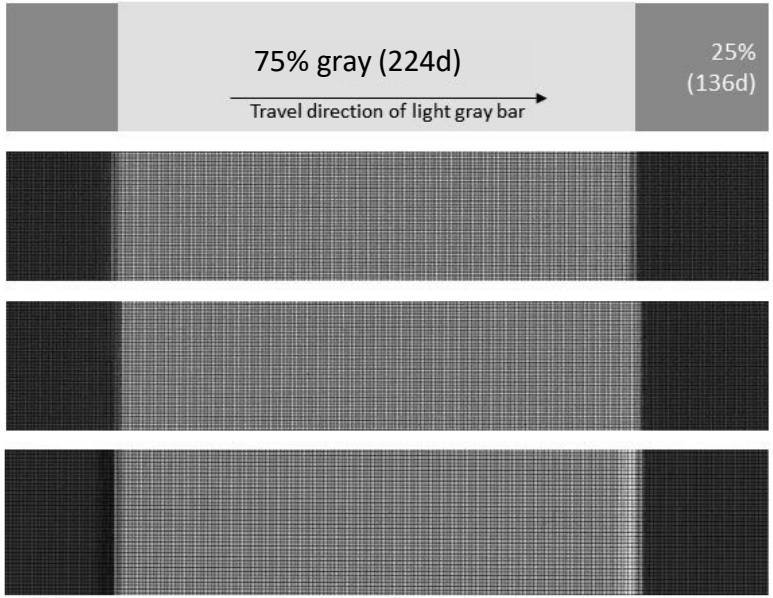
1. Accessed July 26, 2021. https://blurbusters.com/faq/lcd-motion-artifacts
2. Test patterns © 2021, Samsung Display Co., Ltd. right reserved.

Over/undershoot creates ghosts and coronas





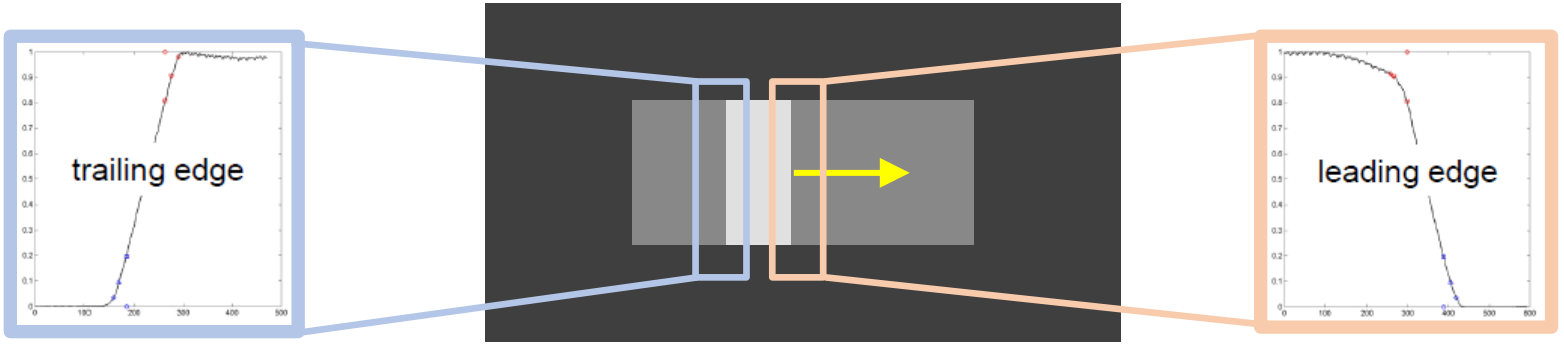
Moving bar subjective test



Picture	Views	Leading Edge seen	Trailing edge seen	Fractional response
Test image	40			
Default	8	0	0	0
Increased overdrive	16	7	6	0.41
Excessive overdrive	16	16	16	1.0

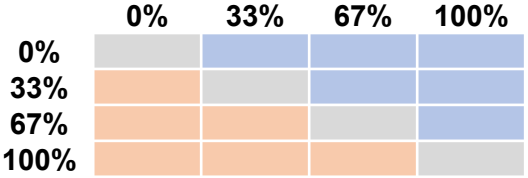
$$Overshoot < 20\%, \quad Undershoot < 10\%$$

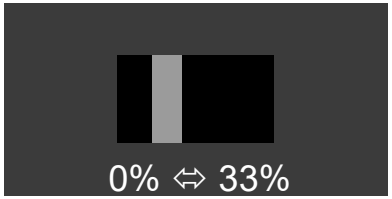
Rising and Falling (Leading and Trailing)

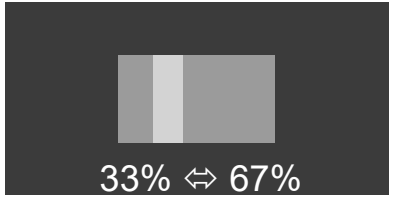


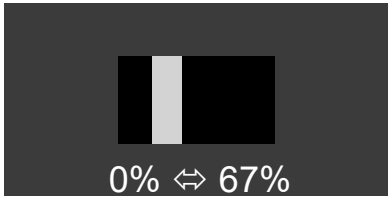
	Leading			Trailing		
	0%	33%	25%	67%	75%	100%
0						
25%						
33%						
67%						
75%						
100%						

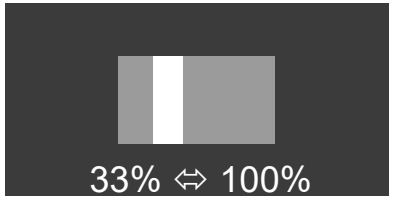
Rising and Falling (Leading and Trailing)

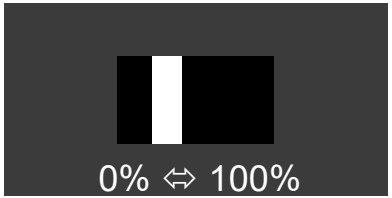


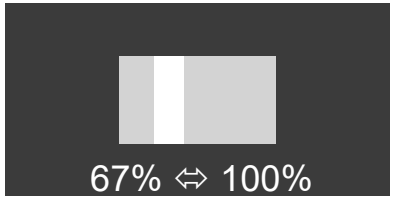


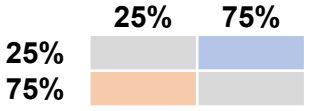


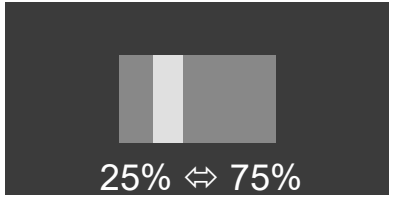


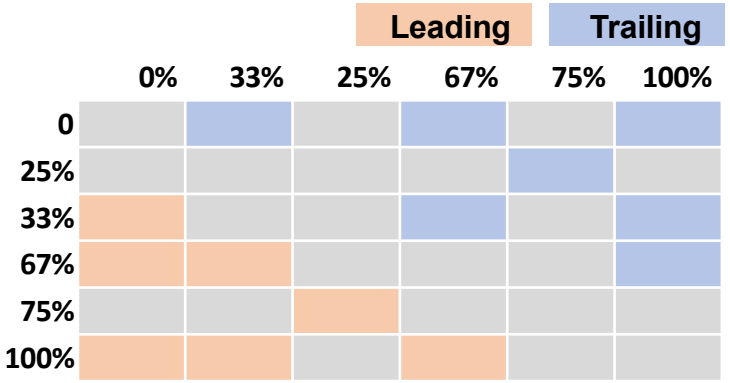












Conclusion

01 Problem statement

02 Clear Motion Ratio design

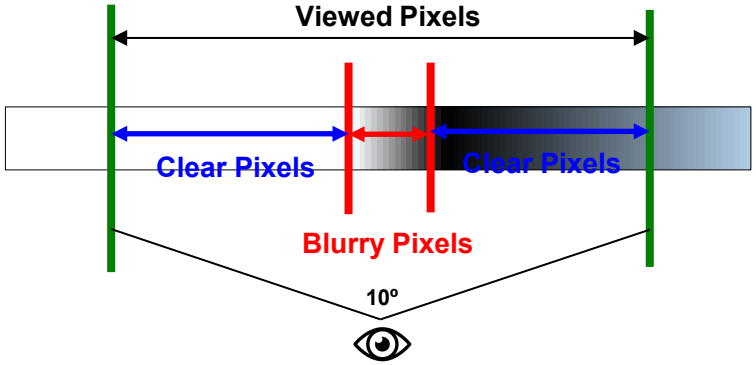
03 Seeing is believing

ClearMR Tiers

VESA CERTIFIED ClearMR

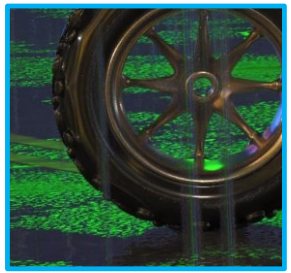
ClearMR™ TIER	CMR RANGE
ClearMR *3000*	2500 ≤ CMR < 3500
ClearMR *4000*	3500 ≤ CMR < 4500
ClearMR *5000*	4500 ≤ CMR < 5500
ClearMR *6000*	5500 ≤ CMR < 6500
ClearMR *7000*	6500 ≤ CMR < 7500
ClearMR *8000*	7500 ≤ CMR < 8500
ClearMR *9000*	8500 ≤ CMR < 9500
ClearMR *10000*	9500 ≤ CMR < 10500
ClearMR *11000*	10500 ≤ CMR < 11500
ClearMR *12000*	11500 ≤ CMR < 12500
ClearMR *13000*	12500 ≤ CMR

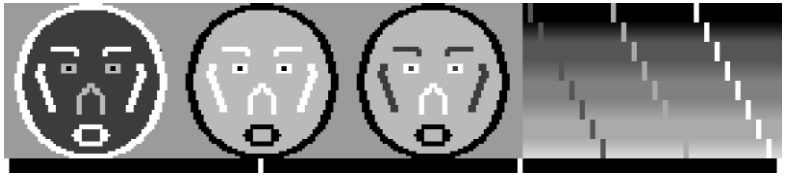
*These tables may be extended in the future to certify faster products



$$\mathbf{CMR} = \frac{\boldsymbol{Clear\ pixels}}{\boldsymbol{Blurry\ pixels}}$$

Simulated results : Seeing is believing

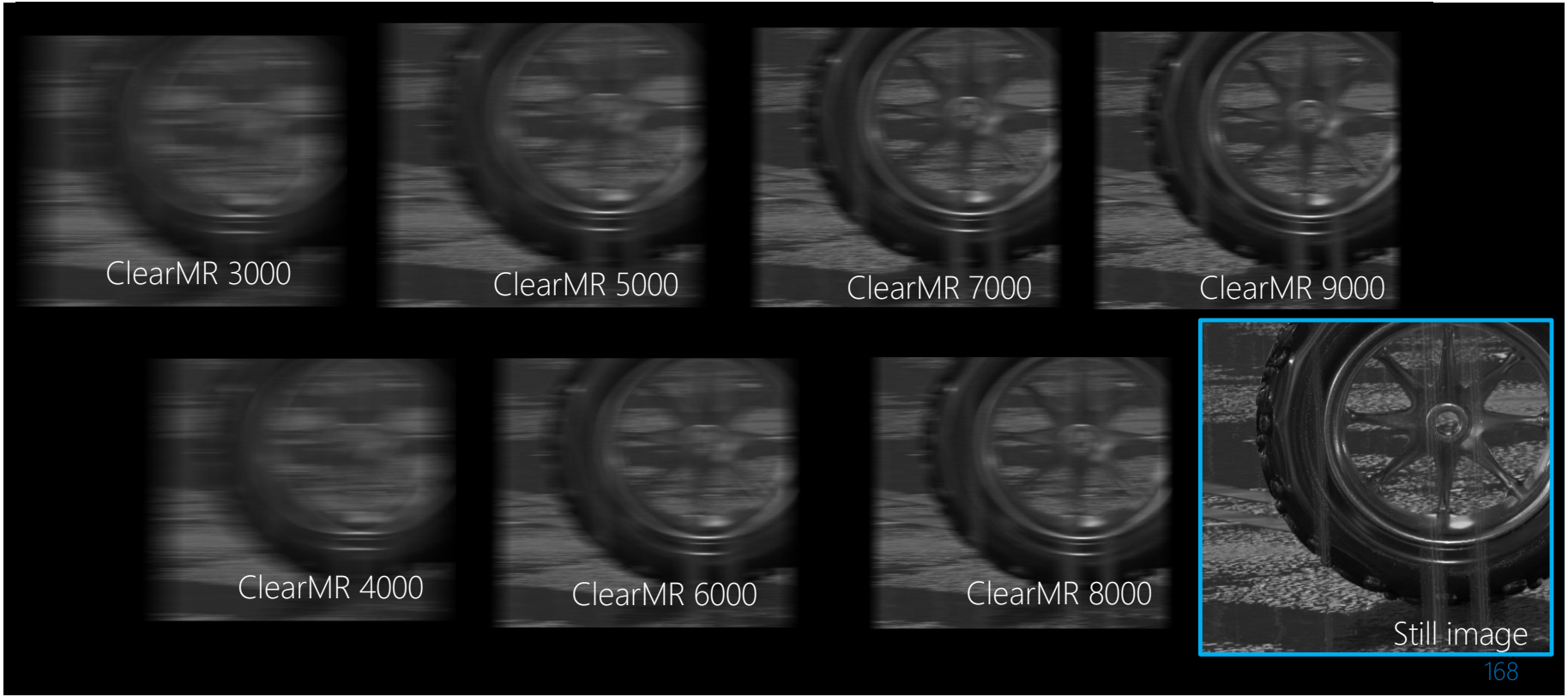




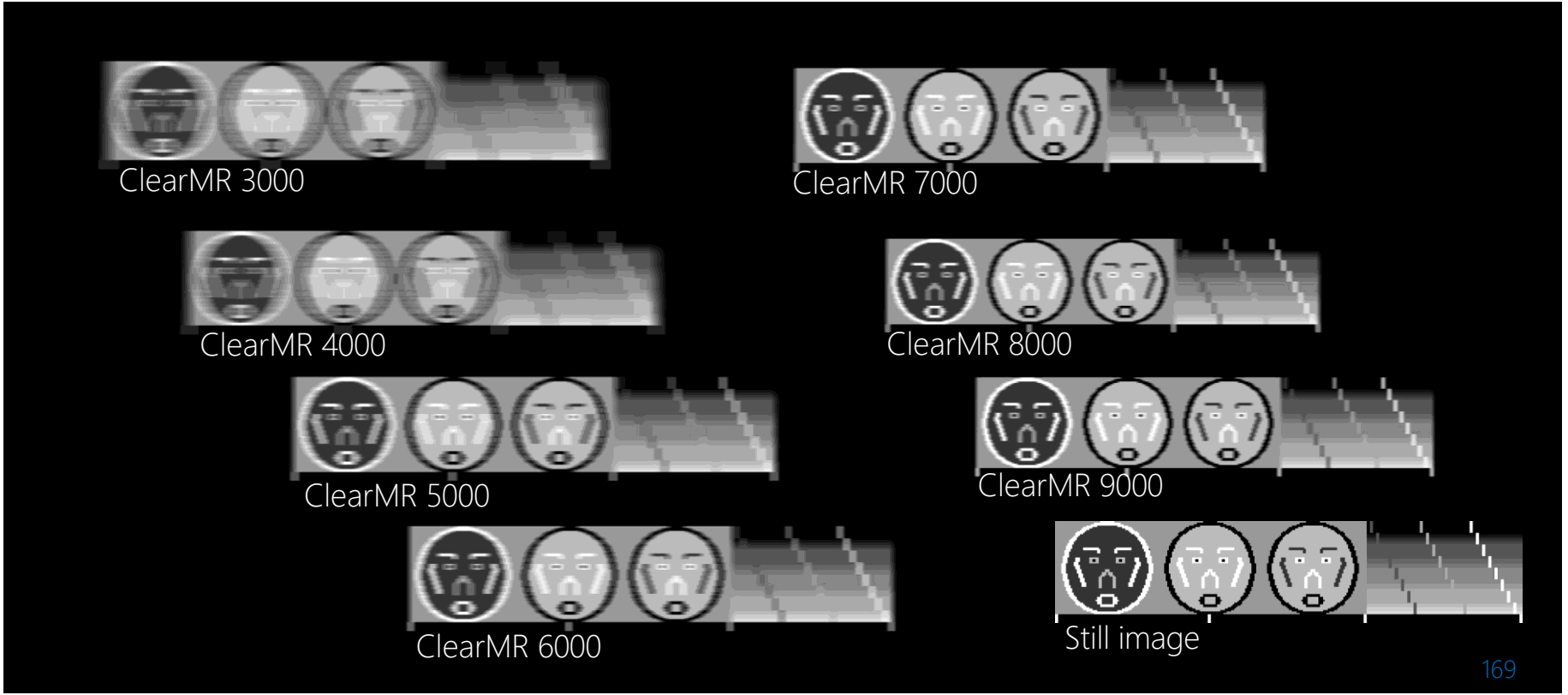
- Ideal edges, $C_M = 1$, $r^2 = 1$
- Show on 2560 x 1440 display

* ambientCG images are 400 x 400 from York University, licensed under a Creative Commons BY 4.0 license)
* Grayscale test pattern 300 x 70 © 2022 Samsung Display Co., Ltd. rights reserved.

Animated tire

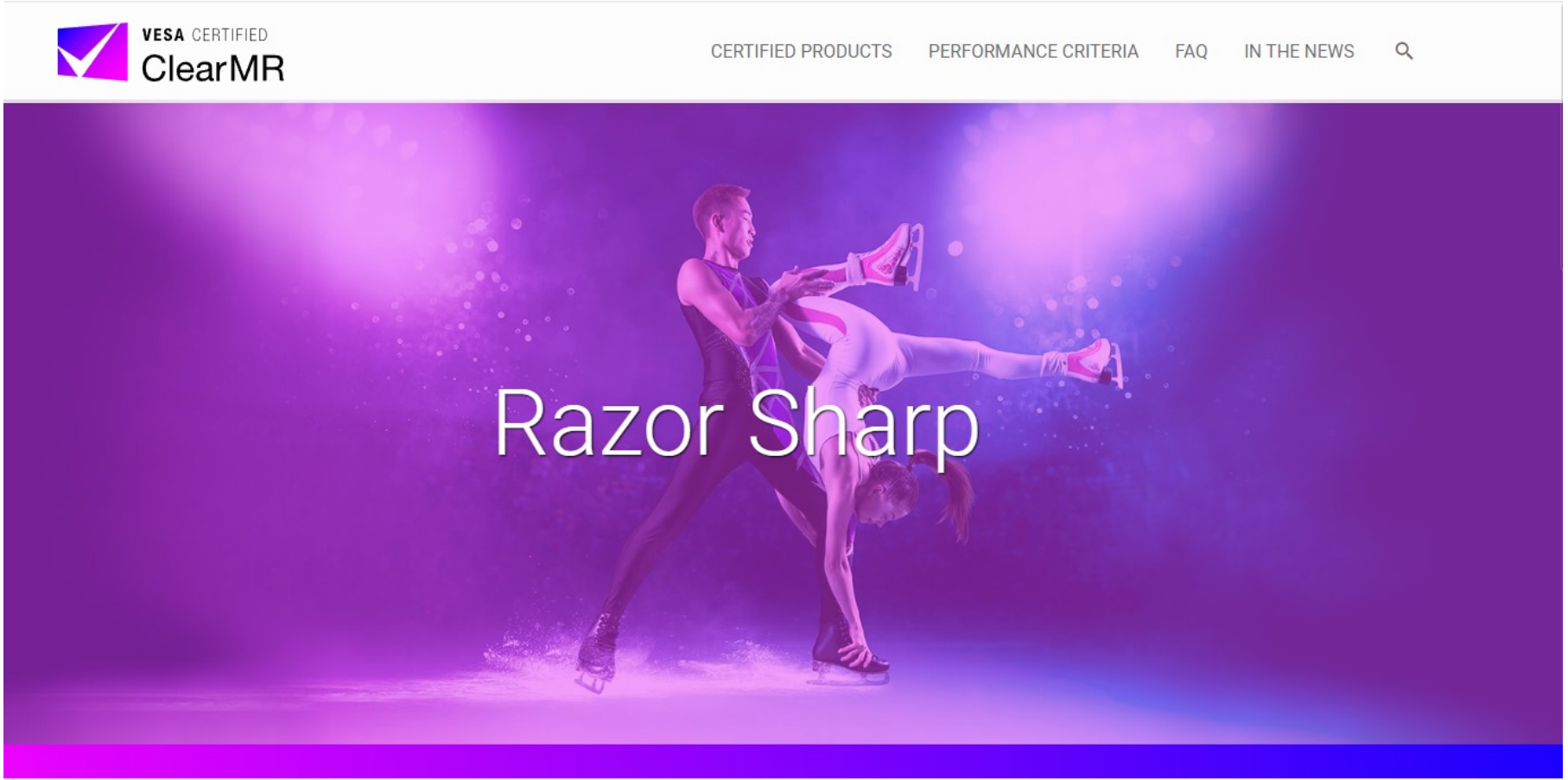


Grayscale cartoons and diagonal bars



Summary

- Press release announcing ClearMR certification program and specification, www.vesa.org, **Aug 22, 2022**.
- **ClearMR 1.1** is a minor update of original ClearMR test specification launched on **Oct 17, 2023**.
- ClearMR captures all blur not 80% like other metrics
- Visually verified
- Sets a fair basis for comparison
  - Limits overdrive to eliminate ghosts
  - Eliminates strobing unless an intrinsic part of the panel design
- VESA is continuously refining its front-of-screen performance standards to align with new display and test technologies



Visit www.clearmr.org for the latest certifications and test details.

VESA

Thank you

Yongwoo Yi
yongwoo.yi@samsung.com

Compliance Testing

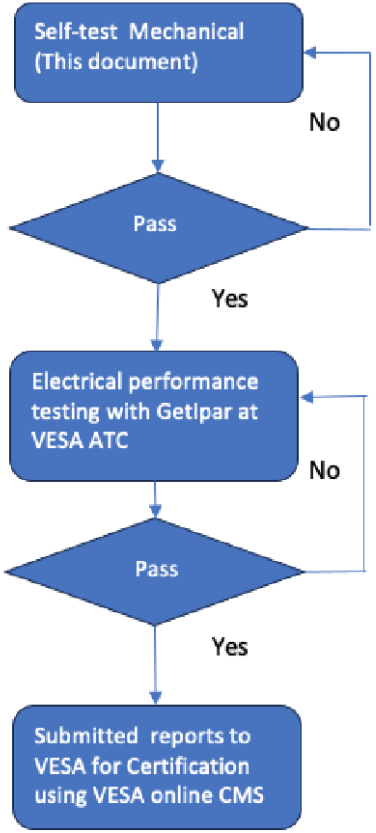
Compliance Test Specification Updates

VESA has updated base specification and CTS documents in past two years

- DP 2.1a Spec update – released 12/2023
- DP 2.1 PHY CTS v1.0 – released 6/23
- DP 2.1 Link CTS v1.0 – released 11/2023
- Enhanced DP Connector Self-Test v2.1 – 8/2024
- DP Alt Mode CTS v2.1 – 8/2024
- Embedded DP (eDP) – 9/2024

Enhanced Connectors

- UHBR rates = the need for high performance DP connectors
- VESA created specification and test requirements for Enhanced DP connectors (fsDP and mDP)
- This includes both right angle and vertical mount connectors



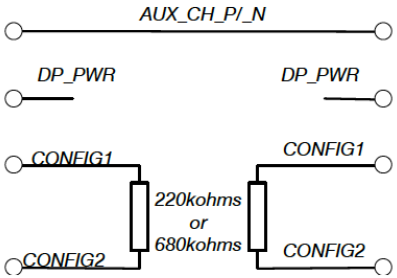
DP40, DP54 and DP80 Cable Specification and Certification program

- Work on Enhanced DP cable and connector specifications and test requirements started in 2021 to ensure high performance connectors and cables would be available for products supporting UHBR rates
- DP40, DP54 and DP80 Certified cables provide added assurance of proper operation at the highest link rates (UHBR10, UHBR13.5 and UHBR20 Gbps)
- Over 150 Enhanced DP cables and connectors have been certified since launch of the Enhanced DP cable and connector certification programs
- DP40 cable performance tier replaced with DP54 in 2024
- DP54 cables are required to support UHBR10 and UHBR13.5 link rates, enabling longer cables for sources and sinks that implement 13.5Gbps as highest link rate

DP54 cables replace DP40

DP40	DP80	
UHBR10	UHBR13.5	UHBR20
10GbpsX4 lanes	13.5GbpsX4 lanes	20GbpsX4 lanes
~3 meters max	~1 meter max length	
DP54 (DP 2.1a specification)		**DP80**
UHBR10	UHBR13.5	UHBR20
10GbpsX4 lanes	13.5GbpsX4 lanes	20GbpsX4 lanes
~3 meters max length		~1 meter max

Cable ID used to detect cable caps



Product certifications* 2022/2023/2024

Products	2022	2023	2024
DP Sources	141	99	60
DP Sinks	339	277	320
DP Cables	42	59	56
DisplayHDR	388	397	369
ClearMR	14	45	30
AdaptiveSync	25	80	48

*Note: numbers are base model certs not including family models

VESA PlugTest Events

- Provide significant value to member companies, particularly as new capabilities and products are deployed.
- Demonstrate and improve Traditional Interoperability
- Test Native DP and DP Alt Mode over USB Type-C™ products
  - UHBR rates, DSC, FEC, DisplayHDR and other new capabilities
  - Verify Test Equipment Correlation
- VESA hosted two successful PlugTests in 2023 (Taiwan and US)
- VESA hosts two PlugTests in 2024
  - Hawaii, USA: **Q1 2024 (completed)**
  - Taipei, Taiwan: **Q4 2024 (Oct 14-18th Taiwan)**

VESA Technology Development Areas

VESA technology development

VESA members are collaborating on several key technology areas

- Embedded DisplayPort - v2.0 (published Sept 2024)
- DP Tunneling over USB4 – compliance testing has begun
- AR/VR Task Group
  - Focused on creating solutions roadmap to meet performance, power and implementation requirements for future AR/VR needs. Specification is released. Work on CTS underway
- DP Automotive Extension Task Group
  - Working with automotive industry to address needs for high-resolution performance in this market segment
  - Working on DP AE CTS and testing
- Bulk Display Protocol
  - BDP specification and CTS nearing release
- Display Performance Metrics Task Group
  - DisplayHDR, ClearMR, AdaptiveSync

Summary

Summary

- Product shipments and certifications on based on VESA technologies continue to grow
- DP 2.1 UHBR capable product development and certifications have ramped up in 2024
- VESA Enhanced cable and connector certification programs have been very successful with significant numbers of DP40, DP54 and DP80 cables certified
- DisplayPort over USB-C is a game changer for small form factor and portable products and is now the defacto standard for laptops, tablets and handheld devices
- Display Performance Standards adoption and certification have been extremely successful the last several years
- Development and adoption of new technologies continues to drive increases in VESA membership growth

THANK YOU

DisplayPort.org
DisplayHDR.org
ClearMR.org
AdaptiveSync.org
VESA.org

Questions?

Teledyne LeCroy
Test Solutions
for DisplayPort v2.1

M42de 80G Video Analyzer/ Generator

TELEDYNE LECROY
Everywhereyoulook™

Kyongsik Kim
president@ksdata.co.kr
Tel. +82 (02) 4073496-7
Website: http://www.teledyne.com/

Teledyne LeCroy
Kyong Sung Data Co.
#906, New Family-2 Officetel
99-2, Garakbon-dong, Songpa-ku,
Seoul, Korea 05719

Teledyne LeCroy DisplayPort Test Platforms

- **Quantumdata M42de Analyzer / Generator**
  - DisplayPort 1.4 & 2.1 (UHBR) Lane Rates
  - DP80 and USB Type-C® connectors
  - Deep Capture / Analysis
  - T.A.P.4™ Passive Monitoring
  - Comprehensive DP 1.4 & 2.1 Compliance Coverage
    - Link, DSC, LTTPR, EDID & MST
  - qdPrime™ Automated Test Suite

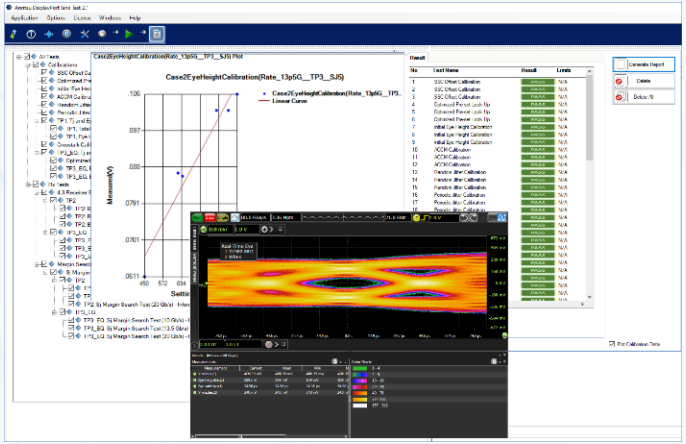
- **Quantumdata M21 Analyzer**
  - Portable DP Analyzer & HDMI Analyzer / Generator
  - DisplayPort Source Testing only (up to UHBR 13.5Gb/s)
  - AUX Channel Monitoring

GRL
Connecting the World

graniteriverlabs.com

GRL DisplayPort

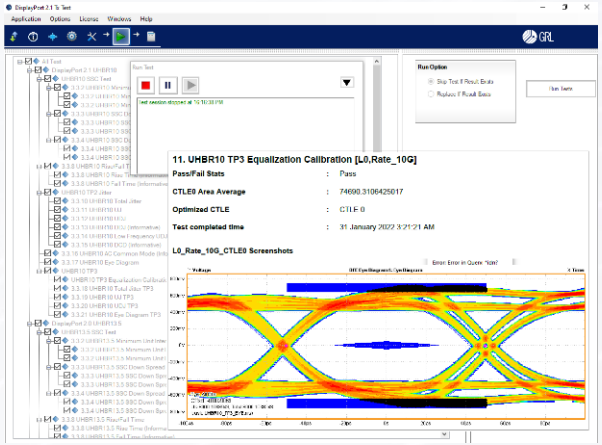
2.1 Tx PHY Test Solution
1.4/2.1 Rx PHY Test Solution



DisplayPort 1.4/2.1 Receiver Calibration and Test Automation

An automated and efficient way to test your DisplayPort 2.1 Sink Device (GRL-DP21-SINK-AN, GRL-DP14-SINK-AN)

24Q4 Note: The Preset calibration feature based on “SCR_DP 2.1 PHY CTS Preset Calibration d3” is planned to be added in the next SW release.



DisplayPort 2.1 Transmitter Test Automation Solution

A quick and straightforward way to test and debug your DisplayPort 2.1 transmitter products efficiently (GRL-DP21-TX)

UNIGRAF

DisplayPort

USB Type-C

sales.asia@unigraf.fi

UCD-500 Gen2

DP 2.1 Generator & Analyzer

- DP 2.1 and DP 1.4a Link Layer CTS Tool
- DP 2.1 Sinks and Sources up to 8K@60Hz (UHBR 20Gbps / Lane) and 16K@60Hz with DSC
- Supports DP and USB-C connectivity
- DP TX/RX Link Training, Power Delivery(USB-C), DSC, FEC, DPCD/EDID editor, Adaptive-Sync, HDCP 2.3, etc.
- Capture and logging functions
- Now featuring Link Analyzer, Panel Replay and eDP test functions

USB Type-C

DisplayPort

UNIGRAF

DisplayPort Alt Mode Compliance Testing

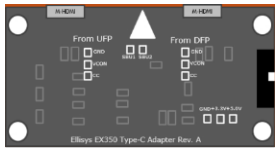
SYMBIOSYS ALLIANCE

Ellisys USB Explorer 350

- The Explorer has three main functions
  - Analyzer
  - Generator
  - Examiner™ Compliance Test Suite
    - VESA-Approved

USB Explorer™ 350

- The Examiner compliance test suite performs all required DisplayPort Alt Mode testing



Type-C Interconnect Assembly

KEYSIGHT

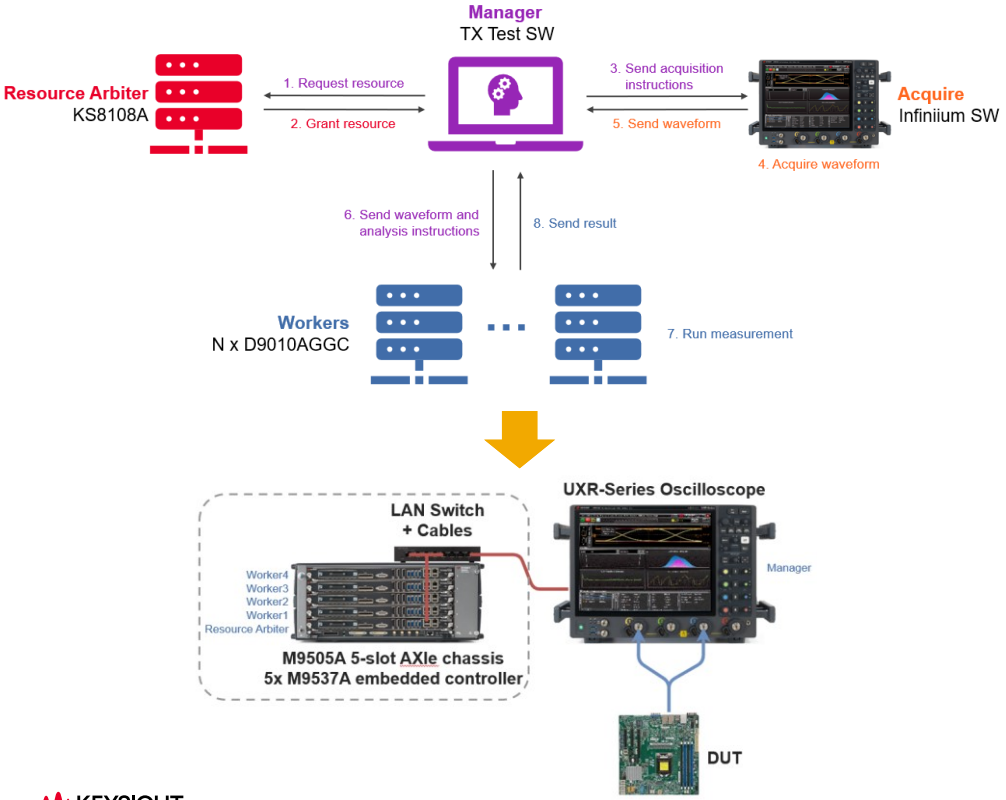
Measurement Disaggregation

Contact Information
Abhijeet Shinde
Abhijeet.Shinde@keysight.com

Keysight Technologies

Challenge: DisplayPort Test Time Optimization

Solution: Measurement Disaggregation

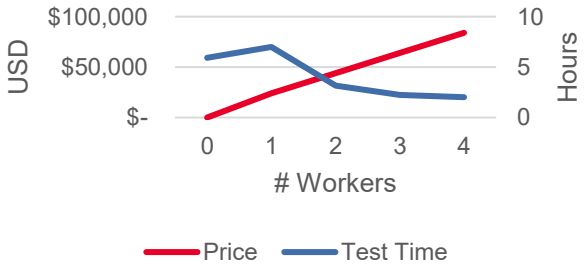


What is it costing you?

- Extensive test plan requires long test time
- 75% of test time is spent processing data

What is an ideal solution?

- Significant test time improvement using Measurement Disaggregation
- Re-use of your invested solution
  - Saves $$$
  - Builds on your present equipment and knowledge

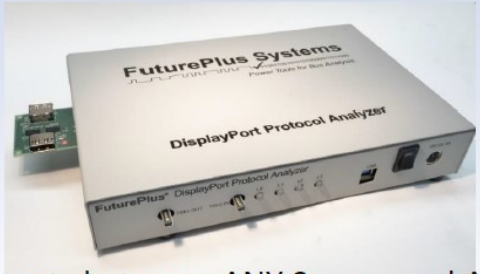


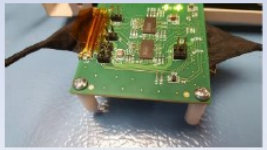
DisplayPort Protocol Analyzer In Action!

FuturePlus Systems

01100110011100000111001 1

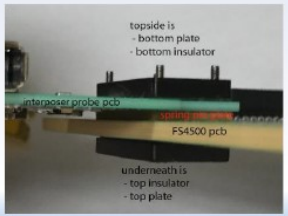
Advancing Technology Development





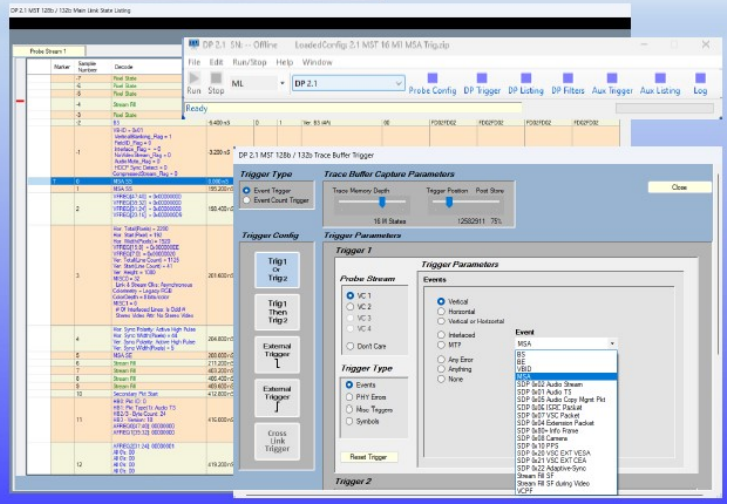
40 pin eDP Repeater

USB Type C Repeater



Regular DP Snooper

- Connects between ANY Source and ANY Sink
  - Supports 8b/10b, eDP, FEC/DSC, DP1.2b DP 1.4b, DP2.1
  - Supports 128b/132b DP2.1
  - Probe, Decode, and Time Correlate High Speed Main Link and Aux Channel
  - Snooper and Repeater Probing Solutions Available

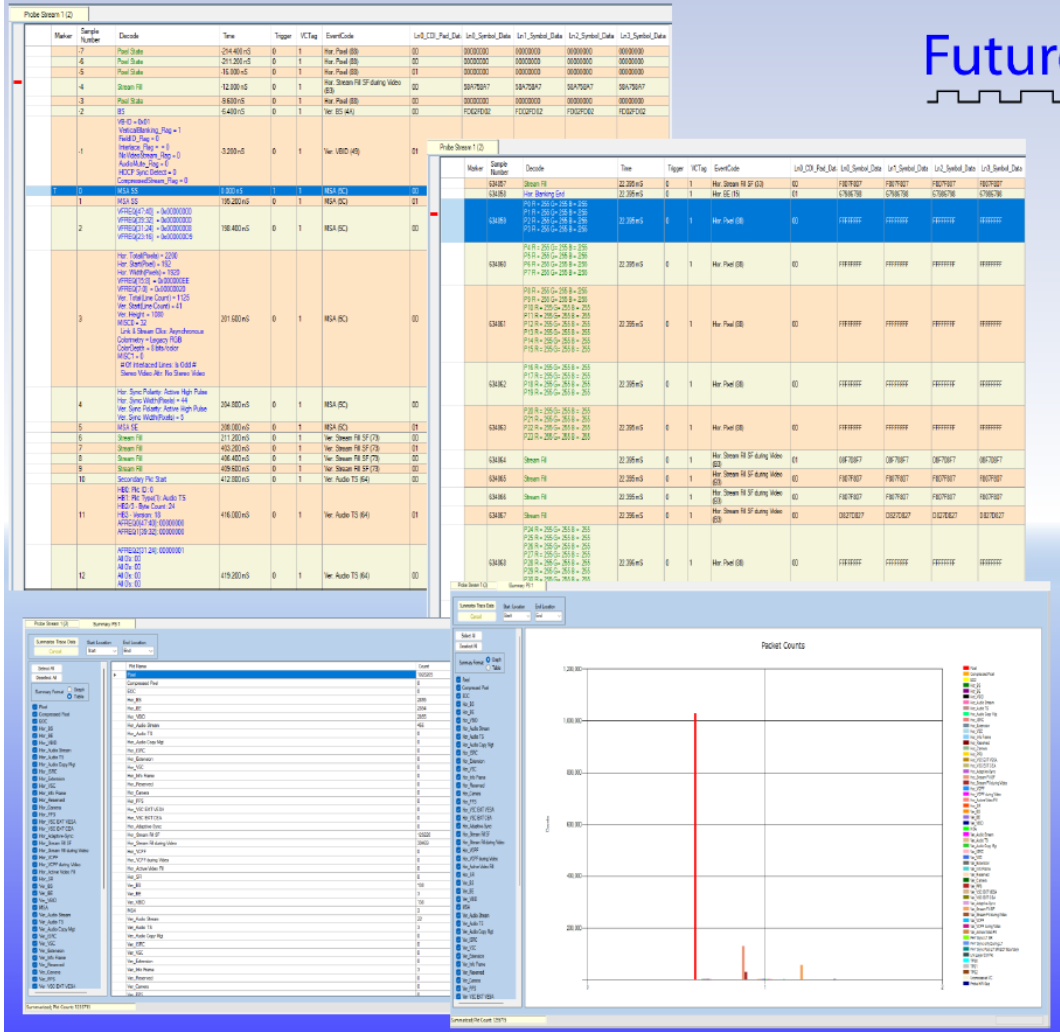


See our Rep in S.Korea

XDANA Technologies Inc.

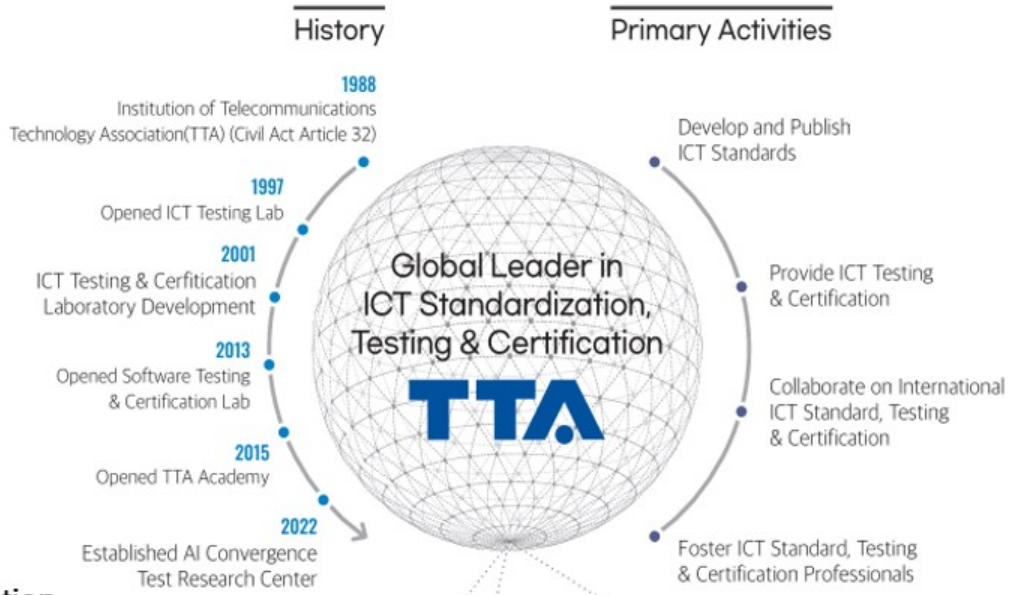
FuturePlus Systems

Advancing Technology Development



- DP 2.1 Color Bar Test
- 16 Million States
- Captured Complete Frame
- Data Includes video resolutions and frame settings shown in MSA.
- Detailed Decodes of SDP
- Decoded Pixel information
- 128/132 raw data traffic for each lane
- Summary Window containing all packet counts

Telecommunications Technology Association(TTA)



DP Test Contact Information

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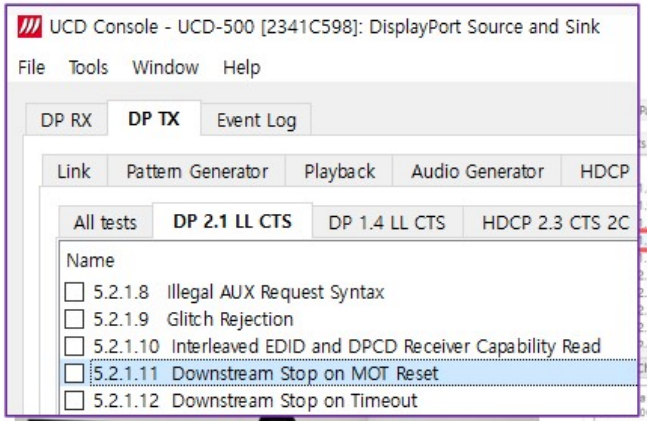
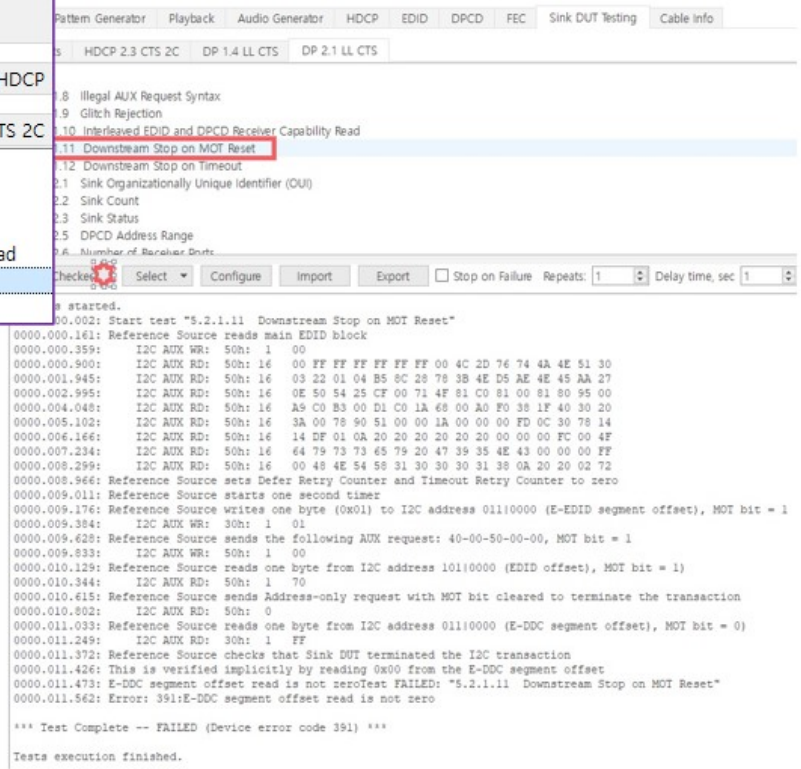
010-5111-1347, martin@tta.or.kr

Ms. Hye-Young Lee ,

010-5111-1020, h775275@tta.or.kr

DP 2.1 Sink Device Link Layer Demo :





UCD-500 Gen2 + Dell U3224KB Monitor

TELEDYNE LECROY

Everywhereyoulook™

Tel : 02-558-8833
Email : korea_marketing@teledynelecroy.com

Demo 1 at a glance

- DisplayPort Source/Sink PHY Compliance
  - Using SDA8000HD Serial Data Analyzer
  - QPHY-DP Automation
- You can see :
  - Compliance Test Setup details
  - Automated DP Source/Sink Compliance
  - Multi-Lane Analysis
    - TP2 & TP3 Eye Diagram
  - Embed/De-Embed Channels

Demo 2 at a glance

- DisplayPort Source/Sink PHY Compliance
  - Using WavePulser 40iX High-speed Interconnect Analyzer
  - Sink Channel Calibration
- You can see :
  - S-Parameter and TDR Measurement
  - How to measure the Insertion Loss
    - ISI channel measurement
  - 2X Thru to de-embed the Test Fixtures
  - Channel Emulation with Simulated/Capture waveforms

Thank you for attending the VESA Workshop Seoul Korea 2024