Welcome
VESA Workshop Taipei, Taiwan 2024

VESA Workshop Agenda

Time	Topic	Speaker
10:00am	VESA Overview and Standards Updates, Including DisplayPort v 2.1a and Display Panel Standards	Jim Choate, Compliance Program Manager
10:30am	DisplayPort Link Layer CTS v 2.1	Alok Soni, Software Lead, Teledyne LeCroy
11:00am	eDP and DP v 2.1 PHY CTS Overview and Updates	Abhijeet Shinde, Product Manager, Keysight Technologies
11:30am	DP Alt Mode v 2.1a Overview and CTS Updates	Mike Micheletti, Product Manager, Teledyne LeCroy
12:00pm – 1:00pm	Lunch	
1:00pm	VESA DisplayHDR Specification Overview and Test	Robert Yang, Granite River Labs
1:40pm	LRD/Active cable testing and DP 2.1 enhanced connector certification	Lexus Lee, Technical Program Manager, Allion Labs
2:15pm	UHBR DPTX and DPRX device design challenges	Jay Lin, Senior Technical Manager, Realtek
3:00pm – 3:15pm	Break	
3:15pm	VESA Compliance Program	Jim Choate, Compliance Program Manager
	Summary, Questions & Answers	
4:00pm – 4:30pm	Demo Stations Overview	

VESA Overview and Standards Updates

Jim Choate
VESA Compliance Program Manager
10/09/2024

Agenda

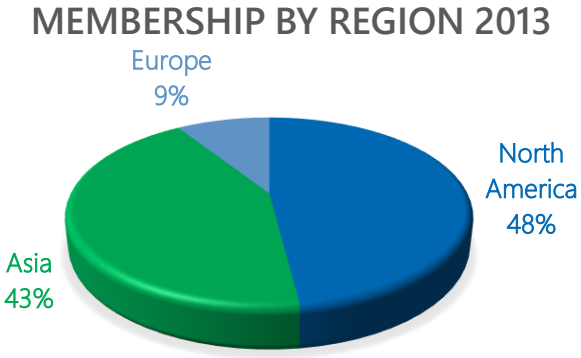
- VESA Overview
- DisplayPort Overview
- VESA Certified DisplayHDR, ClearMR and Adaptive-Sync
- VESA Technology Development Areas
- Summary

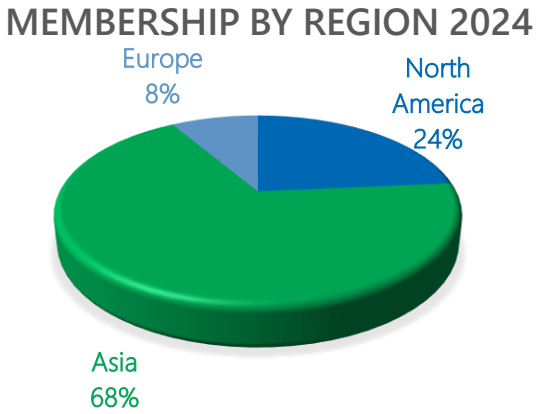
VESA OVERVIEW

About VESA

- A growing global industry alliance with nearly 340 members in 2024. Strong growth in membership over 10 years.
- Mission to develop, promote and support ecosystem of vendors and certified interoperable products for the electronics industry.
- *Develops OPEN standards, contribution is open to all companies at all stages of development*

VESA Membership Growth





Changes from 2013:
Asia + 25%

VESA Standards Enable Many Market Segments…

Monitors, PCs and laptops

Gaming consoles and headsets

Digital signage / kiosks

Smartphones and tablets

Automotive

Digital projectors

...As Well as Many Aspects of Display Technology

Display Interfaces

- DisplayPort
- Embedded DisplayPort
- DisplayPort Alt Mode (Native DisplayPort over USB-C connector)
- DisplayPort Tunneling (USB4 and Thunderbolt)
- Automotive Extensions Services (DP AE specification)

Display Data Compression

- Display Stream Compression (DSC)
- VESA Display Codec for Mobile (VDC-M)

Display Metrology

- Standardized Display Performance Measurement
- DisplayHDR Certification (High Dynamic Range)
- ClearMR Certification
- AdaptiveSync Display Certification

Display Capability Parameters

- DisplayID
- Extended Display Identification Data (EDID)
- Multi-Display Interface (MST)

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VESA Local Asian Support Capability

- VESA continues to provide local support to Asia to address growing regional membership needs
- China (Mainland) and Taiwan are the fastest growing areas for VESA's membership.
- **Kellen** is VESA's Representative in Asia
- This partnership provide members with a communication option in their native language. Kellen handles membership related activities including, new membership requests, renewals, event support and translation of VESA member messaging, etc.
- AsiaVESA@kellencompany.com or at +86 10 6580 0670

DisplayPort ™ Overview

DisplayPort Market Penetration

- DisplayPort adoption continues to grow in 2024
- DisplayPort and DisplayPort Alternate Mode over USB-C
  - The common monitor interface for personal computers
  - Supported on the USB-C interfaces
  - Mandated for USB4 and Thunderbolt
  - Automotive integration with DP AE specification
  - Mobile phones with USB-C
- Embedded DisplayPort (eDP)
  - ~95% penetration in notebook PCs, used in many high-end tablets and now automotive

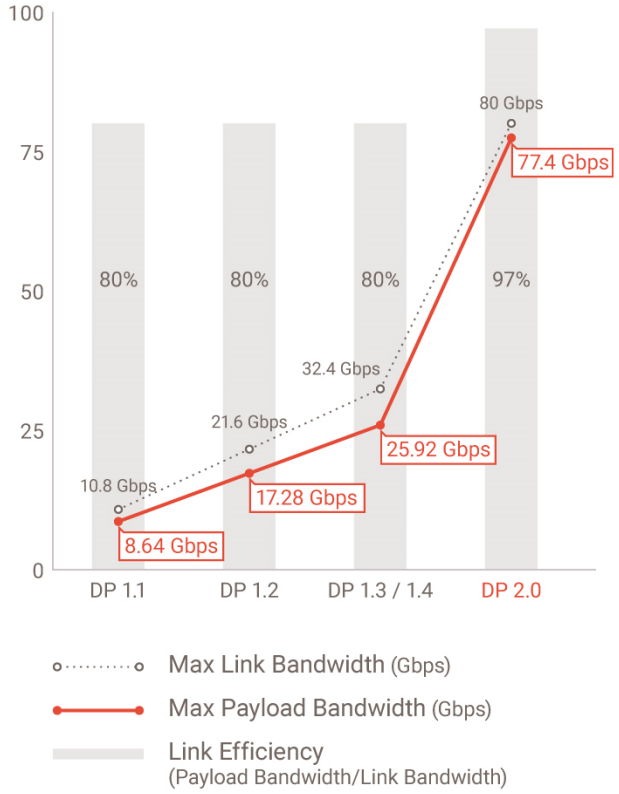
DisplayPort 2.1a Summary

- DisplayPort v2.1a was released in December 2023
- Major features added in **v2.0/v2.1/v2.1a**:
  - Added 128b/132b DP channel coding
  - Increase in data bandwidth performance (almost 3X) with new link rates up to 20 Gbps/lane
  - Panel Replay, similar to PSR (Panel Self Refresh) used for eDP
  - DSC support mandated
  - Enhanced DP connectors and cables (DP40 and DP80)
  - DP PHY specification alignment with USB4 PHY specification
  - Updated DP to HDMI v2.1 or higher protocol converter (PCON)
  - Corrects errata
  - Replaces DP40 cables with DP54 to expand higher rate cable length
  - Expanded Tunneling capability
  - Updates for DP AE Services specification

- DisplayPort **2.1a** enables up to 3X increase in video bandwidth performance vs DP **1.4**
- 3 new data rates added. UHBR10, UHBR13.5 and UHBR20 provides up to 80Gbps link bandwidth for 4 lanes at 20Gbps.
- First standard to support 8K resolution (7680 x 4320) at 60 Hz refresh rate with full-color 4:4:4 resolution, including with 30 bits per pixel (bpp) for HDR-10 support
- Beyond 8K resolutions achieved with maximum link rate to up to 20 Gbps/lane and more efficient 128b/132b channel coding

DisplayPort™

EVOLUTION OF DISPLAYPORT DATA BANDWIDTH



DisplayPort 2.1a Resolution Capability
(Single Display Examples)

Port Configuration	DisplayPort 1.4a	DisplayPort 2.1a
No Compression		
4 Lanes, max link rate	5K (5120x2800)@60fps 24bpp	10K (10240x4320)@60fps 24bpp
2 Lanes, max link rate	4K (3840x2160)@60fps 24bpp	8K (7680x4320)@30fps 30bpp
With Compression (DSC)		
4 Lanes, max link rate	8K (7680x4320)@60fps 30bpp	16K (15360x8460)@60fps 30bpp
2 Lanes, max link rate	5K (5120x2800)@60fps 24bpp	10K (10240x4320)@72fps 30bpp

Notes:

- 2 Lane configuration is common for USB-C DP Alt Mode
- All above modes assume full 4:4:4 color encoding
- 30bpp is required for DisplayHDR operation

Key:

- DSC = Display Stream Compression
- fps = frames per second
- bpp = bits per pixel

VESA Certified DisplayHDR, ClearMR and AdaptiveSync

VESA Display Performance Standards

VESA's display performance work group has been busy since the initial release of the DisplayHDR CTS in 2017.

- VESA Certified DisplayHDR r1.2 - *update covered by GRL*
- VESA Certified AdaptiveSync r1.1
- VESA Certified Clear Motion Ratio (CMR) r1.1

DisplayHDR Summary

- Industry's first open HDR specification for LCD and emissive (OLED/microLED) displays with a fully transparent testing methodology
- More than 3000 display models certified under logo program to date makes VESA Certified DisplayHDR one of the most successful logo programs in VESA history.
- More details available at https://displayhdr.org

VESA Defines New Standard to Help Speed PC Industry Adoption of High Dynamic Range Technology in Laptop and Desktop Monitor Displays

DisplayHDR is industry's first open HDR specification with a fully transparent testing methodology

SAN JOSE, Calif. – December 11, 2017 – The Video Electronics Standards Association (VESA®) today announced it has defined the display industry's first fully open standard specifying high dynamic range (HDR) quality, including luminance, color gamut, bit depth and rise time, through the release of a test specification. The new VESA High-Performance Monitor and Display Compliance Test Specification (DisplayHDR) initially addresses the needs of laptop displays ar

ClearMR Summary

- VESA developed motion blur performance compliance test specification for LCD and emissive (OLED/microLED) displays with a new Clear Motion Ratio (CMR) metric and fully transparent testing methodology
- More than 116 display models certified under ClearMR logo program to date
- More details available at https://www.clearmr.org/

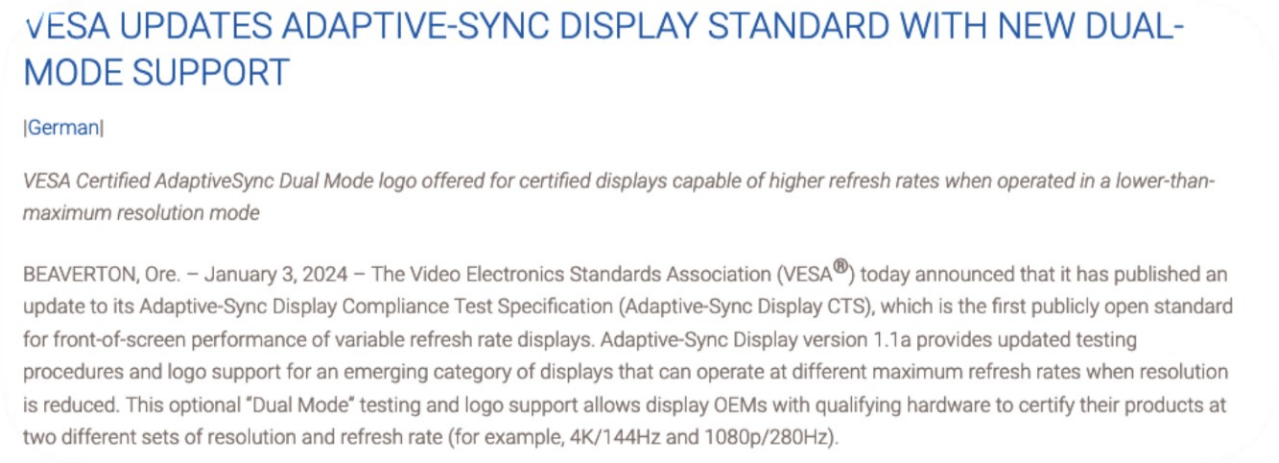
VESA BRINGS CLARITY TO MOTION BLUR IN DIGITAL DISPLAYS WITH NEW COMPLIANCE TEST SPECIFICATION AND LOGO PROGRAM

ClearMR specification and logo program provide consumers with a true quality metric for grading motion blur performance for LCD and OLED panels, TVs, desktop monitors and embedded displays

BEAVERTON, Ore. – August 22, 2022 – The Video Electronics Standards Association (VESA®) today introduced the ClearMR Compliance Test Specification (ClearMR), an industry standard and logo program that provides a new quality metric for grading motion blur in digital displays. ClearMR is applicable to both LCD and emissive display products, including display panels, TVs, monitors, and computers with embedded displays, such as all-in-ones, laptops, notebooks and tablets. The new metric Clear Motion Ratio (CMR), as

VESA Adaptive-Sync Display Summary

- Industry's first publicly open standard for front-of-screen performance of variable refresh rate displays.
- More details available at https://www.adaptivesync.org/



VESA UPDATES ADAPTIVE-SYNC DISPLAY STANDARD WITH NEW DUAL-MODE SUPPORT

|German|

VESA Certified AdaptiveSync Dual Mode logo offered for certified displays capable of higher refresh rates when operated in a lower-than-maximum resolution mode

BEAVERTON, Ore. – January 3, 2024 – The Video Electronics Standards Association (VESA®) today announced that it has published an update to its Adaptive-Sync Display Compliance Test Specification (Adaptive-Sync Display CTS), which is the first publicly open standard for front-of-screen performance of variable refresh rate displays. Adaptive-Sync Display version 1.1a provides updated testing procedures and logo support for an emerging category of displays that can operate at different maximum refresh rates when resolution is reduced. This optional "Dual Mode" testing and logo support allows display OEMs with qualifying hardware to certify their products at two different sets of resolution and refresh rate (for example, 4K/144Hz and 1080p/280Hz).

DP2.1 Compliance Tests

Name : Alok K. Soni

Company : Teledyne LeCroy

Date: 10/09/2024 (09-Oct-2024)

VESA Approved DP2.1 Compliance Tests Coverage:

Source Device Tests:	
AUX and HPD (4.2.1.x)	FEC (4.5.1.x)
EDID and DPCD (4.2.2.x)	DSC (4.6.1.x)
Link Training (4.3.1.x)	EDID and NDID (4.7.x)
Link Maintenance (4.3.2.x)	Adaptive Sync (4.8.x)
Video (4.3.3.x, 4.4.1.x and 4.4.2.x)	LTTPR (4.9.1.x)
Power Management (4.4.3.x)	
Audio (Under Review) (4.4.4.x)	

VESA Approved DP2.1 Compliance Tests Coverage:

Sink Device Tests:	
AUX(5.2.1.x)	Split SDP (5.4.5.x)
DPCD (5.2.2.x)	FEC (5.5.1.x)
Link Training (5.3.1.x)	DSC (5.6.x.x)
Link Maintenance (5.3.2.x)	EDID and NDID (5.7.x)
Video (5.4.1.x and 5.4.2.x)	Adaptive Sync (5.8.1.x)
Power Management (5.4.3.x)	LTTPR (5.9.1.x)
Audio (Under Review) (5.4.4.x)	

VESA Approved DP2.1 Compliance Tests Coverage:

LTTPR/Tunnel Device Tests:	(Loopback setup tests)
LTTPR Cap (7.1.1.x)	8b10b Non-LTTPR link Training (7.1.8.x)
8b10b Transparent link Training (7.1.2.x)	Link Maintenance (7.1.9.x)
8b10b Non-Transparent link Training (7.1.3.x)	DSC test for SST and MST (7.1.10.x)
128b132b Non-Transparent link Training (7.1.4.x)	HDCP test for SST and MST (7.1.11.x)
Symbol Error (7.1.5.x)	Split SDP (7.1.12.x)
8b10b FEC Error (7.1.6.x)	
128b132b FEC Error (7.1.7.x)	

VESA Approved SCRs Lists (Post DP-v2.1-Link-CTS-r1.0) :

SCR Name & Status:	Change Highlights:
Deprecate test 4.3.2.5, update tests 4.2.1.1, 4.2.1.2 and 7.1.1.4 (Approved)	4.3.2.5 Deprecated (lane count reduction) 4.2.1.1 and 4.2.1.2 extra time to retry 7.1.1.4 LTTPR expected value change for Reg 0xE and 0x220E
SCR to DP v2.1 Link CTS r1.0_multiple_comments_part1 (Approved)	4.2.2.13 and 4.2.2.14 for AUX Defer Retry check 7.1.4.8, 7.1.4.9 and 7.1.4.10 F0008 value validation. 5.4.3.1 and 5.4.3.2Time extended for check. 5.4.3.2 and 5.4.3.2 UHBR version of power management tests 5.6.3.7 DSC at max Pixel rate validation at UHBR Rate. 4.9.1.22 LTTPR First DPCD read F0000h to F0009h after Long HPD. 4.3.3.2 Typo correction and 4.6.1.x DSC source table CTS update.
Phase 7 Audio test update (GMR)	Audio tests update to include UHBR rate. Test Audio for both DSC and non compressed Video for up to UHBR rate.

VESA Approved SCRs Lists (Post DP-v2.1-Link-CTS-r1.0) :

SCR Name & Status:	Change Highlights:
SCR to DP v2.1 Link CTS r1.0_ Display ID ARVR HMD update (TGR)	Update/New Test (5.7.1.x and 5.7.2.x) to cover new version for ARVR HMD version.
SCR to DP v2.1 Link CTS r1.0_ Minimum HBlank_size and Vblank Period validation (TGR)	New test 5.7.14.7 to validate Hblank and Vblank for detail timing exposed in EDID/NDID.
Many more SCR pending: based on following document comments.	https://groups.vesa.org/wg/Test/document/20493

- Q/A

DisplayPort Electrical Testing Overview

Abhijeet Shinde
Keysight Technologies
10/09/2024

Agenda

- DP2.1a PHY Updates
- DP2.1a Electrical Compliance Test Requirements
- DP2.1a Transmitter Test
- DP2.1a Receiver Test
- eDP PHY Electrical Conformance Testing

DP2.1a PHY Updates

DP2.1 to DP2.1a Electrical Updates

- No changes in 8b/10b electrical compliance testing
- New DP54 Cable model for UHBR10 and UHBR13.5 Source testing
- Test Limit changes in Source and Sink testing

- UHBR10
  - DPTX TP2
    - Total Jitter =380 mUI
    - Data-Dependent Jitter =160 mUI
    - Eye Width = 600 mUI
    - Eye Height = 242 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 185 mV
  - DPTX TP3_EQ
    - Total Jitter =450 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 115 mV
  - DPRX TP3_EQ
    - Total Jitter =485 mUI
    - Data-Dependent Jitter =240 mUI
    - Eye Width = 540 mUI
    - Eye Height = 112 mV
- UHBR20
  - DPTX TP2
    - Total Jitter =435 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 240 mV
  - DPTX TP3_EQ
    - Total Jitter =455 mUI
    - Data-Dependent Jitter =210 mUI
    - Eye Width = 560 mUI
    - Eye Height = 100 mV
  - DPRX TP3_EQ
    - Data-Dependent Jitter =255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV

- UHBR10
  - DPTX TP2
    - Total Jitter =440 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 550 mUI
    - Eye Height = 162 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 200 mV
  - DPTX TP3_EQ
    - Total Jitter =515 mUI
    - Data-Dependent Jitter =245 mUI
    - Eye Width = 520 mUI
    - Eye Height = 80 mV
  - DPRX TP3_EQ
    - Total Jitter =530 mUI
    - Data-Dependent Jitter =260 mUI
    - Eye Width = 520 mUI
    - Eye Height = 73 mV
- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI

DP2.1a Electrical Compliance Test Requirement

DisplayPort Interface

Main Link

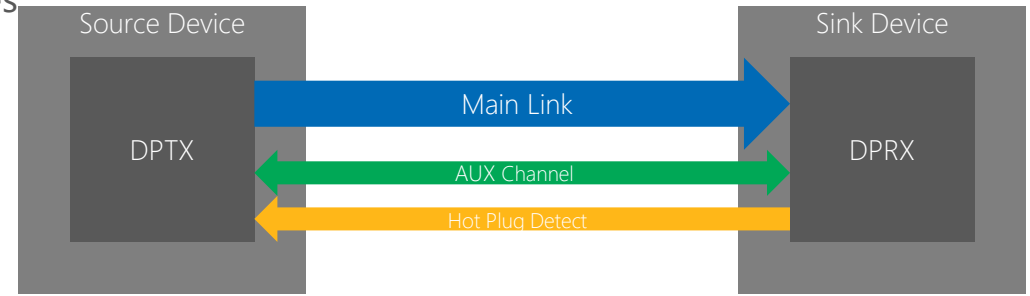
- Display data transfer
- 4 unidirectional high-speed lanes
- Multiple bitrates supported

AUX Channel

- Link management
- Test mode control
- 1 bidirectional low-speed lane

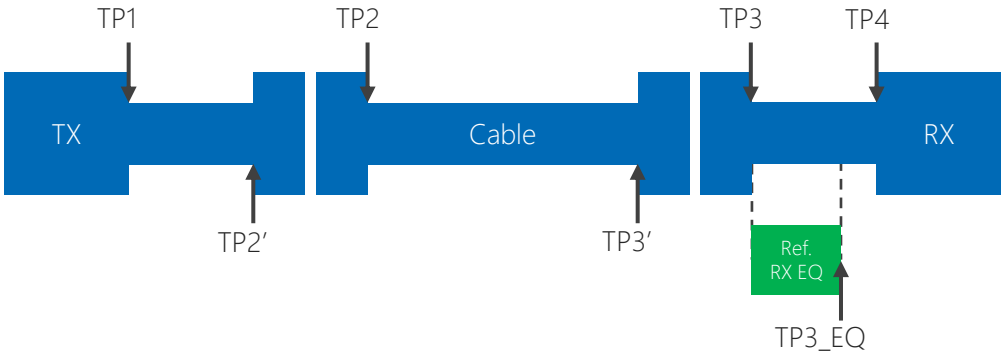
Hot Plug Detect

- Source detects presence of sink
- Sink notifies of status changes via IRQ



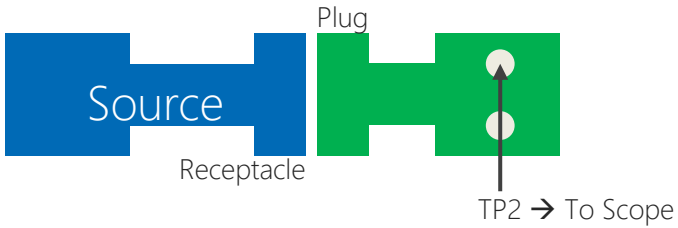
Test Points

Test Point	Definition
TP1	Source transmitter pins.
TP2	Test interface of a TPA, next to mated connection to a DP source.
TP2’	RX JTOL signal injection point for DUTs with plug.
TP2_CTLE	RX JTOL calibration and test point for DUTs with plug.
TP3	Test interface of a TPA, next to mated connection to a DP sink.
TP3’	Signal injection point to a DP sink.
TP3_EQ	TP3 using a defined cable model with equalization applied.’
TP3_CTLE	TP3 using a defined HBR3 cable model with CTLE applied.
TP3_DFE	TP3 using a defined HBR3 cable model with CTLE and DFE applied.
TP4	Sink receiver pins.

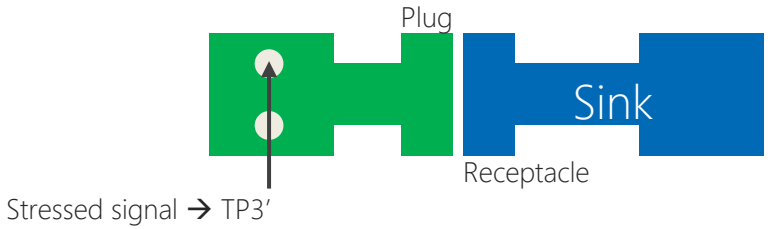


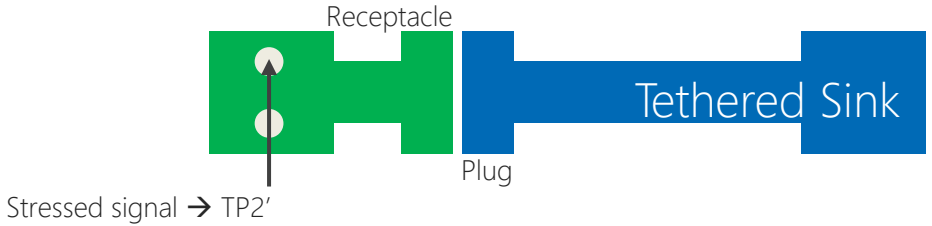
Test Point Access Examples

DPTX Testing



DPRX Testing





How to test the PHY layer?

Source

- Configure the source to output test patterns with certain drive settings → **AUX controller**
- Embed worst-case channels, apply equalization on the oscilloscope
- Run measurements

Sink

- Generate the stress signal with a pattern generator
- Guide the sink through Link Training → **AUX controller**
- Read built-in error counter → **AUX controller**

DP2.1a Transmitter Test

Electrical Transmitter Tests

Item	Name	Normative/ Informative
3.1	Eye Diagram Test	Normative
3.2	HBR/RBR Non-PE Level Verification Test	Normative
3.3	HBR/RBR PE Level Verification and Maximum Differential Peak-to-Peak Voltage Test	Normative
3.4	HBR3/HBR2 PE Level and Equalization Verification Test	Normative
3.5	HBR3/HBR2 $V_{TX\_DIFFp\text{-}p\_MAX}$ Test	Normative
3.6	Inter-pair Skew Test	Informative
3.7	Intra-pair Skew Test	Informative
3.8	AC Common Mode Noise Test	Informative
3.9	Non-ISI Jitter Measurement Test	Normative
3.10	HBR3 TX Differential RL Test	Informative
3.11	TJ/RJ/DJ Measurement Tests	Normative
3.12	Main-Link Frequency Compliance Test	Normative
3.13	Spread-spectrum Modulation Frequency Test	Normative
3.14	Spread-spectrum Modulation Deviation Test	Normative
3.15	dF/dT Spread-spectrum Deviation High-frequency Variation Test	Informative

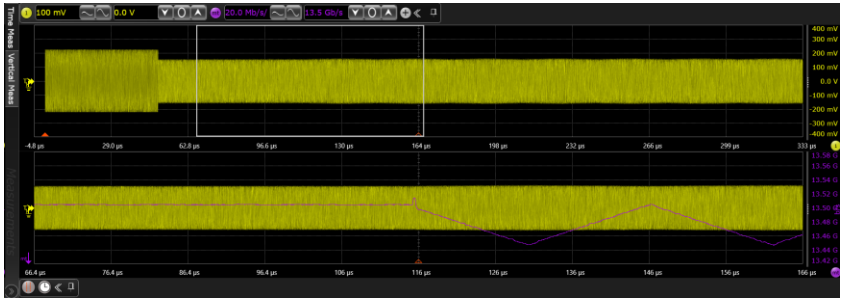
8b/10b

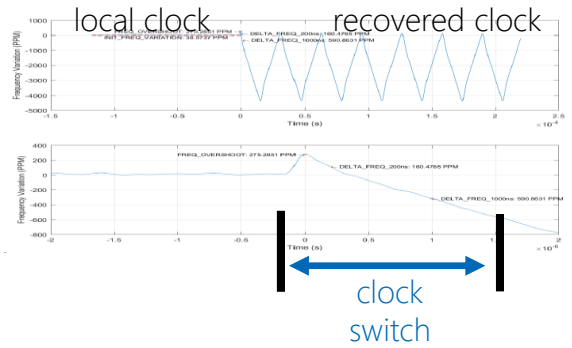
Item	Name	Normative/ Informative
4.2	Preset and CTLE-DFE Declaration	Normative
4.3	UHBR Source Transmitter Equalization	Normative
4.4	UHBR Bit Rate	Normative
4.4	UHBR Unit Interval	Informative
4.5	UHBR SSC Down Spread Range, Rate, Phase Deviation, and Slew Rate	Normative
4.6	UHBR Embedded Re-timer Frequency Variation	Normative
4.7	UHBR TP2 Eye at 1E-6 BER	Normative
4.8	UHBR TP2 Jitter at 1E-9 BER	Normative
4.9	UHBR AC Common Mode Nosie Test	Informative
4.10	UHBR TP3_EQ Eye at 1E-6	Normative
4.11	UHBR TP3_CTLE Jitter at 1E-9	Informative
4.12	UHBR Transmitter Return Loss	Informative

128b/132b

LTTPR Frequency Variation Test

- LTTPRs are needed as total channel loss increases with the PHY rate
  - Longer channel
  - More complex link training
- LTTPR Re-timer Clock Switch Test Mode
  - DPCD 0x0010B – 0x0010Eh [7] =1
- Initial Test Challenges
  - Entering Clock Switch test mode
  - Triggering on LTTPR local clock event





DP TX testing challenges

- The test time for DP TX is significant
- DP Source not supporting PHY Test Automation
  - DP Source does not transmit the compliance pattern

DP2.1a Receiver Test

Electrical Receiver Tests

Item	Name	Normative/ Informative
5.1	8b/10b DP Sink JTOL Test	Normative

Item	Calibration Point	Name
5.1.3.1.1	TP1-TP3	HBR3 Jitter Calibration
5.1.3.1.2	TP1-TP3	HBR2 Jitter Calibration
5.1.3.1.3	TP1-TP3	HBR Jitter Calibration
5.1.3.1.4	TP2/TP3	HBR3 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR2 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR Eye Height and Total Jitter Calibration
5.1.3.1.5	TP1/TP3	HBR3/HBR2/HBR Crosstalk Calibration
5.1.3.2	TP2/TP3	RBR Jitter Calibration
5.1.3.2	TP3	RBR Eye Height Calibration
5.1.3.2.1	TP3	RBR Crosstalk Calibration

Item	Name	Normative/ Informative
6.1	128b/132b DP UHBR Sink JTOL Test	Normative

Item	Calibration Point	Name
6.1.3.1.4.1	TP1	AC Common-Mode Interference Calibration
6.1.3.1.4.2	TP1	Random Jitter Calibration
6.1.3.1.4.3	TP1	Periodic Jitter Calibration
6.1.3.1.4.4	TP1	Total Jitter Calibration
6.1.3.1.4.5	TP1	Eye Height Calibration
6.1.3.1.5	TP3	Insertion Loss Calibration
6.1.3.1.6	TP3	Eye Diagram Calibration

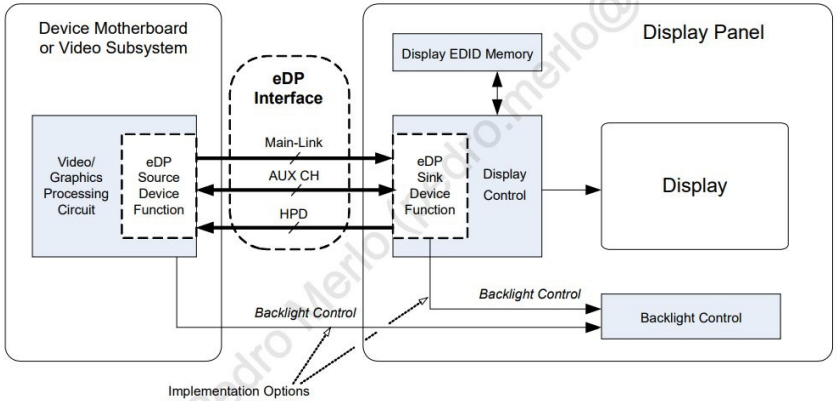
DP RX testing challenges

- DP Sink does not enable error count registers
- DP RX Preset calibration to be required – impacts TE correlation results
- Calibrations take a significant amount of time
  - Different setup needs for 8b/10b and 128b/132b

Embedded DisplayPort

eDP

- Standardized features and interoperability guidelines
  - Feature set determined by the system integrator
- Current specification is eDP1.5a
  - Based on DP1.4a
- No compliance program = Conformance Test!!



Key Differences eDP1.5 vs DP2.1a 8b/10b rates

Required

- DPCD registers for eDP
- Reduced AUX timing
- Enhanced framing
- Fast link training (sink)
- eDP-specific sink noise/jitter budget, reference EQ

Optional

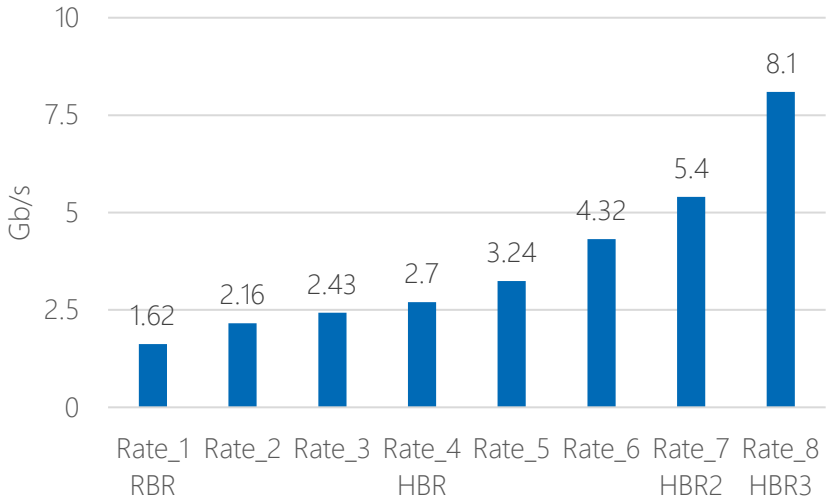
- Low AUX voltage swing
- Source detection by way of AUX CH
- STREAM_STATUS_CHANGED bits support
- GUID registers support
- Fast link training (host)
- Reduced main-link voltage swing level
- EDID
- HPD pin on sink device

Recommended

- Fewest number of lanes possible

Main Link Differences

- Eight nominal rates
- Custom rates supported



- TP3_EQ total jitter budget
- BER = 10^{-9}

Test Point	Description	I/N	DJ_{MAX}	TJ_{MAX}
TP1	eDPTX package pin	Informative	0.17 UI	0.27 UI
TP2	Source device eDP cable connector	Informative	N/A	N/A
TP3	Sink device (panel) eDP cable connector	-	-	-
TP3_EQ	**After reference RX equalizer**	**Normative**	**0.41 UI**	**0.50 UI**
TP4	eDPRX package pins	Informative	0.46 UI	0.55 UI

AUX Channel Differences

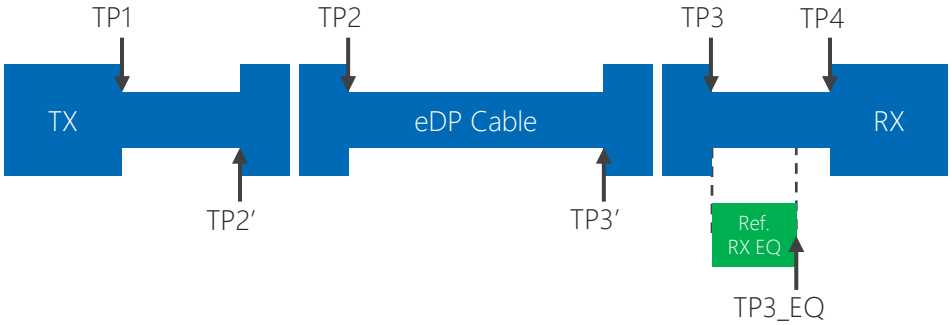
- No AC-coupling capacitors on Sink device side
- No pull-up/-down resistors
- Why?
  - The Sink device does not monitor the common mode voltage on AUX_CH_P and AUX_CH_N for Source device Hot Plug/Unplug and powered/unpowered detection

eDP Electrical Specification

- Low voltage swing levels
- Framework to apply optional customized voltage swings
- Reduced RX differential voltage sensitivity
- New transfer rates
- Framework to apply jitter specifications to optional customized frequencies
- Same Link Training procedures and voltage swing tables like DP, but with lower signal voltages

eDP Transmitter Test

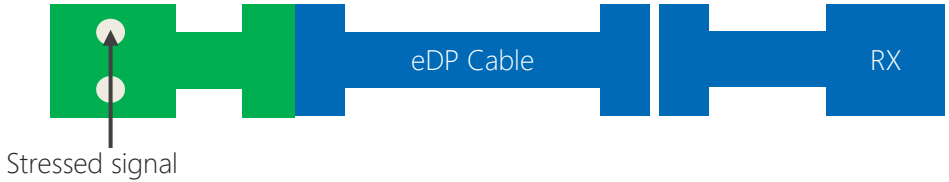
- Test Point/Fixture

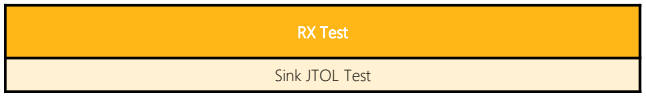


Recommended Source Main-Link TX Electrical Specification
Link Rate
Unit Interval
Total Jitter
Residual ISI
Non-ISI
Eye Diagram

eDP Receiver Test

- Test Point/Fixture





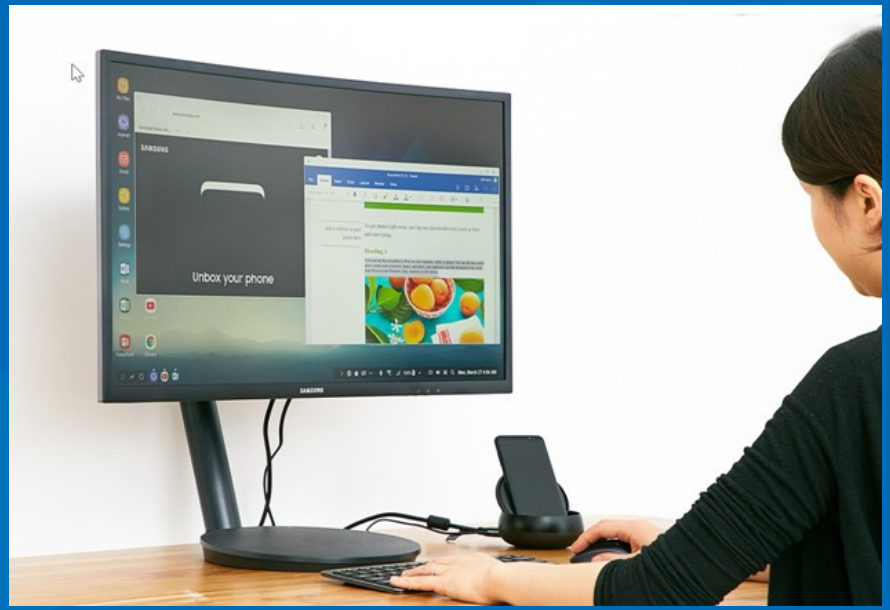
Calibration Point	RX Calibration
TP1	Sinusoidal Jitter Calibration
TP1	Random Jitter Calibration
TP3	Residual ISI
TP3	Eye Diagram
TP3	Crosstalk

eDP2.0 Update

- eDP2.0 draft v0.7 published on Aug 29, 2024
- Supports 128b/132b encoding
- Supports UHBR data rates
  - UHBR10, UHBR13.5 and UHBR20
- Leverages worst-case end-to-end link budget from DP2.1a

Thank You!

DP Alt-Mode 2.1: A Closer Look



Mike Micheletti
Product Manager
Teledyne LeCroy

10/09/2024

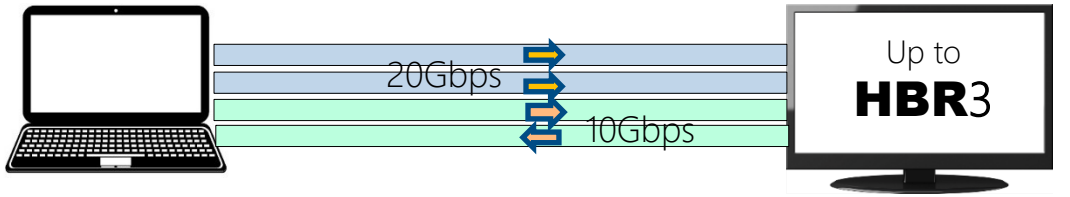
A Closer Look at DP Alt-Mode 2.1

- Agenda
  - DisplayPort 2.1 & Alt Mode Updates
    - DP Alt Mode Overview
    - Type-C pin configurations
  - DPAM 2.1 Version Resolution
  - DPAM 2.1 Cable Discovery
  - DPAM 2.1 Configuration walk-through
  - DPAM 2.1 Compliance Overview

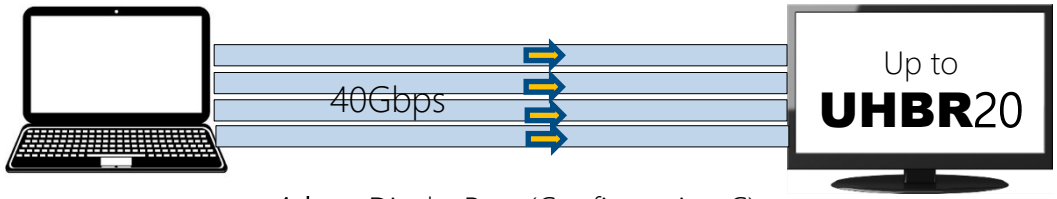
Alternate-Mode Usage Cases

- Alternate Modes
  - Goal – Leverage multi-lane Type-C cable to support alternate communications standards over a single physical cable
- Applications
  - DisplayPort 1.4 / 2.1
  - Thunderbolt™ 3

DP Alt-mode Lane Configurations



2-lane DisplayPort & **2-lane** USB (Configuration D)



4-lane DisplayPort (Configuration C)

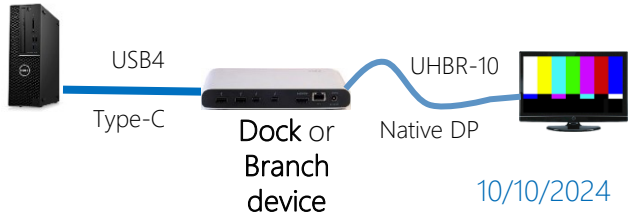
USB 3.2 DisplayPort Native

- Two diff pairs allow up to HBR3 (config: D)
- Four diff pairs allow up to UHBR20 (config: C, E)

DisplayPort 2.1 & DPAM 2.1 Updates

What is new in DisplayPort 2.1 Base Spec

- **DP56/DP80–** Allows UHBR20 ‘native’ DP cables/connectors
- **Active Cables** (LTTPR Retimer / LRD)
- **USB4 PHY** Electrical specification alignment (IR-loss…etc)
  - USB4 tunnel changes for UHBR rates
- **Revised Link Training -** DPCD registers as LTTPR “Intra-Hop AUX”
- **AUX-less ALPM** - Power management control over high-speed lines
- **CableID** allows DP-Tx/DP-Rx to identify DP56 / DP80 cables
- Lots of Clarifications and improvements



What is new in DisplayPort 2.1 Base Spec

- **DP56/DP80–** Allows UHBR20 ‘native’ DP cables/connectors
- **Active Cables** (LTTPR Retimer / LRD)
- **USB4 PHY** Electrical specification alignment (IR-loss…etc)
  - USB4 tunnel changes for UHBR rates
- **Revised Link Training -** DPCD registers as LTTPR “Intra-Hop AUX”
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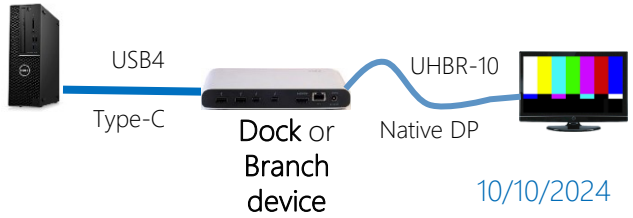
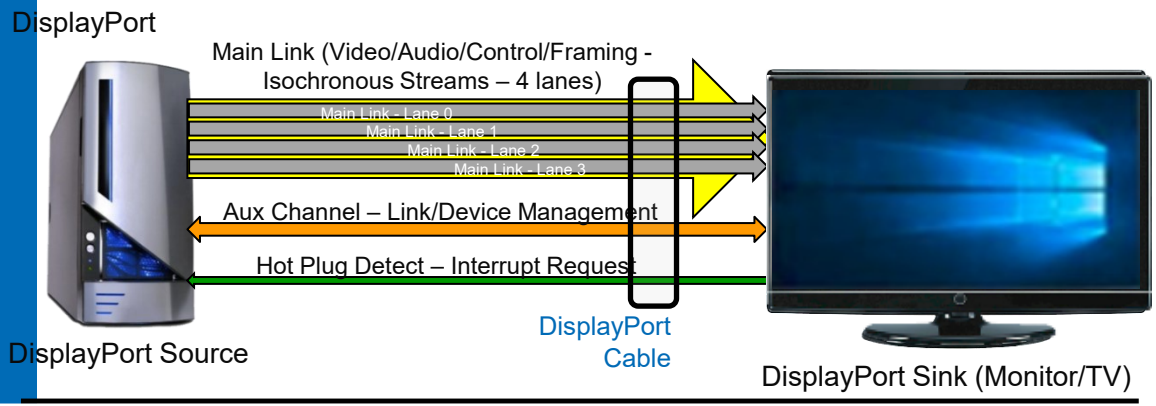
- **CableID** allows DP-Tx/DP-Rx to identify DP56 / DP80 cables
- Lots of Clarifications and improvements

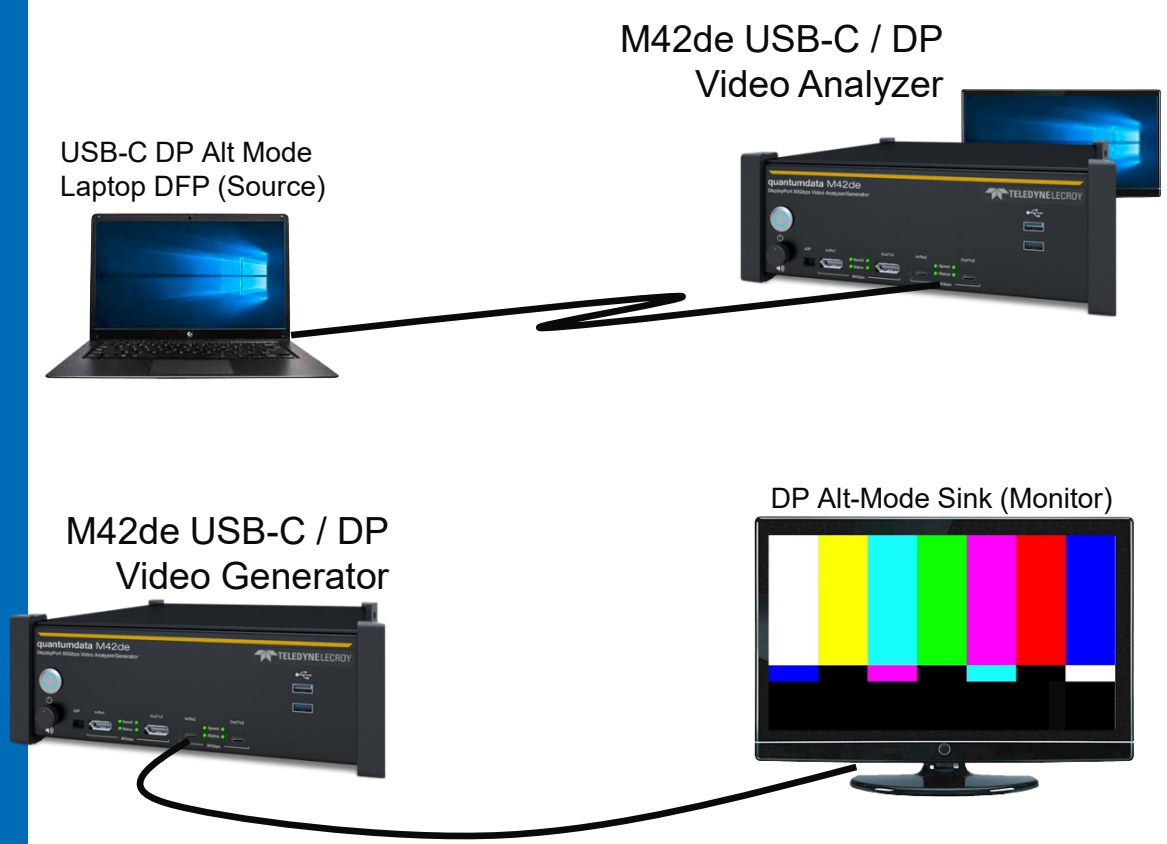


USB-C DP Alt Mode Signaling



- Main Link: high-bandwidth channel used to transport video/audio
  - 1, 2 or 4 Lane Configurations
  - Link rates:1.62Gbps – 20Gbps
- Aux Channel:
  - Bidirectional 1Mbps
- Hot plug signal:
  - Connection Detection
  - Interrupt mechanism

M42de Supports DP Alt-Mode SRC/SNK Testing

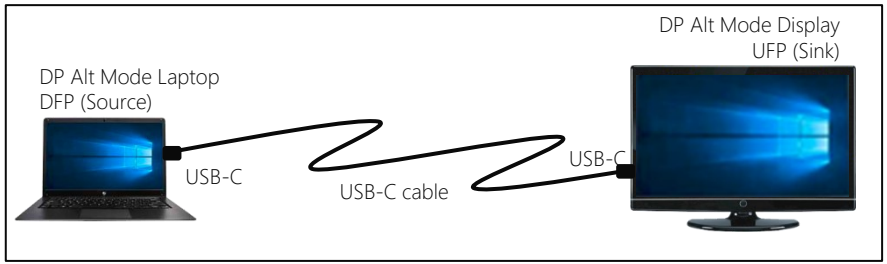


- Protocol Analysis - Source Testing
  - Sink emulation EDID, DPCD.
  - Protocol Analysis – Main Link & Aux
  - Compliance Testing - Link Layer, (including FEC), DSC, HDCP.
- Video Generation - Sink Testing
  - Source emulation and Link Training control.
  - Video Pattern Testing –generation of Display Stream Compression (DSC) Panel Replay and FEC.
  - Compliance Testing (Link Layer, FEC, HDCP).
- DP Alt Mode Testing
  - Run all VESA source and sink testing through the USB-C DP Alt Mode ports.

USB-C DP Alt Mode – High Level Overview

Key roles for PD/CC messages:

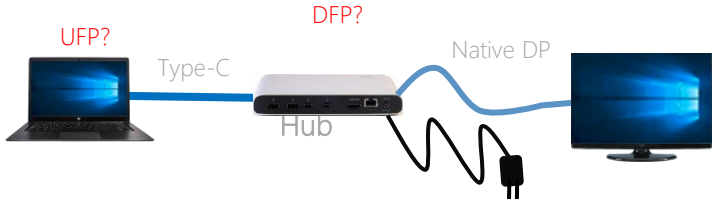
1. Discovery DP Alt Mode Capabilities
2. Decide which Pin Configuration to use
   - DP Sink
   - Active cables

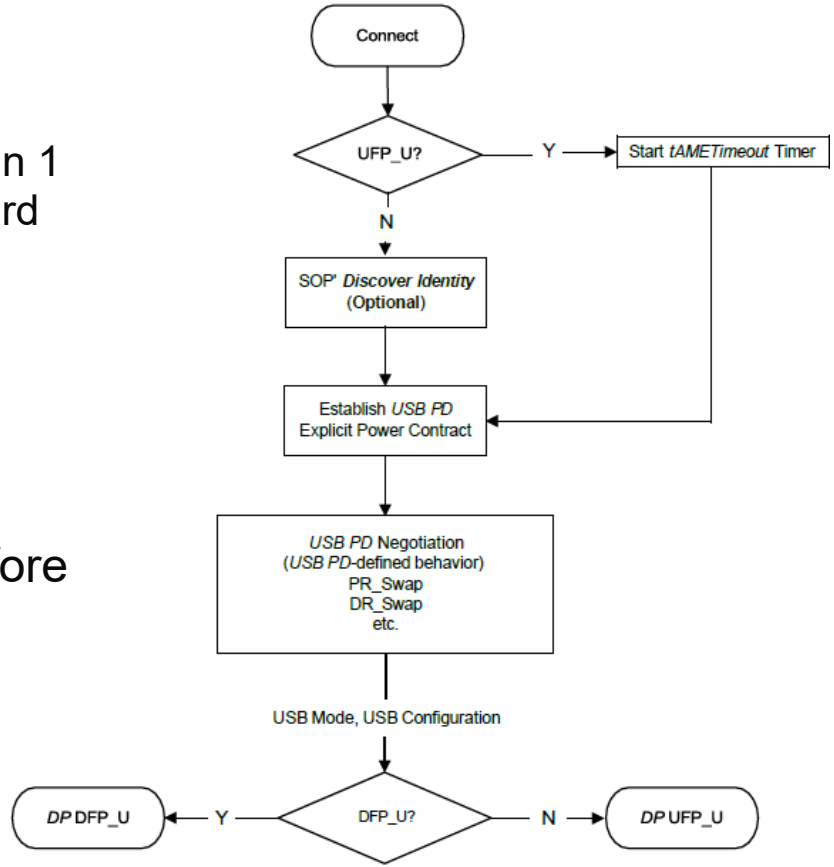


- Captures PD and AUX–
  - Sequential list of transactions
  - Shows full DP-Alt Mode entry flow
  - Captures all AUX channel transactions
  - Real-time

Getting Ready for DP Alt Mode…

- Initial Type-C State Detection
  - ***Starts tAMETimeout*** timer
    - If Sink does not enter DP Alt Mode within 1 Sec UFP_U shall present a USB billboard
- Negotiate initial PD Power Contract
- Establish port's data role
  - Port assumes the role of either:
    - DFP_U
    - UFP_U
- Complete any other PD transactions before starting DisplayPort Alt Mode (ie: PR_Swap)





DPAM 2.1 Version Resolution

Key Changes: DISCOVER MODE Response

DPAM Version[j]	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

SOP

DPAM2.0

Table 5-5: DP Capabilities (VDO in the Responder *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED. 01b = DP Sink device-capable (including DP Branch device). 10b = DP Source device-capable (including DP Branch device). 11b = Both DP Source and Sink device-capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP Standard* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = DP interface is presented on a USB-C plug. 1 = DP interface is presented on a USB-C receptacle.
7	*USB 2.0* Signaling Not Used	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)	00000000b = DP Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c,d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	00000000b = DP Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c,g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
31:24	RESERVED	RESERVED (always 00b).

DPAM2.1

Table 5-5: DP Capabilities (VDO in the Responder USB PD *Discover Modes*

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED 01b = *DP* Sink device-capable (including *DP* [illegible]evice). 10b = *DP* Source device-capable (including [illegible] device). 11b = Both *DP* Source and Sink device-cap[illegible]
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP* bit rates and electr[illegible]gs (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED X1XXb = RESERVED 1XXXb = RESERVED
6	Receptacle Indication	0 = *DP* interface is presented on [illegible] plug. 1 = *DP* interface is presented [illegible]*C* receptacle.
7	USB 2.0 Signaling Not Used	0 = *USB 2.0* may be needed [illegible] A7 –or– B6 – B7 while in DisplayPort Configura[illegible] 1 = *USB 2.0* is not needed [illegible] – A7 –or– B6 – B7 while in DisplayPort Configu[illegible]
15:8	DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)	00000000b = *DP* Sour[illegible]ce pin assignments are not supported. XXXXXXX1b = R[illegible]VED. XXXXXX1Xb = R[illegible]VED. XXXXX1XXb = [illegible]Assignment C is supported.[b] XXXX1XXXb = [illegible]n Assignment D is supported.[c,d] XXX1XXXXb = [illegible] Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	00000000b = *DP* Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c,g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
29:24	RESERVED	RESERVED (always 00b).
31:30	DPAM Version[i]	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

SOP'

DPAM2.0

SOP' Cable DP Capabilities (DPAM2.0)		
Bits	Field	CTS Value
B31-24	Reserved	0000 0000b
B23-16	DP Sink Device Pin Assignment Supported	0000 1100b
B15-8	DP Source Device Pin Assignment Supported	0000 1100b
B7-6	Reserved	00b
B5-2	Signal for Transport of DP Protocol	0001b
B1-0	Reserved	00b

DPAM2.1

Bit(s)	Description	Values
1:0	RESERVED	RESERVED (always 00b).
5:2	Signaling for Transport of DisplayPort Protocol[b]	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1Xb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[c]
7:6	RESERVED	RESERVED (always 00b).
15:8	DP Source Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported. 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
23:16	DP Sink Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
25:24	RESERVED	RESERVED (always 00b).
26[d]	UHBR13.5	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[e]
27	RESERVED	RESERVED (always 0).
29:28[f]	Active Component	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30	DPAM Version	00b = Original version. 01b = Version 1.

Discover Modes Response from UFP

Discover Modes Response from Cable

Key Changes: DISCOVER MODE Response

Discover ID and *Discover Modes* (DP Capabilities) Response

will be identified by having a non-zero value in bits 31:24 of the VDO. The DFP_U shall examine the list of modes returned until it finds 0s in bits 31:24 of the VDO and a non-zero value in bits 23:0 of the VDO (i.e., DisplayPort capabilities). The DFP_U and UFP_U shall use the corresponding offset (indexed from 1) as the Object Position in the Enter Mode, DisplayPort Configure, DisplayPort Status Update, Attention, and Exit Mode commands.

SOP

DPAM2.0

Table 5-5: DP Capabilities (VDO in the Responder *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED. 01b = DP Sink device-capable (including DP Branch device). 10b = DP Source device-capable (including DP Branch device). 11b = Both DP Source and Sink device-capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP Standard* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = DP interface is presented on a USB-C plug. 1 = DP interface is presented on a USB-C receptacle.
7	*USB 2.0* Signaling Not Used	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)	00000000b = DP Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	00000000b = DP Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
31:24	RESERVED	RESERVED (always 00b).

DPAM2.1

Table 5-5: DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED. 01b = *DP* Sink device-capable (including *DP* Branch device). 10b = *DP* Source device-capable (including *DP* Branch device). 11b = Both *DP* Source and Sink device-capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1Xb = RESERVED. 1Xb = RESERVED.
6	Receptacle Indication	0 = *DP* interface is presented on a *USB-C* plug. 1 = *DP* interface is presented on a *USB-C* receptacle.
7	USB 2.0 Signaling Not Used	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
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23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	00000000b = *DP* Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
29:24	RESERVED	RESERVED (always 00b).
31:30	DPAM Version[i]	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Discover Modes Response from UFP

SOP'

DPAM2.0

SOP' Cable DP Capabilities (DPAM2.0)		
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B23-16	DP Sink Device Pin Assignment Supported	0000 1100b
B15-8	DP Source Device Pin Assignment Supported	0000 1100b
B7-6	Reserved	00b
B5-2	Signal for Transport of DP Protocol	0001b
B1-0	Reserved	00b

DPAM2.1

Bit(s)	Description	Values
1:0	RESERVED	RESERVED (always 00b).
5:2	Signaling for Transport of DisplayPort Protocol[b]	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1Xb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[c]
7:6	RESERVED	RESERVED (always 00b).
15:8	DP Source Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported. 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
23:16	DP Sink Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
25:24	RESERVED	RESERVED (always 00b).
26[d]	UHBR13.5	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[e]
27	RESERVED	RESERVED (always 0).
29-28[d]	Active Component	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30	DPAM Version	00b = Original version. 01b = Version 1.

Discover Modes Response from Cable

Structured VDM Version

- SVDM Version Revised in Power Delivery Spec (Revision 1.3; Version 1.6)
  - Adds Major & Minor “VDM” version fields

Table 5-4: SVDM Header

Bit(s)	Description	Values
4:0	**Command**	0h = RESERVED, shall not be used. 1h = *USB PD* ***Discover Identity***. 2h = *USB PD* ***Discover SVIDs***. 3h = *USB PD* ***Discover Modes***. 4h = ***Enter Mode***. 5h = ***Exit Mode***. 6h = *USB PD* ***Attention***. 7h – Fh = RESERVED, shall not be used. 10h = ***DisplayPort Status Update***. 11h = ***DisplayPort Configure***. 12h – 1Fh = RESERVED for DP_SID use.
12:11	**Structured VDM Version (Minor)[a]**	Version number (Minor) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier 01b = Version 2.1 All other values are RESERVED.
14:13	**Structured VDM Version (Major)[a]**	Version number (Major) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier. 01b = Version 2.x. (x indicates SVDM minor version) All other values are RESERVED.
15	**VDM Type**	1 = SVDM.
31:16	**Standard or Vendor ID (SVID)**	Base SID (for a *USB PD* ***Discover SVIDs*** Command request) or DP_SID, a 16-bit unsigned integer, assigned by the USB-IF.

RESERVED (always 0).

00b = REQ (Request from Initiator Port).
01b = ACK (*USB PD* Responder ACK response).
10b = NAK (*USB PD* Responder NAK response).
11b = BUSY (*USB PD* Responder BUSY response).

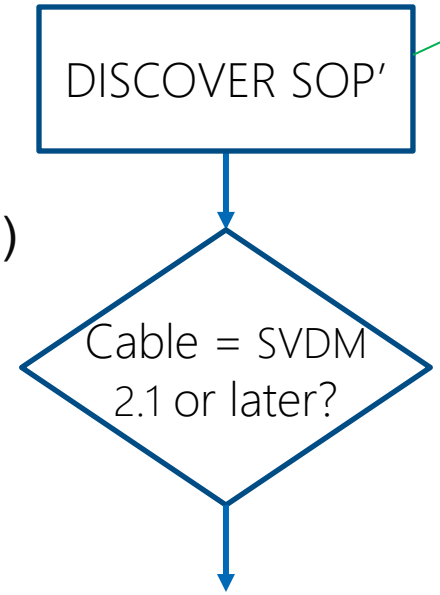
For ***Enter Mode*** Command requests/responses, ***Exit Mode*** Command requests/responses, and *USB PD* ***Attention*** Command requests:
- 000b = RESERVED.
- 001b – 110b = Index into the list of Vendor Defined Objects (VDOs) to identify the needed Mode VDO.
- 111b = Exit all Active Modes (equivalent of a power-on reset). Shall only be used with an ***Exit Mode*** Command request.

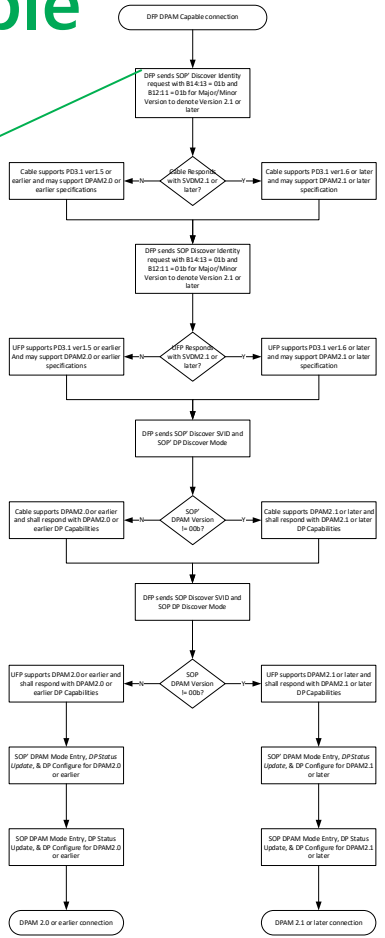
For *USB PD* ***Discover Identity***, ***Discover SVIDs***, and ***Discover Modes*** Command requests/responses:
- 000b.
- 001b – 111b = RESERVED.

- SVDM Minor: 2.0 = *DP Alt mode 2.0*
- SVDM Minor: 2.1 = *DP Alt mode 2.1*

SVDM Version Resolution Example

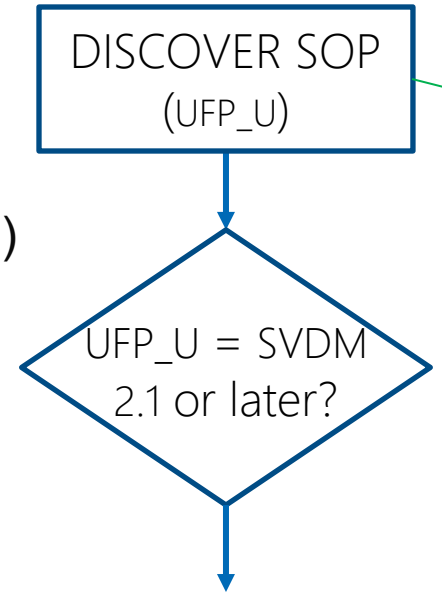
- SVDM Version resolution
  - DISCOVER IDENTITY (SOP'/ UFP)
  - DISCOVER SVIDs (SOP'/ UFP)
  - DISCOVER MODES (SOP'/ UFP)
    - DFP_U sends Discover Modes IF response "SVDM version = 2.1" then use "DPAM 2.1"
    - Else must use "DPAM 2.0"
  - ENTER MODE (SOP'/ UFP)
  - DP CONFIGURE (SOP'/ UFP)

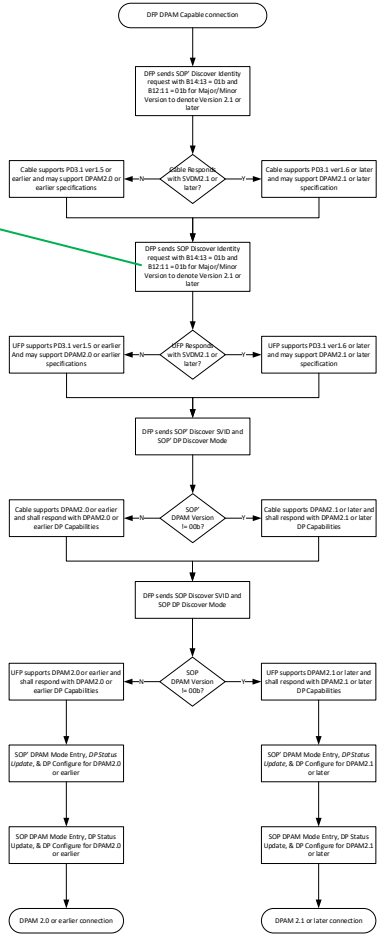




SVDM Version Resolution Example

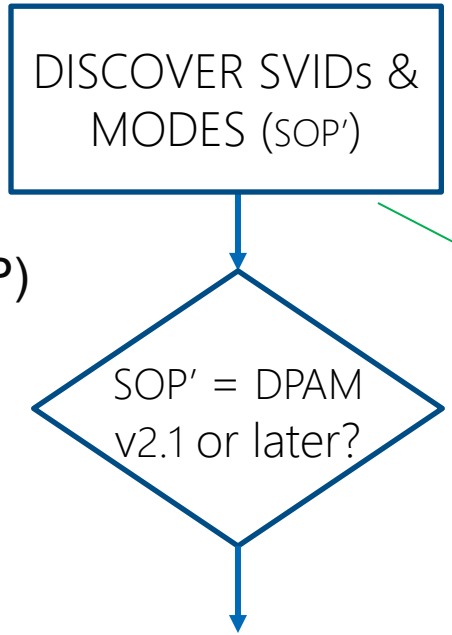
- SVDM Version resolution
  - DISCOVER IDENTITY (SOP'/ UFP)
  - DISCOVER SVIDs (SOP'/ UFP)
  - DISCOVER MODES (SOP'/ UFP)
    - DFP_U sends Discover Modes IF response "SVDM version = 2.1" then use "DPAM 2.1"
    - Else must use "DPAM 2.0"
  - ENTER MODE (SOP'/ UFP)
  - DP CONFIGURE (SOP'/ UFP)

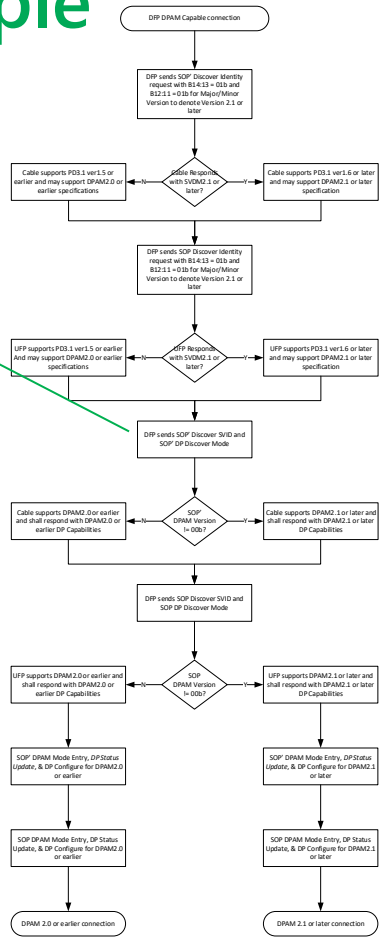




SVDM Version Resolution Example

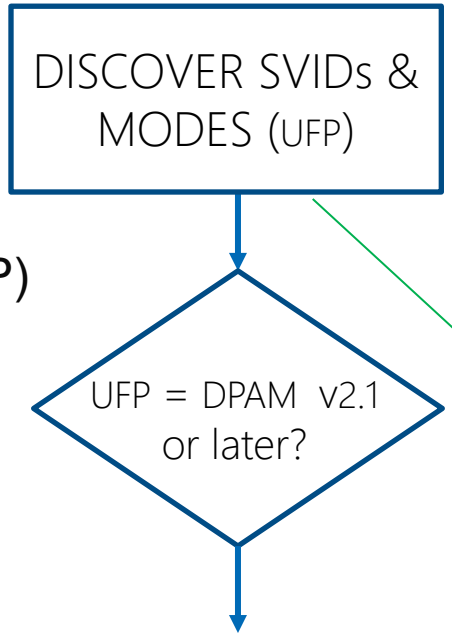
- SVDM Version resolution
  - DISCOVER IDENTITY (SOP'/ UFP)
  - DISCOVER SVIDs (SOP'/ UFP)
  - DISCOVER MODES (SOP'/ UFP)
    - DFP_U sends Discover Modes IF response "SVDM version = 2.1" then use "DPAM 2.1"
    - Else must use "DPAM 2.0"
  - ENTER MODE (SOP'/ UFP)
  - DP CONFIGURE (SOP'/ UFP)





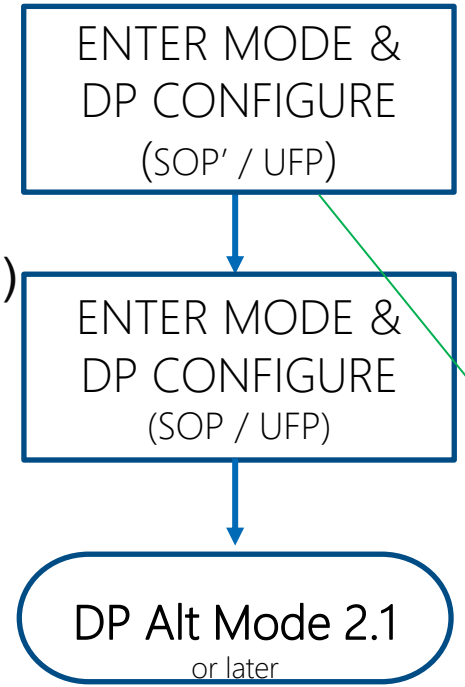
SVDM Version Resolution Example

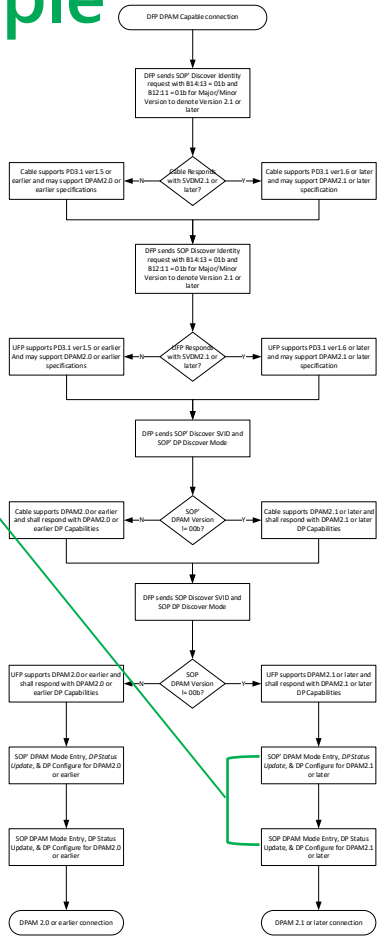
- SVDM Version resolution
  - DISCOVER IDENTITY (SOP'/ UFP)
  - DISCOVER SVIDs (SOP'/ UFP)
  - DISCOVER MODES (SOP'/ UFP)
    - DFP_U sends Discover Modes IF response "SVDM version = 2.1" then use "DPAM 2.1"
    - Else must use "DPAM 2.0"
  - ENTER MODE (SOP'/ UFP)
  - DP CONFIGURE (SOP'/ UFP)



SVDM Version Resolution Example

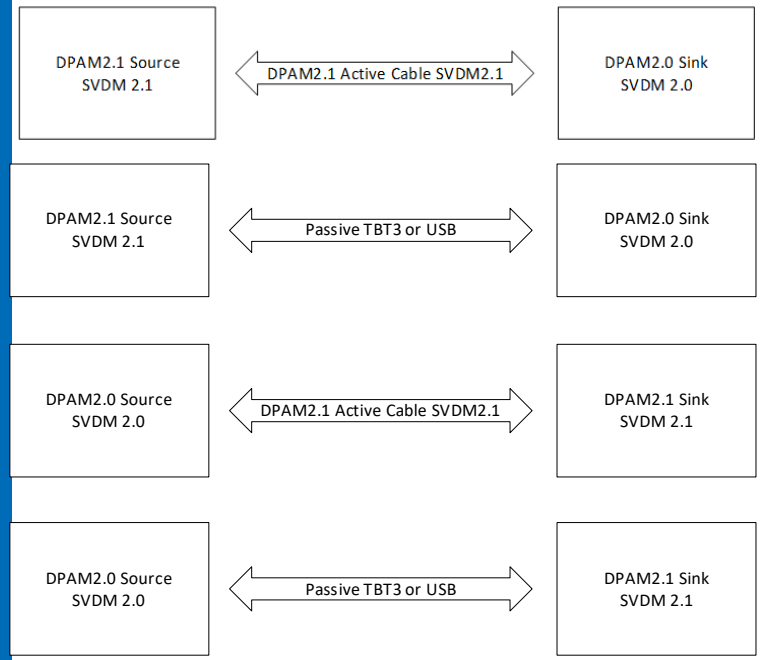
- SVDM Version resolution
  - DISCOVER IDENTITY (SOP'/ UFP)
  - DISCOVER SVIDs (SOP'/ UFP)
  - DISCOVER MODES (SOP'/ UFP)
    - DFP_U sends Discover Modes IF response "SVDM version = 2.1" then use "DPAM 2.1"
    - Else must use "DPAM 2.0"
  - ENTER MODE (SOP'/ UFP)
  - DP CONFIGURE (SOP'/ UFP)



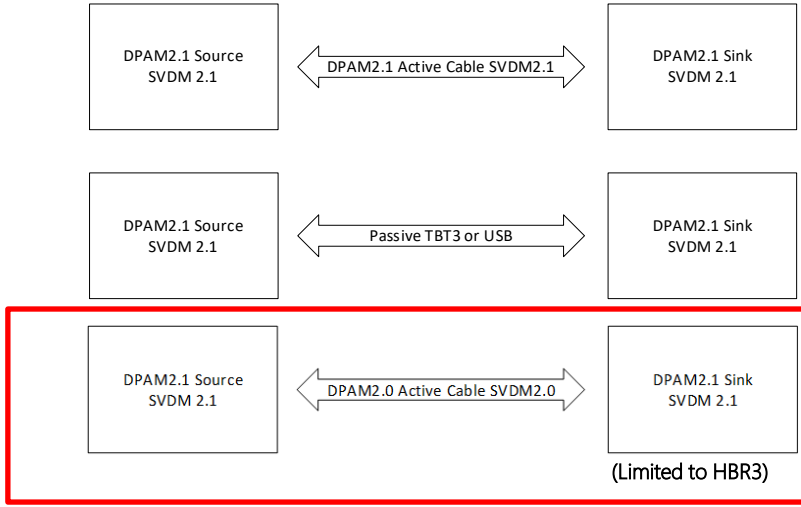


DP Alt-Mode SVDM Resolution Scenarios

DFP sends **DPAM2.0** DP Configure



DFP sends **DPAM2.1** DP Configure



Key Field Changes: DISCOVER MODE Response

SOP

DPAM2.0

Table 5-5: DP Capabilities (VDO in the Responder *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED. 01b = DP Sink device-capable (including DP Branch device). 10b = DP Source device-capable (including DP Branch device). 11b = Both DP Source and Sink device-capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP Standard* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = DP interface is presented on a USB-C plug. 1 = DP interface is presented on a USB-C receptacle.
7	*USB 2.0* Signaling Not Used	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)	00000000b = DP Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c,d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	00000000b = DP Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c,g] XXX1XXXXb = Pin Assignment E is supported.[b] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
31:24	RESERVED	RESERVED (always 00h).

DPAM2.1

Table 5-5: DP Capabilities (VDO in the Responder USB PD *Discover Modes*

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED 01b = *DP* Sink device-capable (including *DP* [illegible]vice). 10b = *DP* Source device-capable (including [illegible] device). 11b = Both *DP* Source and Sink device-cap[illegible]
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP* bit rates and electr[illegible]gs (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = *DP* interface is presented on [illegible] plug. 1 = *DP* interface is presented [illegible]*C* receptacle.
7	USB 2.0 Signaling Not Used	0 = *USB 2.0* may be needed [illegible] A7 –or– B6 – B7 while in DisplayPort Configura[illegible] 1 = *USB 2.0* is not needed [illegible] – A7 –or– B6 – B7 while in DisplayPort Configu[illegible]
15:8	DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)	00000000b = *DP* Sou[illegible]ce pin assignments are not supported. XXXXXXX1b = R[illegible]VED. XXXXXX1Xb = [illegible]VED. XXXXX1XXb = [illegible] Assignment C is supported.[b] XXXX1XXXb = [illegible]n Assignment D is supported.[c,d] XXX1XXXXb = [illegible] Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	00000000b – *DP* Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c,g] XXX1XXXXb = Pin Assignment E is supported.[b] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
29:24	RESERVED	RESERVED (always 00h).
31:30	DPAM Version[f]	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

29:28[d]	**Active Component**	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
	Signaling for Transport of DisplayPort Protocol[b]	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20).
	UHBR13.5	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[e]

SOP'

DPAM2.0

SOP' Cable DP Capabilities (DPAM2.0)		
Bits	Field	CTS Value
B31-24	Reserved	0000 0000b
B23-16	DP Sink Device Pin Assignment Supported	0000 1100b
B15-8	DP Source Device Pin Assignment Supported	0000 1100b
B7-6	Reserved	00b
B5-2	Signal for Transport of DP Protocol	0001b
B1-0	Reserved	00b

DPAM2.1

	Description	Values
	RESERVED	RESERVED (always 00b).
	Signaling for Transport of DisplayPort Protocol[b]	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[e]
7:6	RESERVED	RESERVED (always 00b).
15:8	DP Source Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported. 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
23:16	DP Sink Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
24	RESERVED	RESERVED (always 00b).
25	UHBR13.5	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[e]
27	RESERVED	RESERVED (always 0).
29:28[d]	Active Component	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30	DPAM Version	00b = Original version. 01b = Version 1.

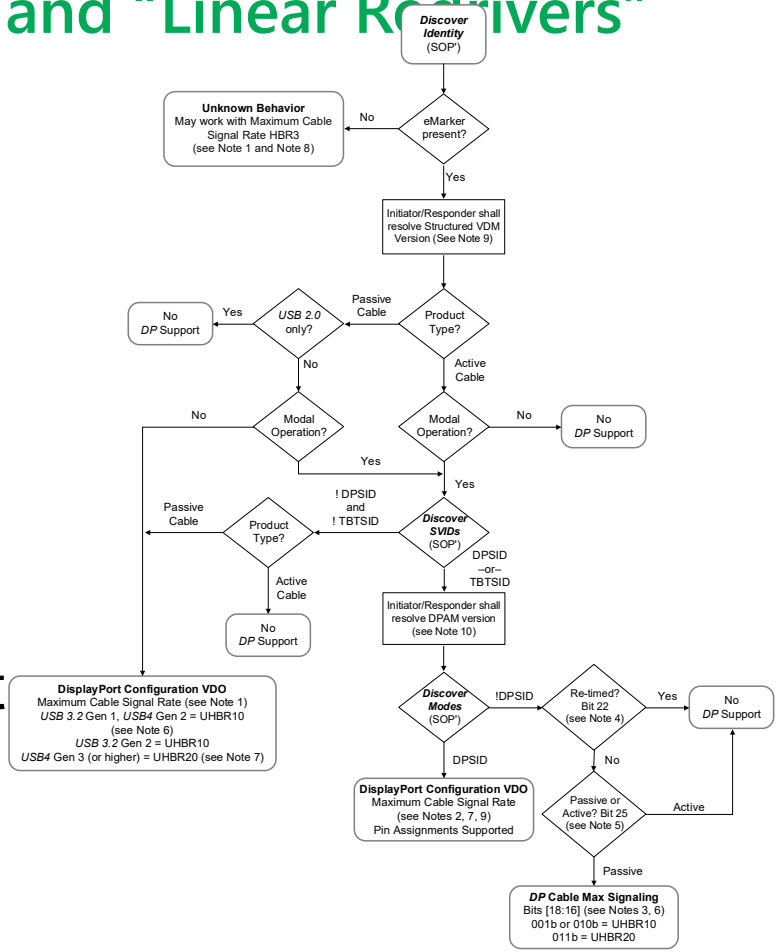
Discover Modes Response from UFP

Discover Modes Response from Cable

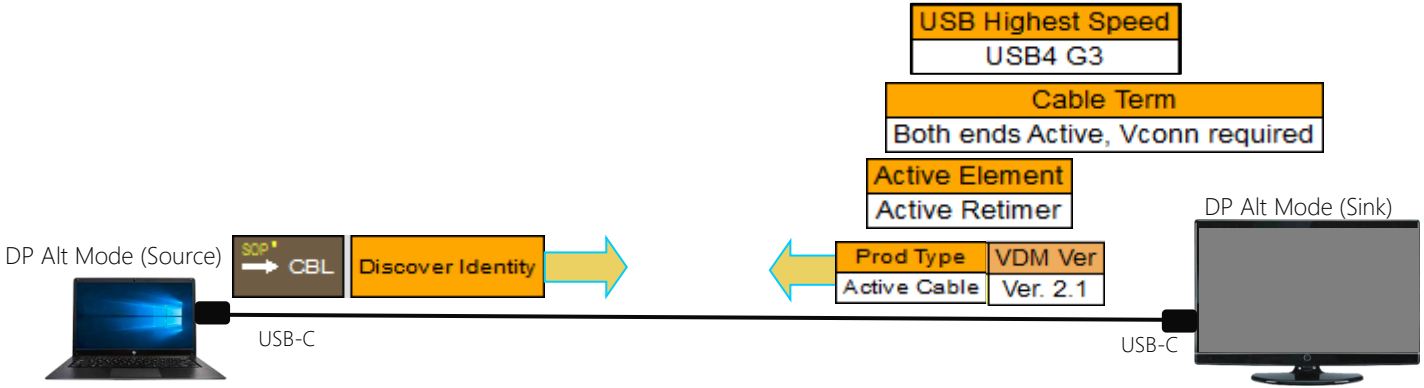
DP Alt Mode 2.1
Configuration with Active Cable

Active Cables: "Retimers" and "Linear Redrivers"

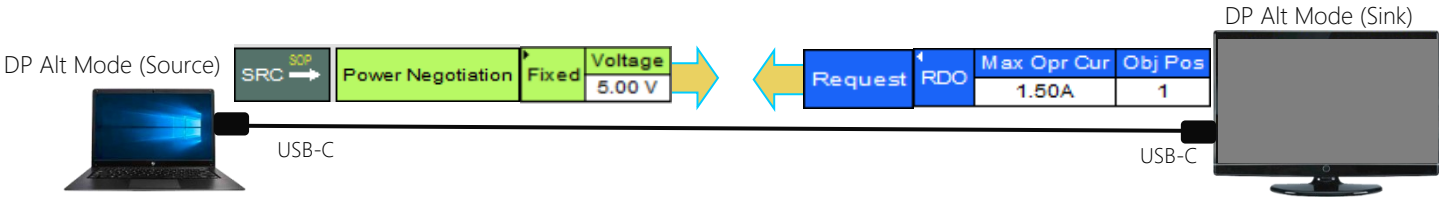
- DFP_U Must send ENTER MODE to the Cable
- C-to-DP Adapters: should support "reversible" operation
  - if not, visually indicate which direction they support
- Active Type-C Cables must support one bidirectional USB 3.2 link



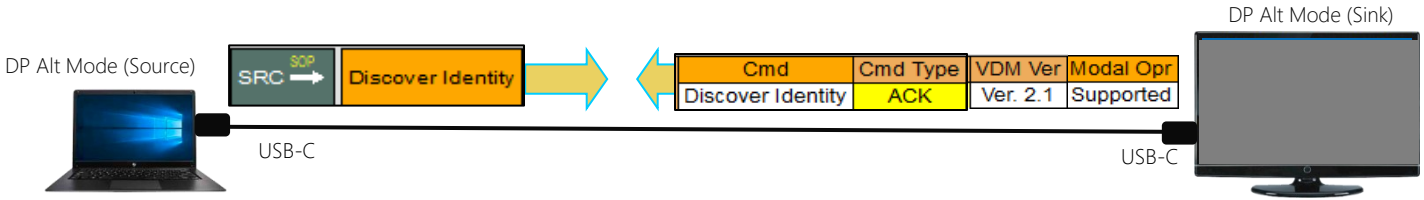
DFP Sends Discover Identity to the Cable (SOP')



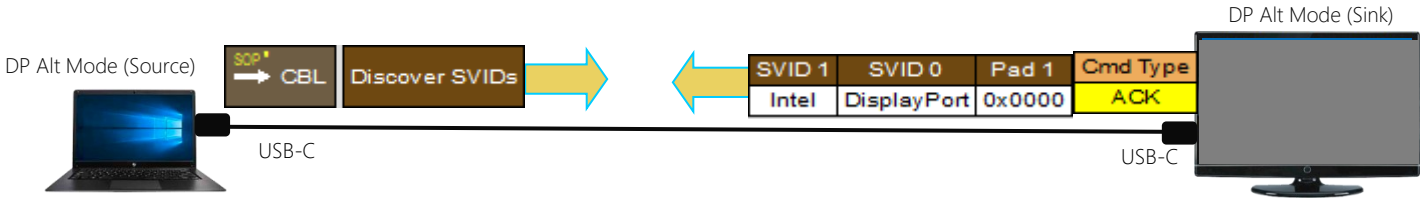
DFP Negotiates Initial Power Delivery Contract



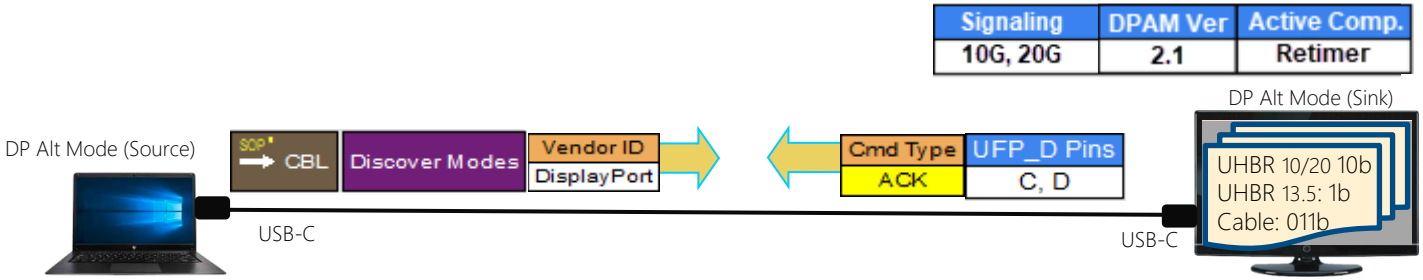
DFP Sends Discover Identity to the Sink (SOP)



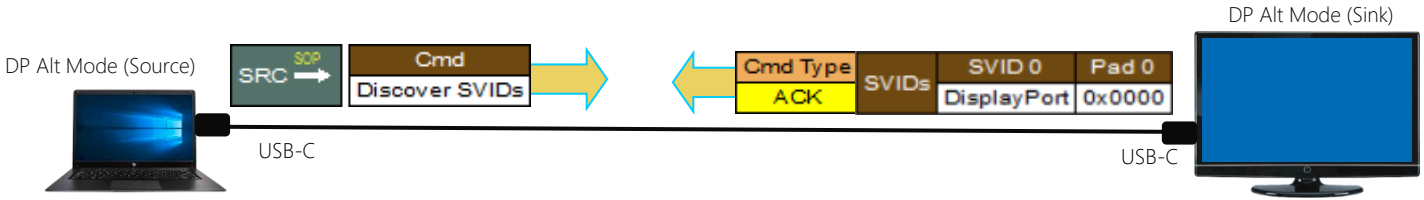
DFP Sends Discover SVIDs to the Cable (SOP')



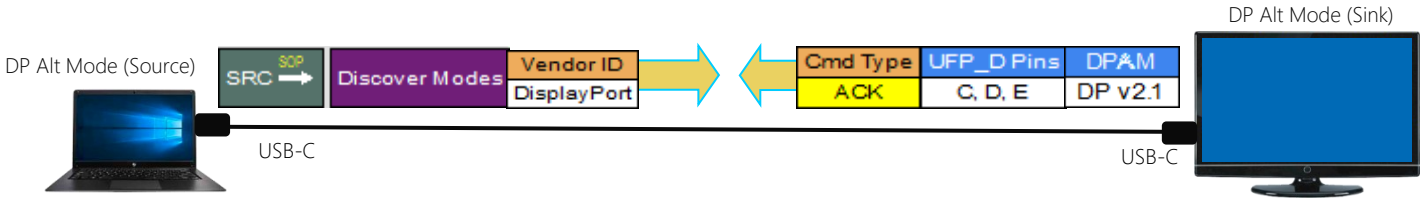
DFP Sends Discover Modes to the Cable (SOP')



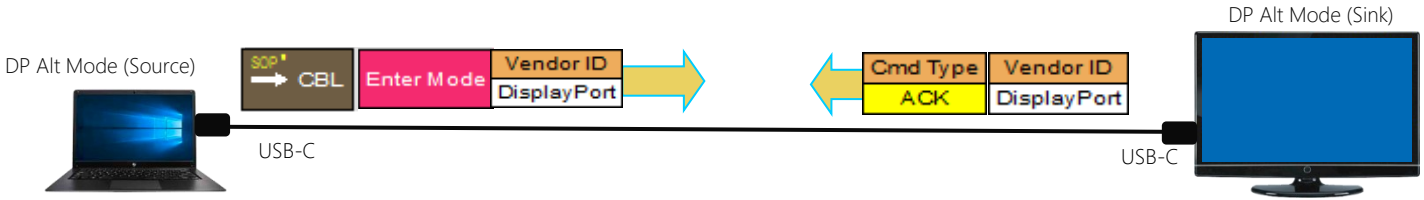
DFP Sends Discover SVIDs to the Sink (SOP)



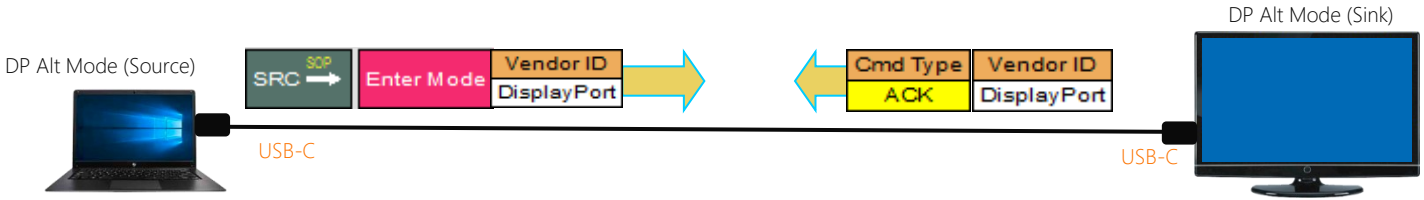
DFP Sends Discover Modes to the Sink (SOP)



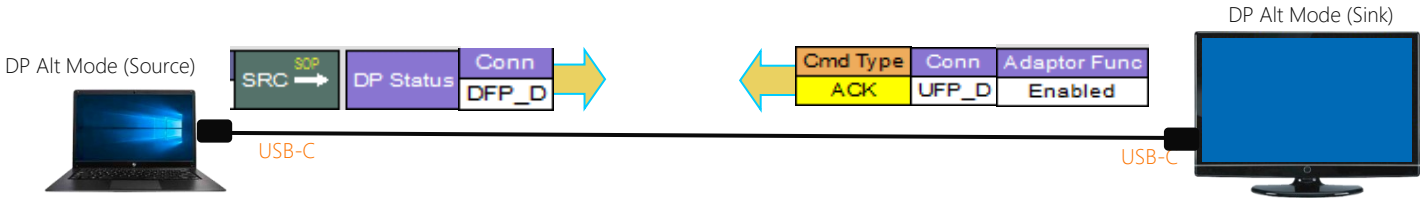
DFP Sends Enter Mode to the Cable (SOP')



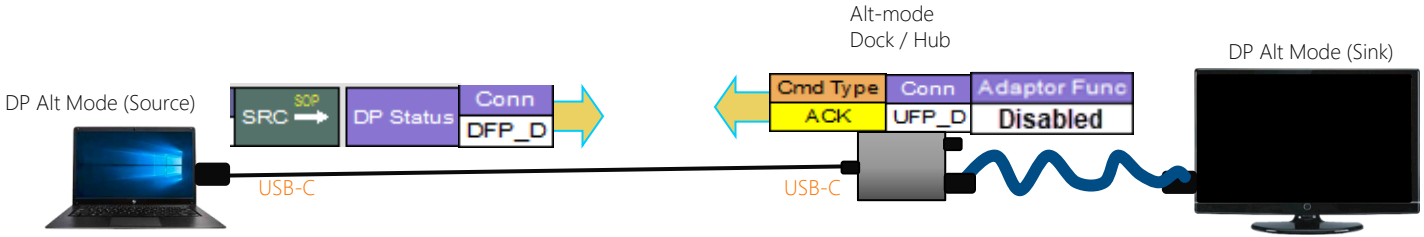
DFP Sends Enter Mode to the Sink (SOP)



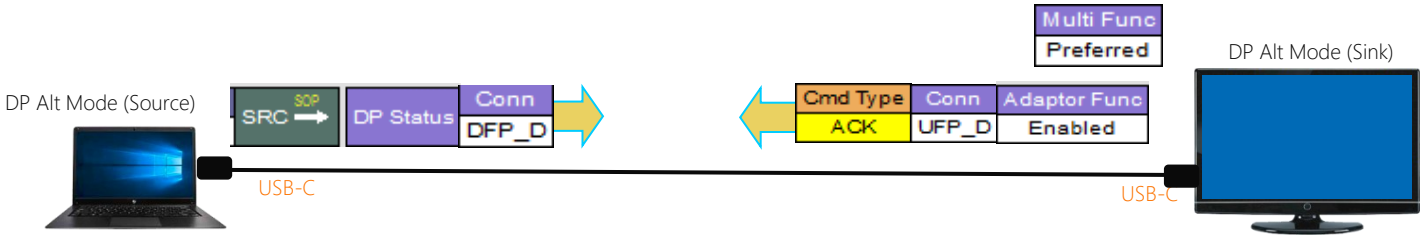
DFP Sends DP Status to the Sink (SOP)



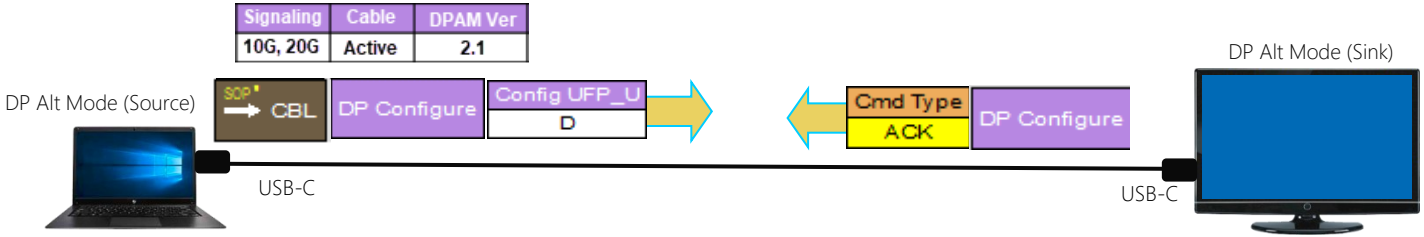
DFP Sends DP Status to the Sink (SOP)



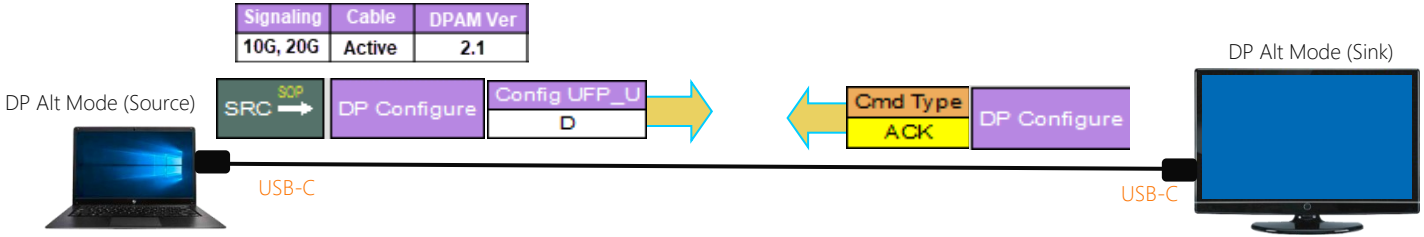
DFP Sends DP Status to the Sink (SOP)



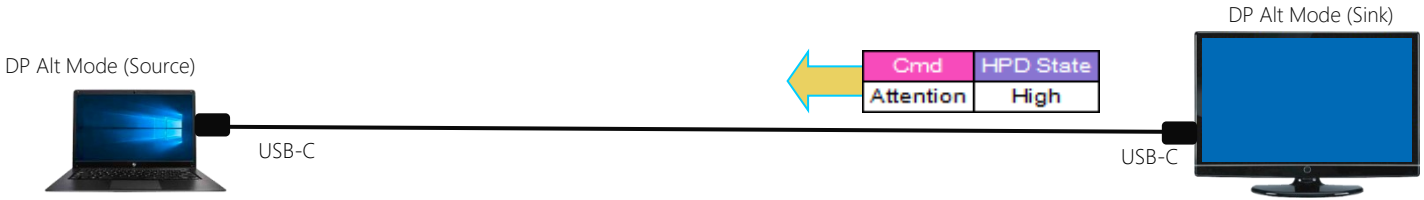
DFP Sends DP Configure to the Cable (SOP')



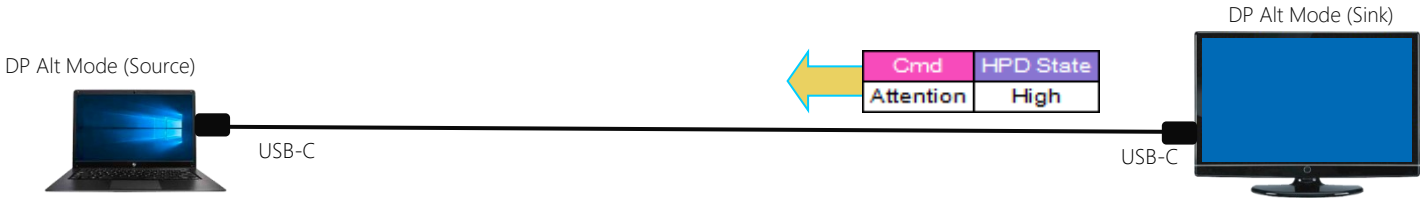
DFP Sends DP Configure to the Sink (SOP)



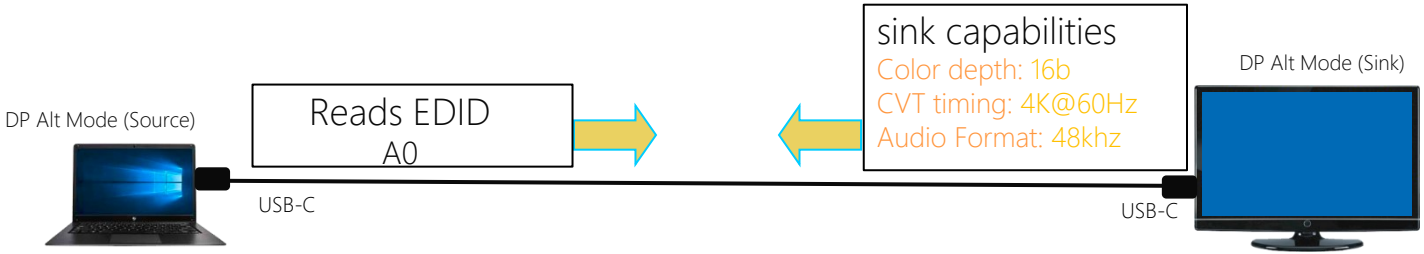
UFP Sends Attention Message to the DFP



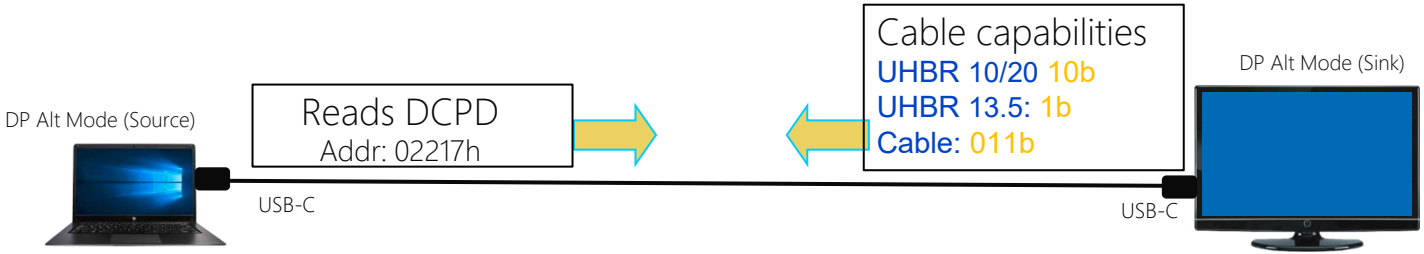
UFP Sends Attention Message to the DFP



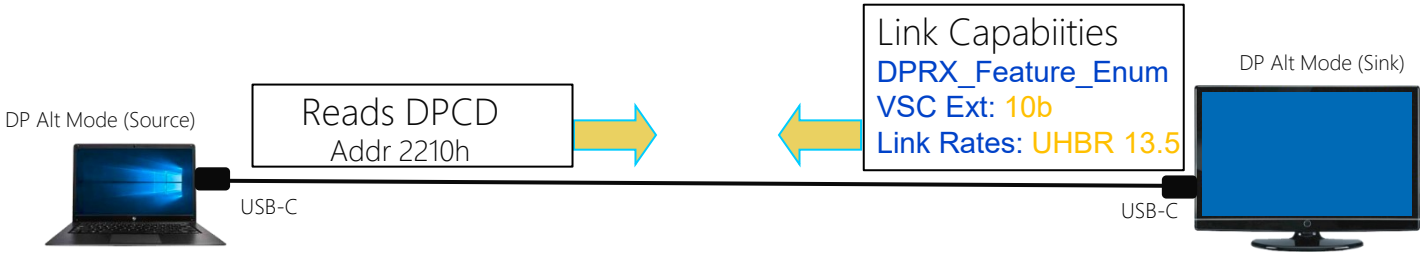
Link Training: Read DisplayID or legacy EDID



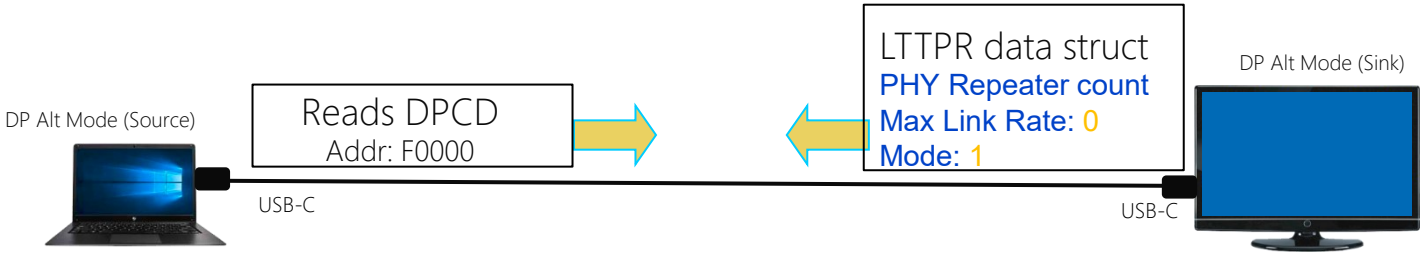
Link Training: Read Cable Capabilities



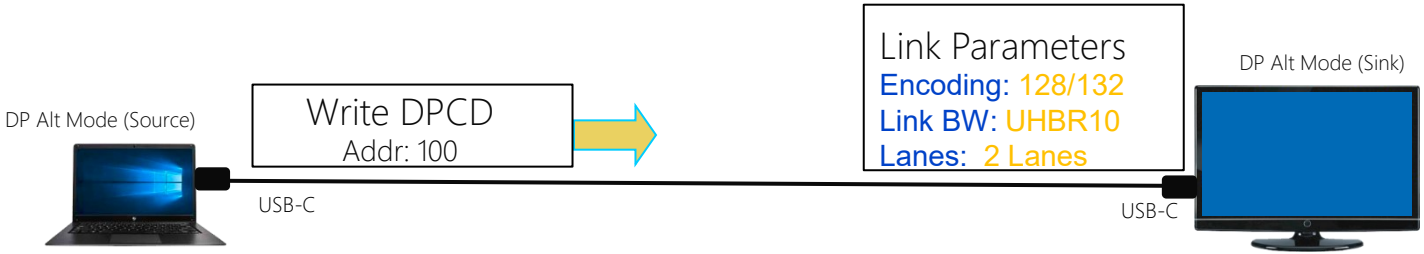
Link Training: Read Link Capabilities



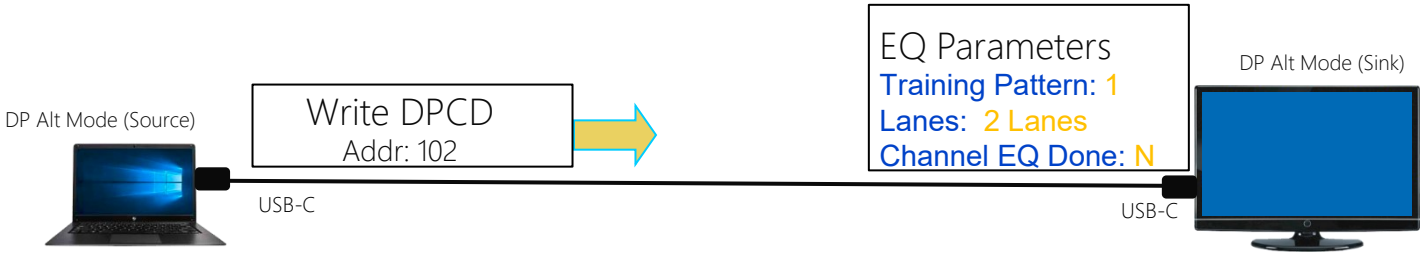
Link Training: Read LTTPR Data



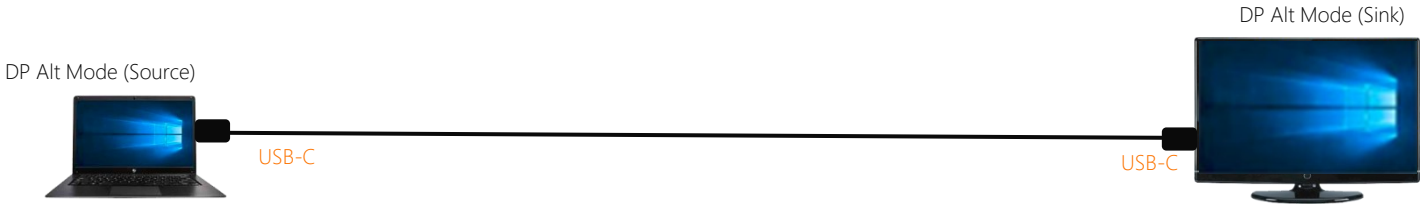
Link Training: Lanes & Link Bandwidth Set



Link Training: Equalization & Clock Domain Switch

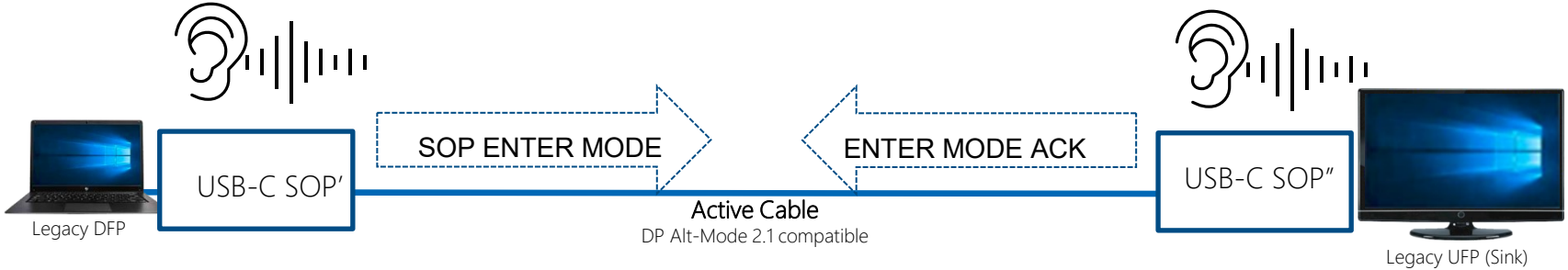


Link Training: Equalization & Clock Domain Switch

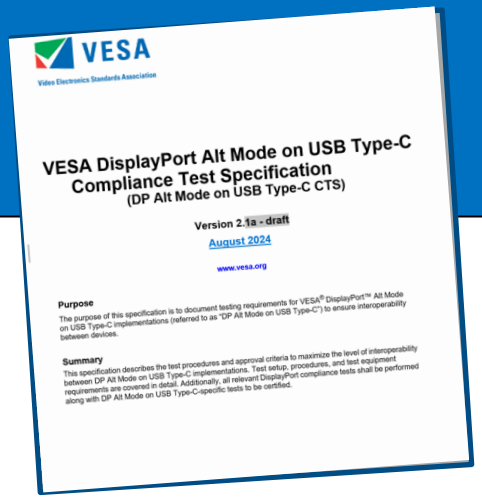


DP 2.1 Active Cable “Snoop” mode

- **Special Situation**: Legacy DP_Sources that do not send ENTER MODE to the cable:
  - **DP Alt Mode 2.1** Active cables are required to snoop SOP commands and silently perform the same on SOP’ & SOP” for:
    - ENTER MODE
    - CONFIGURE
    - EXIT MODE



DP Alt-Mode v2.1a
Compliance Test Specification


VESA
Video Electronics Standards Association

VESA DisplayPort Alt Mode on USB Type-C
Compliance Test Specification
(DP Alt Mode on USB Type-C CTS)

Version 2.1a - draft
August 2024

www.vesa.org

Purpose
The purpose of this specification is to document testing requirements for VESA® DisplayPort™ Alt Mode on USB Type-C implementations (referred to as "DP Alt Mode on USB Type-C") to ensure interoperability between devices.

Summary
This specification describes the test procedures and approval criteria to maximize the level of interoperability between DP Alt Mode on USB Type-C implementations. Test setup, procedures, and test equipment requirements are covered in detail. Additionally, all relevant DisplayPort compliance tests shall be performed along with DP Alt Mode on USB Type-C-specific tests to be certified.

TELEDYNE LECROY
Everywhereyoulook™

DP Alt Mode v2.1 Compilance Test Specification

- Contents
  - Ch:3 Physical Layer
  - Ch:4 Cables
  - Ch:5 Type-C-to-DP Plug Connector
  - Ch:6 DP Alt Mode Protocol Converter
  - Ch:7 DP Alt Mode Type-C Source
  - Ch:8 DP Alt Mode Type-C Sink
  - Ch:9 AUX and HPD
  - Ch:10 Discovery and USB PD
  - Ch:11 VBUS and VCONN

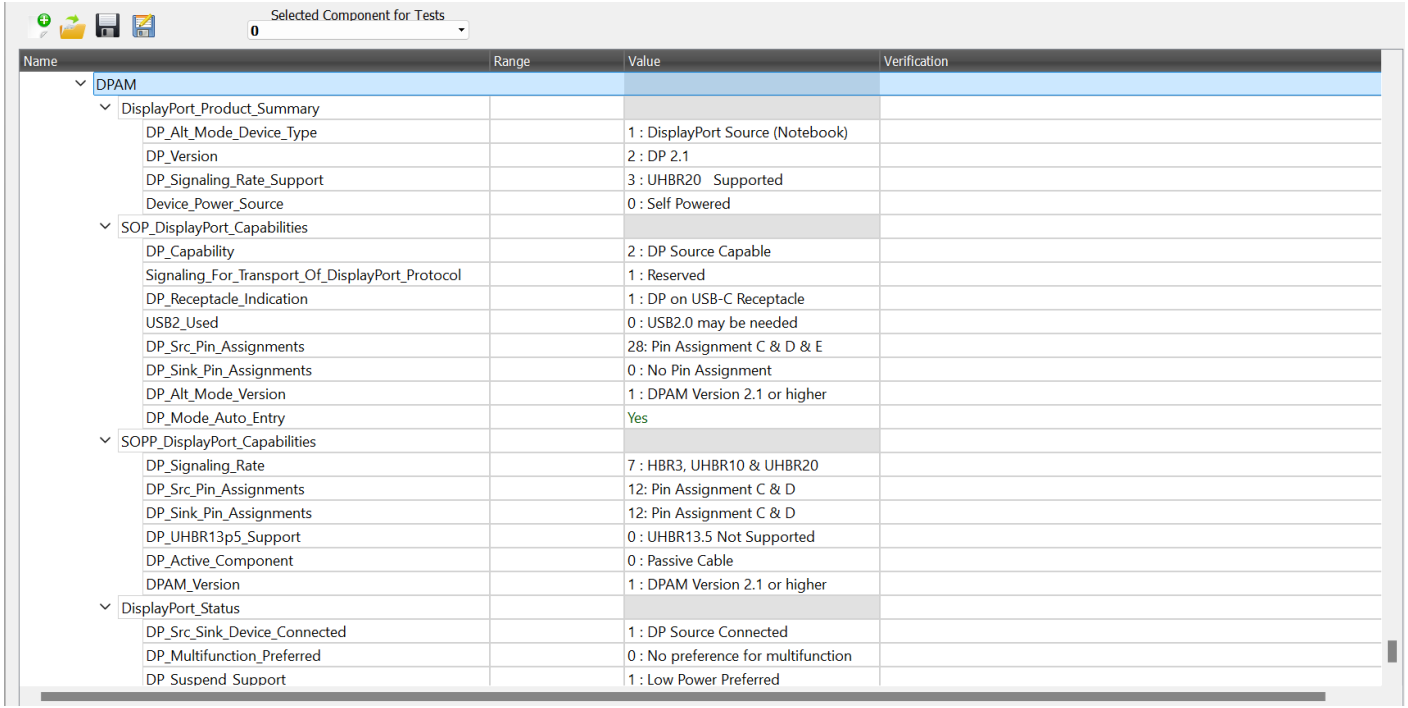
LabMaster 10Zi A

Quantumdata M42de
DP 2.1 Compliance Tester

Voyager M310e USB-C
Compliance Tester

DP Alt Mode VIF

- Utilizes USB.org VIF: Optional Content fields
- Allows efficient testing of DPAM devices
- Download latest revision: www.VESA.org
-



Name	Range	Value	Verification
DPAM			
DisplayPort_Product_Summary			
DP_Alt_Mode_Device_Type		1 : DisplayPort Source (Notebook)	
DP_Version		2 : DP 2.1	
DP_Signaling_Rate_Support		3 : UHBR20 Supported	
Device_Power_Source		0 : Self Powered	
SOP_DisplayPort_Capabilities			
DP_Capability		2 : DP Source Capable	
Signaling_For_Transport_Of_DisplayPort_Protocol		1 : Reserved	
DP_Receptacle_Indication		1 : DP on USB-C Receptacle	
USB2_Used		0 : USB2.0 may be needed	
DP_Src_Pin_Assignments		28: Pin Assignment C & D & E	
DP_Sink_Pin_Assignments		0 : No Pin Assignment	
DP_Alt_Mode_Version		1 : DPAM Version 2.1 or higher	
DP_Mode_Auto_Entry		Yes	
SOPP_DisplayPort_Capabilities			
DP_Signaling_Rate		7 : HBR3, UHBR10 & UHBR20	
DP_Src_Pin_Assignments		12: Pin Assignment C & D	
DP_Sink_Pin_Assignments		12: Pin Assignment C & D	
DP_UHBR13p5_Support		0 : UHBR13.5 Not Supported	
DP_Active_Component		0 : Passive Cable	
DPAM_Version		1 : DPAM Version 2.1 or higher	
DisplayPort_Status			
DP_Src_Sink_Device_Connected		1 : DP Source Connected	
DP_Multifunction_Preferred		0 : No preference for multifunction	
DP_Suspend_Support		1 : Low Power Preferred	

DP Alt-Mode 2.1 Cable Discovery Tests (for DFPs)

Verify UUT identifies cable speed, type, DPAM ver w/ SOP **DP CONFIGURE** message

Test	Description
10.3.3	Alt Mode Entry with USB Type-C to USB Type-C Passive non-emarked
10.3.4	Alt Mode Entry with USB Type-C to USB Type-C Passive TBT3 cable
10.3.5	Alt Mode Entry with Type-C to Type-C Passive USB4 Gen3 cable
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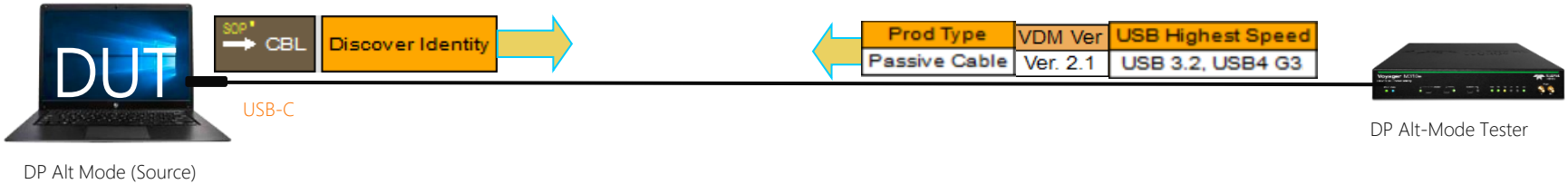

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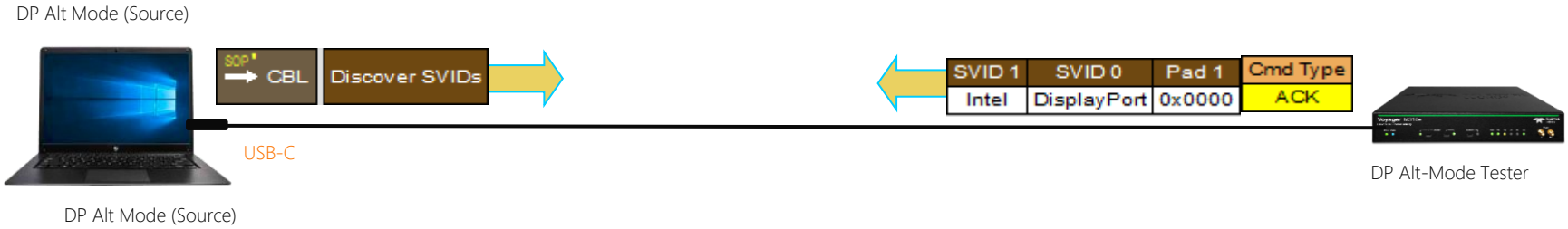

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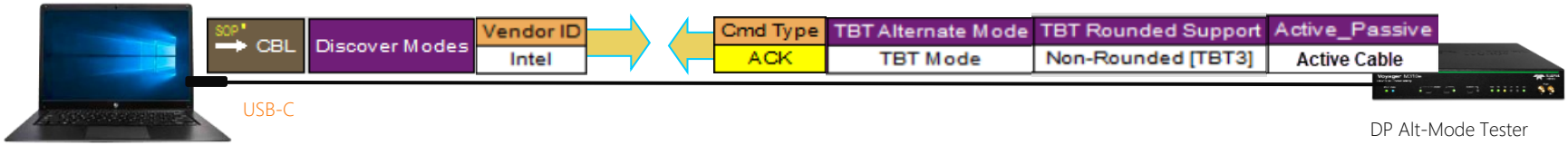

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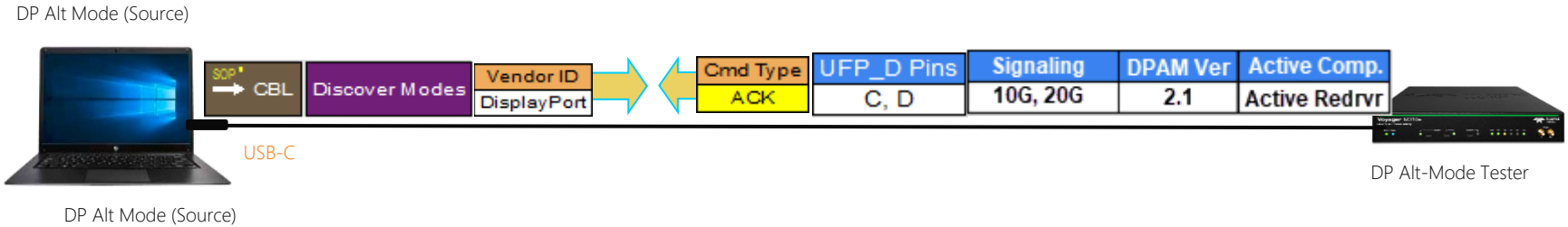

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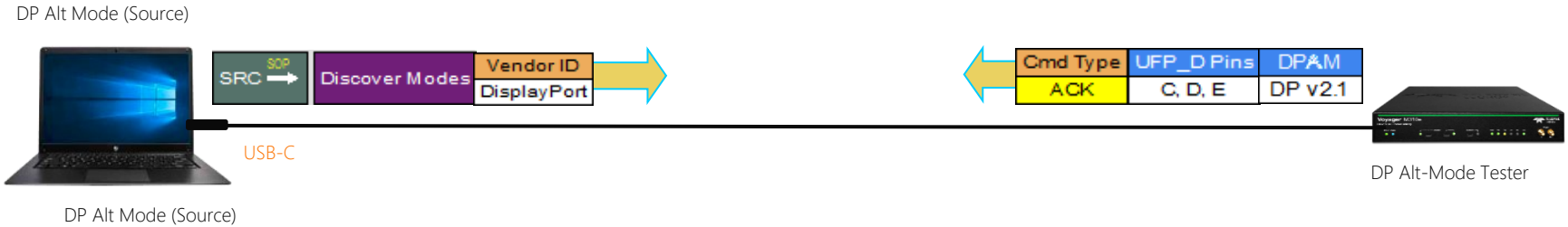

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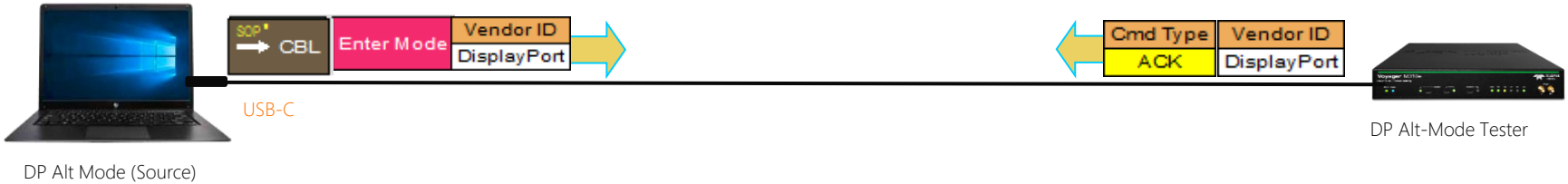

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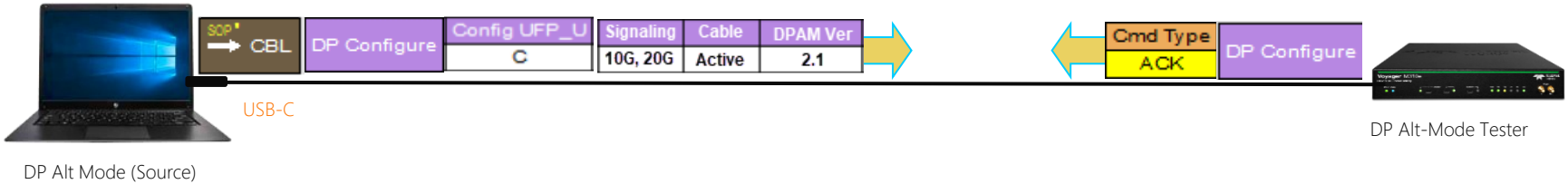


Thank You

VESA DisplayHDR CTS r1.2

Robert Yang

Granite River Labs

2024 / 10 / 09

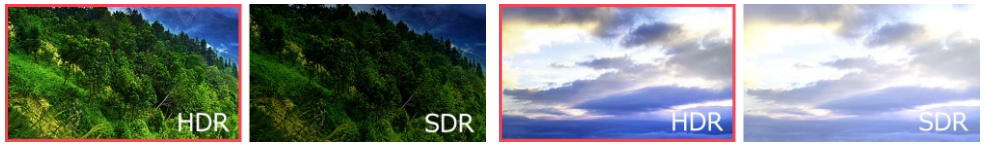
Tables

- HDR Overview
- VESA DisplayHDR Introduction
- DisplayHDR CTS r1.2 Update
- DisplayHDR CTS r1.2 Implementation
- DisplayHDR Common Issues
- Summary

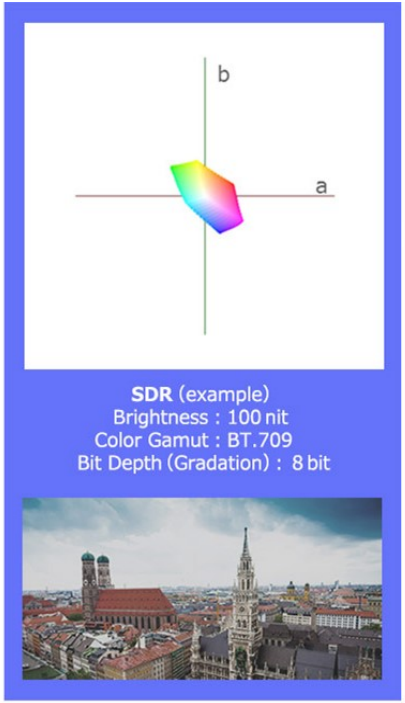
VESA

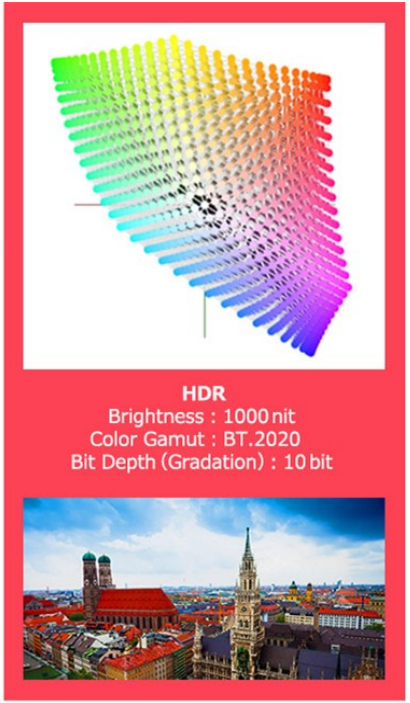
HDR Overview

Introduction - HDR (High Dynamic Range Imaging)



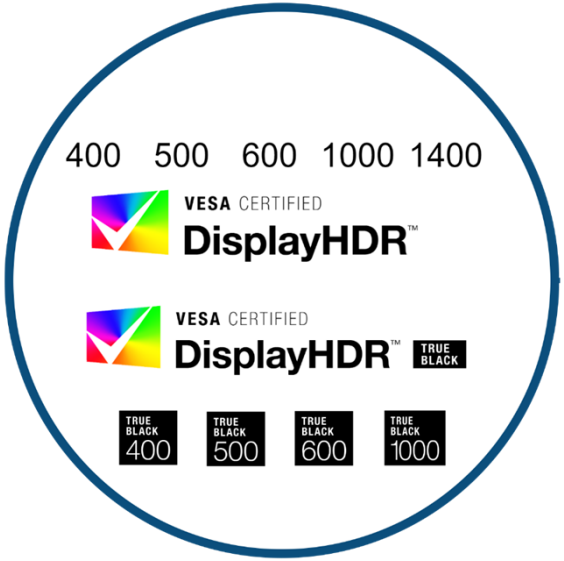
More details in the shadow





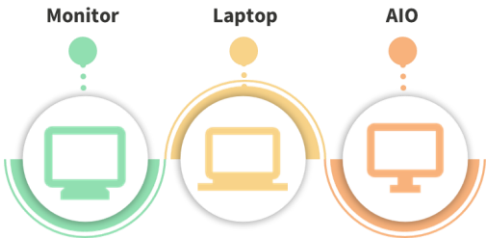
VESA DisplayHDR Introduction

Introduction – VESA DisplayHDR Certification



- **Brightness**
- **Contrast**
  - Dynamic Contrast Ratio
  - Static Contrast Ratio
- **Range of color**
  - DCI-P3
  - sRGB (BT.709)
- **Bit-Depth**
- **Rise time**

Product Type



Timeline – VESA DisplayHDR Certification

CTS r1.0

2017

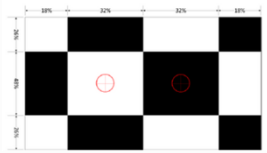
- Initial release
  - Classic 400 / 600 / 1000

CTS r1.1

2019

- Added new performance tier
  - Classic 500 / 1400
  - TrueBlack 400 / 500 / 600 / 1000 / 1400
- Add / optimize testing items
- Static contrast method → dynamic

CTS r1.1 E2



2021

- Checkerboard test
  - Added a 4x3 pattern for DUT smaller than 20“
  - Luminance for TrueBlack
- Revised descriptions for some test items

CTS r1.2

2024

- Stricter testing standards
- New Pattern
- Add 5 new testing items

Introduction – Specification Update

New spec for CTS r1.2

VESA CERTIFIED DisplayHDR™	Minimum Peak Luminance	Range of Color		Maximum Black Level Luminance	Static Contrast Ratio	Max ΔTP Color Patch Error
	Brightness in cd/m²	ITU-R BT.709 Coverage	DCI-P3 (D65) Coverage	Brightness in cd/m²	-	Number of Video Frames
DisplayHDR 400	400	95% → 99%	N/A → 95%	0.4	1,300 : 1	8
DisplayHDR 500	500	99%	90% → 95%	0.1	7,000 : 1	8
DisplayHDR 600	600	99%	90% → 95%	0.1	8,000 : 1	8
DisplayHDR 1000	1000	99%	90% → 95%	0.05	30,000 : 1	6
DisplayHDR 1400	1400	99%	95%	0.02	50,000 : 1	6
VESA CERTIFIED DisplayHDR™ TRUE BLACK	Minimum Peak Luminance	Range of Color		Maximum Black Level Luminance	Static Contrast Ratio	Max ΔTP Color Patch Error
	Brightness in cd/m²	ITU-R BT.709 Coverage	DCI-P3 (D65) Coverage	Brightness in cd/m²	-	Number of Video Frames
DisplayHDR True Black 400	400	99%	90% → 95%	0.0005	N/A	8
DisplayHDR True Black 500	500	99%	90% → 95%	0.0005	N/A	8
DisplayHDR True Black 600	600	99%	90% → 95%	0.0005	N/A	8
DisplayHDR True Black 1000	1000	99%	90% → 95%	0.0005	N/A	8

Measurement Instrument / Sensor Usage

Recommended Measurement Instruments for DisplayHDR and DisplayHDR True Black Certification		
Certification Level	**Manufacturer**	**Model Numbers**
DisplayHDR	Konica-Minolta™ Photo Research SpectraDuo® Gamma Scientific Topcon TechnoHouse	CA-310a、CA-410: CA-P427、**CA-VP427**、CS-2000 PR-670、PR-680 GS-1220 SR-UL1R
DisplayHDR True Black	Konica-Minolta™ Photo Research SpectraDuo® Photo Research SpectraScan® Topcon TechnoHouse	**CS-2000A**、CS-3000、CS-3000HDR PR-680、PR-680L PR-740、PR-745、PR-788、PR-1050 SR-UL2

Measurement Instrument Mandates for DisplayHDR and DisplayHDR True Black Certification		
Mandate	**Certification Level**	
	DisplayHDR	**DisplayHDR True Black**
Black Level Luminance Range	0.05 to 4 cd/m2 ±4%	0.0005 to 4 cd/m2 ±4%
White Level Luminance Range	400 to 1,400+ cd/m2 ±2%	
Color Accuracy	0.003 x, y	

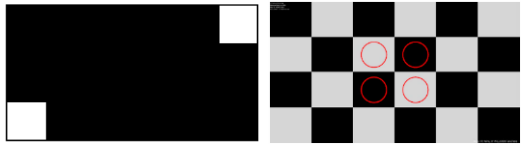
KONICA MINOLTA

PHOTO RESEARCH INC.
The Reference in Color and Light Measurement

GAMMA SCIENTIFIC

TOPCON
TOPCON TECHNOHOUSE CORPORATION

Dual Corner / CheckerBoard ▶



Color Gamut & Luminance Test ▶

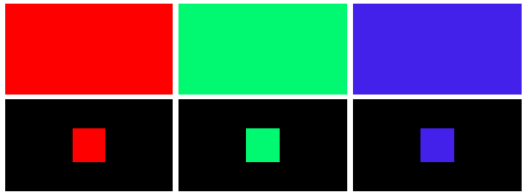


Figure 6-1: RGB Color Gamut Test

VESA

DisplayHDR CTS r1.2 Update

(Released in 2024/4/1)

DisplayHDR CTS r1.1 vs r1.2

CTS No.	Test Tool No.	item
-	Reported Panel Characteristics	EDID.MaxLuminance
5.1.1	1a	10% Center Luminance Patch
5.1.2	2a	Flash Luminance Test
5.1.3	3a	Full Screen Luminance Test
5.2.1	4	Dual Corner Test
5.2.2	5 / 5.1 / 5.2	CheckerBoard Test
6	6	Color Gamut & Luminance Test
7	7	DisplayHDR Bit Depth
8	8	Rise Time measurements
9	9	Delta-ITP
10	1.2.1	Static Contrast Ratio Test
11	1.2.2	HDR vs. SDR Black Level Test
12	v1.2.3	Black Crush Test
13	1.2.4	Subtitle Luminance Flicker Test
14	1.2.5	XRite Color Square Test

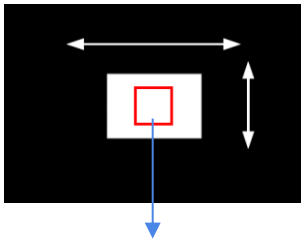
= criteria update in current item

= CTS r1.2 New Item

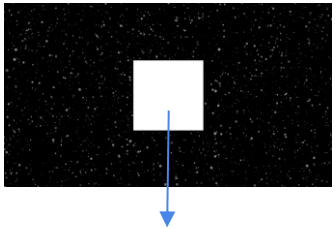
CTS r1.2 New Item

DisplayHDR CTS r1.1 vs r1.2 – Spec Update

Test / Specification			Performance Tier				
Test item	**Revision 1.1**	**Revision 1.2**	**400**	**500**	**600**	**1000**	**1400**
5.1.1 Minimum-white Luminance	10% Center Patch Test	8% Center Square Test + star field pattern	400	500	600	1000	1400
6 Color Gamut Specifications	sRGB Coverage u'v' for the 10% Patch	sRGB Coverage u'v' for the 8% Patch	95% → 99%	99%			
	DCI-P3 Coverage u'v' for the 10% Patch	DCI-P3 Coverage u'v' for the 8% Patch	N/A → 90%	90% → 95%			95%
7 Bit-depth testing	DisplayHDR Bit Depth	DisplayHDR Bit Depth	8b → 8b+2b FRC	8b+2b FRC			



CTS 1.1: 10% Center Patch Test



CTS 1.2: 8% Center Patch Test + star field pattern

Test effort added		
Type	**Classic**	**TrueBlack**
Time	19%	29%

DisplayHDR CTS r1.1 vs r1.2 – Spec Update

Test item	Revision 1.1	Revision 1.2	400	500	600	1000	1400
9 Delta-ITP	10% Test Patch Luminance Target	8% Center Square Target	Delta-ITP				
	N/A	1.0509	N/A → 20				
	5.172	5.172	20				
	14.958	14.958	20 → 15				
	50.825	50.825	15 → 10				
	100.23	100.23					
	199.15	199.15					
	50% of Tier	50% of Tier	15 → 10				
	N/A	Near Tier	N/A → 10				

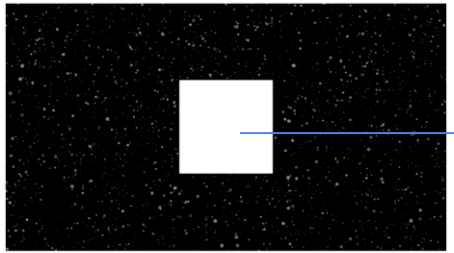


Figure 9-4: Luminance and White Point Test Pattern – Shown with Maximum Luminance Subtest

8% Center Patch Test + star field pattern

DisplayHDR CTS r1.1 vs r1.2 – New Items

Test / Specification		Performance Tier				
Test item	**Test Pattern**	**400**	**500**	**600**	**1000**	**1400**
10 Static Contrast Ratio Test	1D pattern for 400 / 500 / 600 2D pattern for 1000 / higher	1300:1	7000:1	8000:1	30k:1	50k:1
11 HDR vs. SDR Black Level Test	Black and white split-screen image	>90%				
12 Black Crush Test	Full screen black and dark-gray	5				
13 Subtitle Luminance Flicker Test	Gray 8% center square at 10 cd/m²	13%			10%	
14 XRite Color Square Test	50, 100 cd/m², 50% of Logo Level	8			6	

DisplayHDR CTS r1.2

CH10 Static Contrast Ratio Test

- This test measure the maximum contrast ratio in a single scene by measuring black and white on one image.

1D pattern: For DisplayHDR-400, 500, and 600

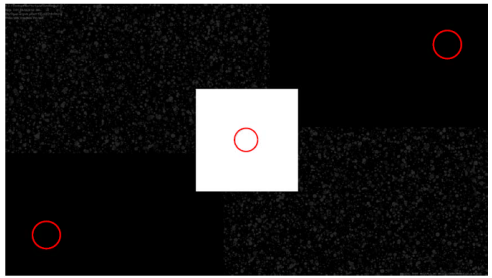


Figure 10-1: Static Contrast Ratio Test Pattern for DisplayHDR-400, 500, and 600 – Shown with Location Guidance Circles and Informational Text

2D pattern: For DisplayHDR 1000 and Higher

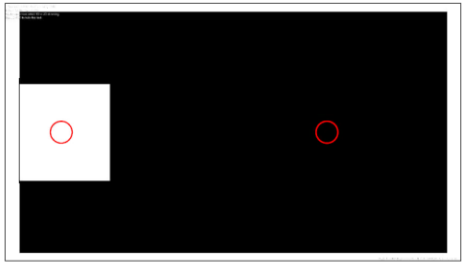


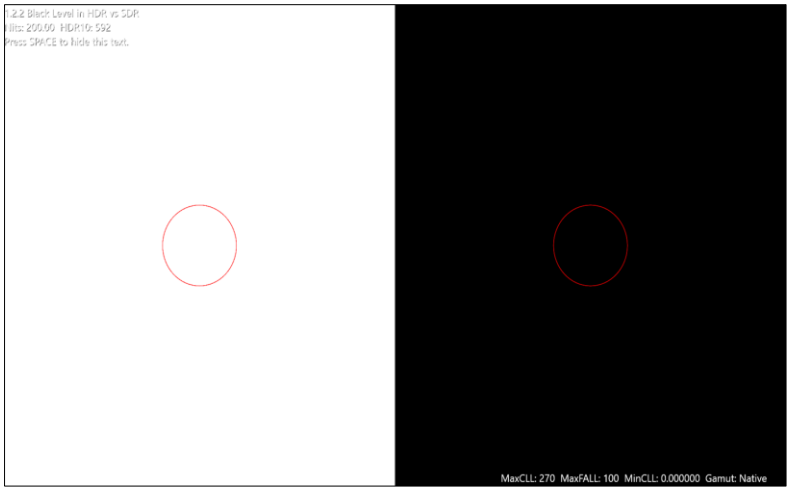
Figure 10-2: Static Contrast Ratio Test Pattern for DisplayHDR-1000 and 1400 – Shown with Measurement Location Circles and Informational Text

DisplayHDR Performance Tier	Test Pattern Required	Required Contrast Ratio
400	1D	1300:1
500		7000:1
600		8000:1
1000	2D	30k:1
1400		50k:1

DisplayHDR CTS r1.2

CH11 HDR vs SDR Black Level Test

- This test confirms that the display's black level in HDR mode is as dark, or darker than the black level when in SDR mode to ensure that HDR mode performs at least as well as SDR mode.



$$CR_{HDR} \geq CR_{SDR} \times 0.9$$

DisplayHDR CTS r1.2

CH12 Black Crush Test

- This test verifies that the display is capable of distinguishing dark gray levels and is not crushing gray levels into black.
- Full screen, five test images: 0, 0.05, 0.1, 0.3, 0.5 cd/m^2
- The sequence of five luminance tests must yield five sequentially brighter output results without assessing output accuracy.

DisplayHDR CTS r1.2

CH13 Subtitle Luminance Flicker Test

- This test confirms correct behavior with subtitles in movies.
- The subtitles should not affect the gray square's luminance level.
- Measure the gray square's percentage variance in luminance

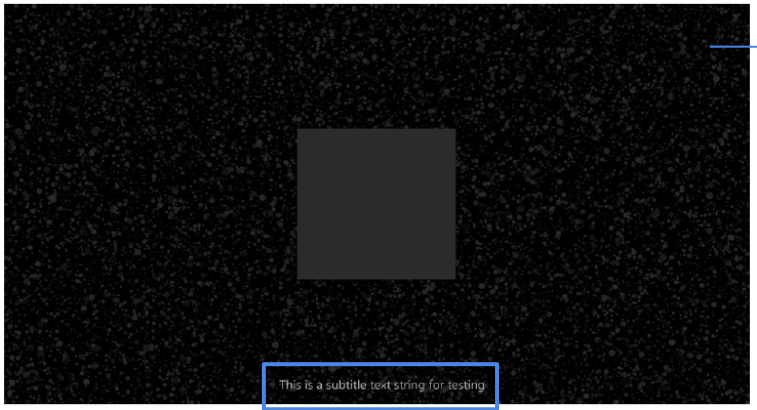


Figure 13-1: Subtitle Flicker Test – Gray Center Square Luminance Should Not Change as Subtitles Appear and Disappear from the Screen

star field pattern (10nits)

Subtitle (100nits)

Performance Tier	400	500	600	1000	1400
Spec	13%			10%	

Maximum Luminance divided by Minimum Luminance.

DisplayHDR CTS r1.2

CH14 XRite Color Square Test

- This test measures the display's color accuracy at various HDR luminance levels, using a large set of 96 test color squares.
- This test focuses purely on color, not luminance, and thus uses a Delta-TP measurement method.
- The colors are tested at three different luminance levels, with each luminance level indicating the target luminance for white:
  - 50 cd/m2
  - 100 cd/m2
  - 50% of DisplayHDR Compliance Logo level

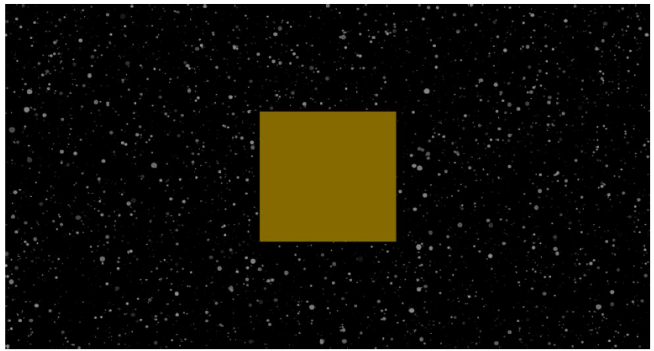


Figure 14-1: Xrite Color Square Test – One of 96 Test Colors, Tested at Three Different Luminance Levels

Performance Tier	400	500	600	1000	1400
Spec (Delta-TP averages)	8			6	

VESA

DisplayHDR CTS r1.2 Implementation

DisplayHDR CTS r1.2 Implementation

- Testing of CTS r1.2 has already been able to start since May 2024.
- The implementation deadline for the CTS r1.1 specification:
  By the end of May 2025 **for monitors.**
  By the end of May 2026 **for laptops.**

2024.5

CTS r1.2 has started to be enabled.

2025.5

The monitor can no longer obtain the CTS r1.1 certification.

2026.5

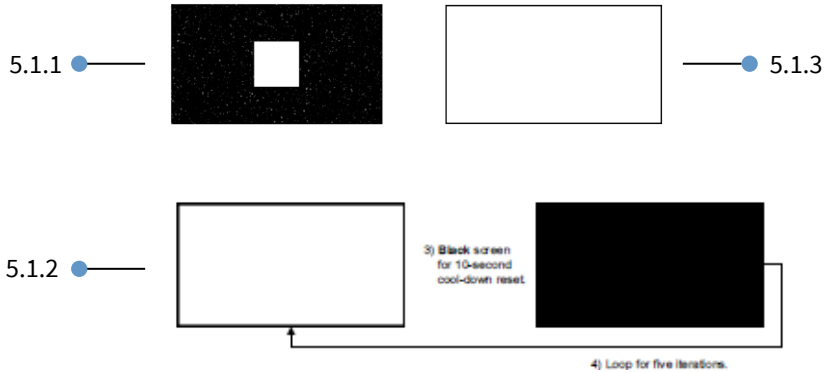
The laptop can no longer obtain the CTS r1.1 certification.

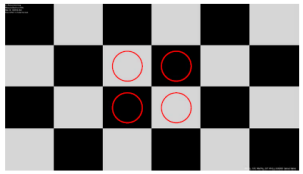
VESA

DisplayHDR Common Issues

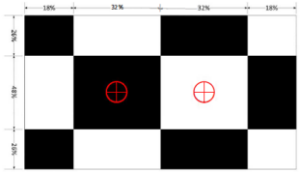
DisplayHDR – Common Test Issues

- Overall brightness
  - 5.1.1、10% Center Luminance
  - 5.1.2、Flash Luminance Test
  - 5.1.3、Full Screen Luminance Test
- Local dimming capability
  - 5.2.2、CheckerBoard Test

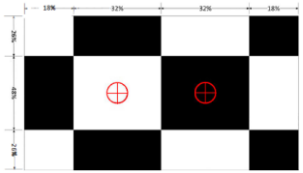




6x4 Pattern

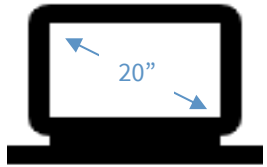


4x3 Pattern



4x3 Pattern

Monitor



Laptop

Summary

Summary

HDR Overview

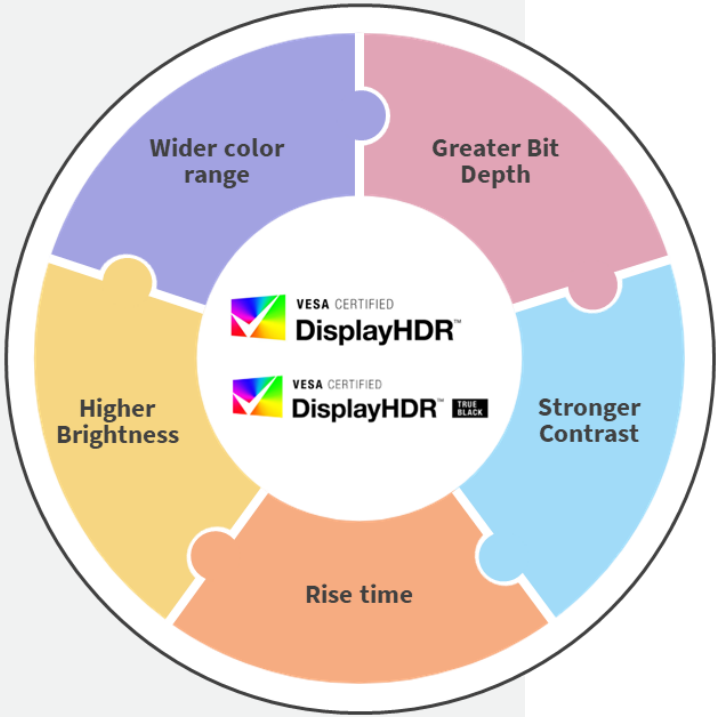
1. HDR vs. SDR

DisplayHDR Introduction

1. Logo
2. Entry Level & High Performance
3. Focus on Sink (Panel)
4. Test equipment

DisplayHDR CTS r1.2 Update

1. New Criteria
2. 5 New test items
3. DisplayHDR CTS r1.2 Timeline



GRL Worldwide Locations

- Silicon Valley HQ, 9 labs around the world, > 350 employees
- Recognized World Leader in Test Services and Automation Solutions for Connectivity and Charging

WW HQ & Lab
Santa Clara, CA

US R&D
Austin, TX

Taiwan Lab
Taipei

India R&D & Lab
Bangalore

Japan Lab
Yokohama

Korea Lab
Incheon

Asia Pacific HQ
Singapore

Malaysia R&D
Penang

China Lab
Shanghai

China Lab
Dongguan

Germany Lab
Karlsruhe

Belgium Lab
Hasselt

DP LRD Active Cable Testing Challenges and DP2.1 Connector Certification

Lexus Lee

Allion Labs,Inc

2024/10/4

Overview

- VESA LRD Active Cable Testing Challenges
- VESA Enhanced Connector Compliance Test Introduction

Overview

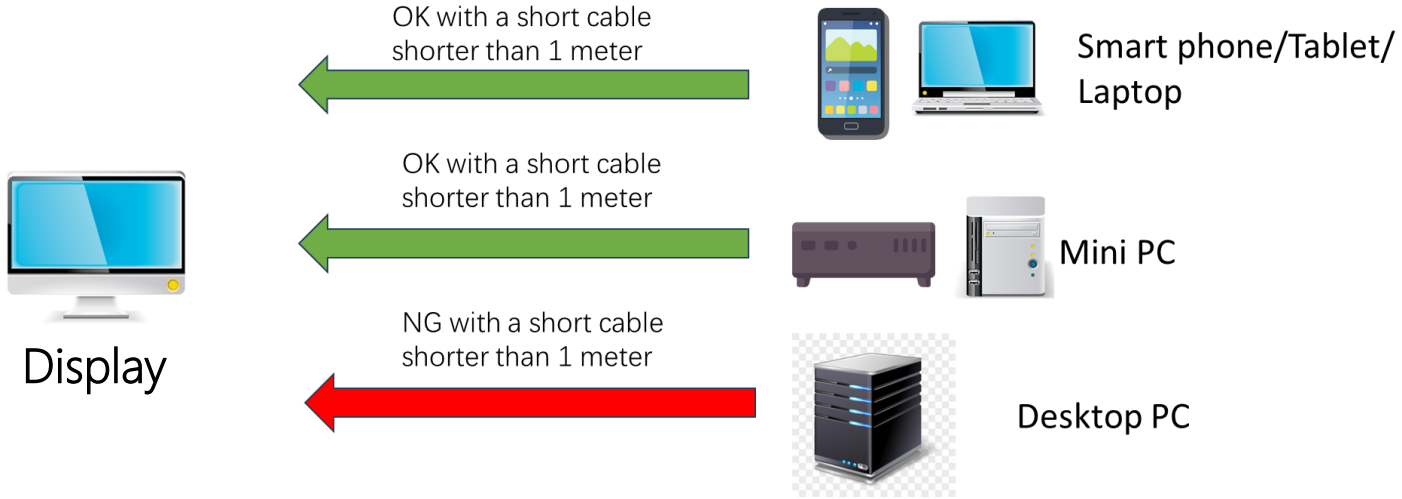
- VESA LRD Active Cable Testing Challenges
- VESA Enhanced Connector Compliance Test Introduction

The Current UHBR Passive Cable Status

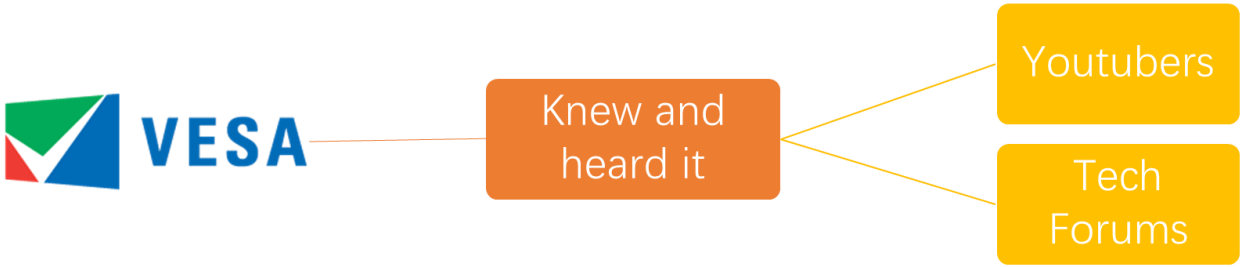
- DP to DP and USB-C to DP Passive cables for UHBR transmission
  - According to DP2.1a spec
    - UHBR 20-Capable Passive cable length: around 1 meter
    - UHBR 13.5-Capable Passive cable length: around 2 meters

- Criticism of UHBR20 ecosystem from youtubers and tech forums.

The Current UHBR Passive Cable Status Cont’



DisplayPort LRD Active Cable Solution

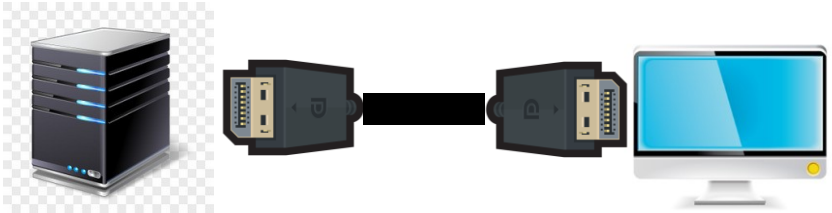


- VESA is going to bring us a solution to the criticism this year.
  - LRD Active Cable Solution
    - Get UHBR20 transmission to successfully work longer than 2 meter-long cable.
    - Creating a LRD Active Cable CTS

CTS Testing Challenges

- Knowledge to get DP LRD cable to work up
  - AUX and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Aux P: Pull down to GND
2. Aux N: Pull high to 2.89~3.6V.
3. DP_PWR:2.89~3.6V
4. Aux transaction if needed

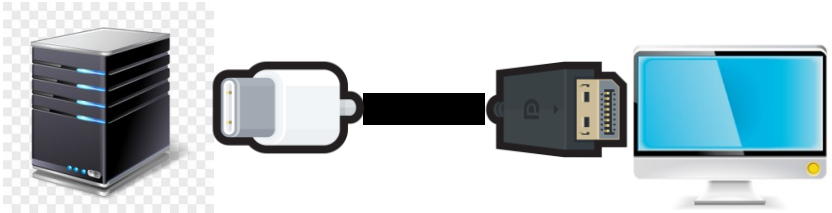


1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull high to 2.25~3.6V
5. Aux transaction if needed

CTS Testing Challenges Cont’

- Knowledge to get C to DP LRD cable to work up
  - Vconn, AUX, and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Vconn:3.0~5.5V
2. DP alt mode exerciser if needed.
3. Aux circuitry if needed.
4. Aux transaction if needed



1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull High to 2.25~3.6V
5. Aux transaction if needed

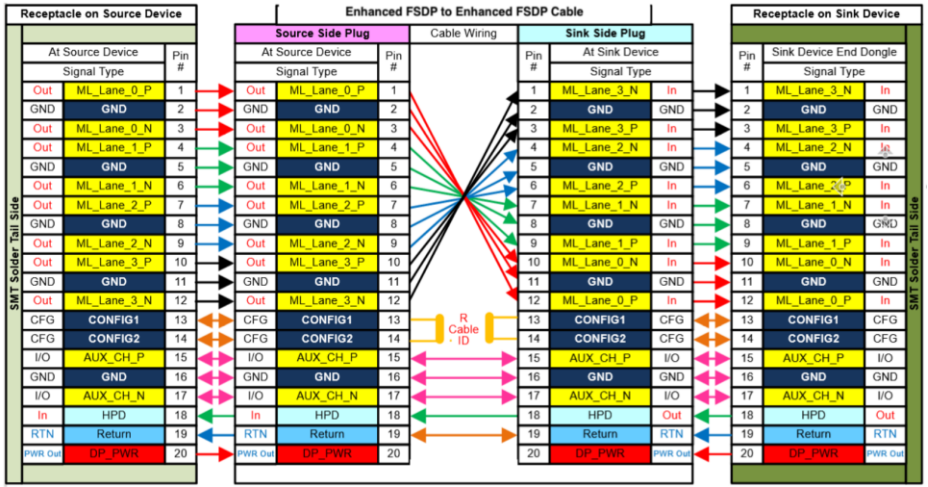
CTS Testing Challenges Cont’

- Power Consumption Check Before You Start Any Test
  - Do Link Training for
    - 1 Lane
    - 2 Lanes
    - 4 Lanes
  - Observe the current change of Vconn or DP PWR.
    - For example

	1 Lane	2 Lanes	4 Lanes
Current	80mA	170mA	380mA

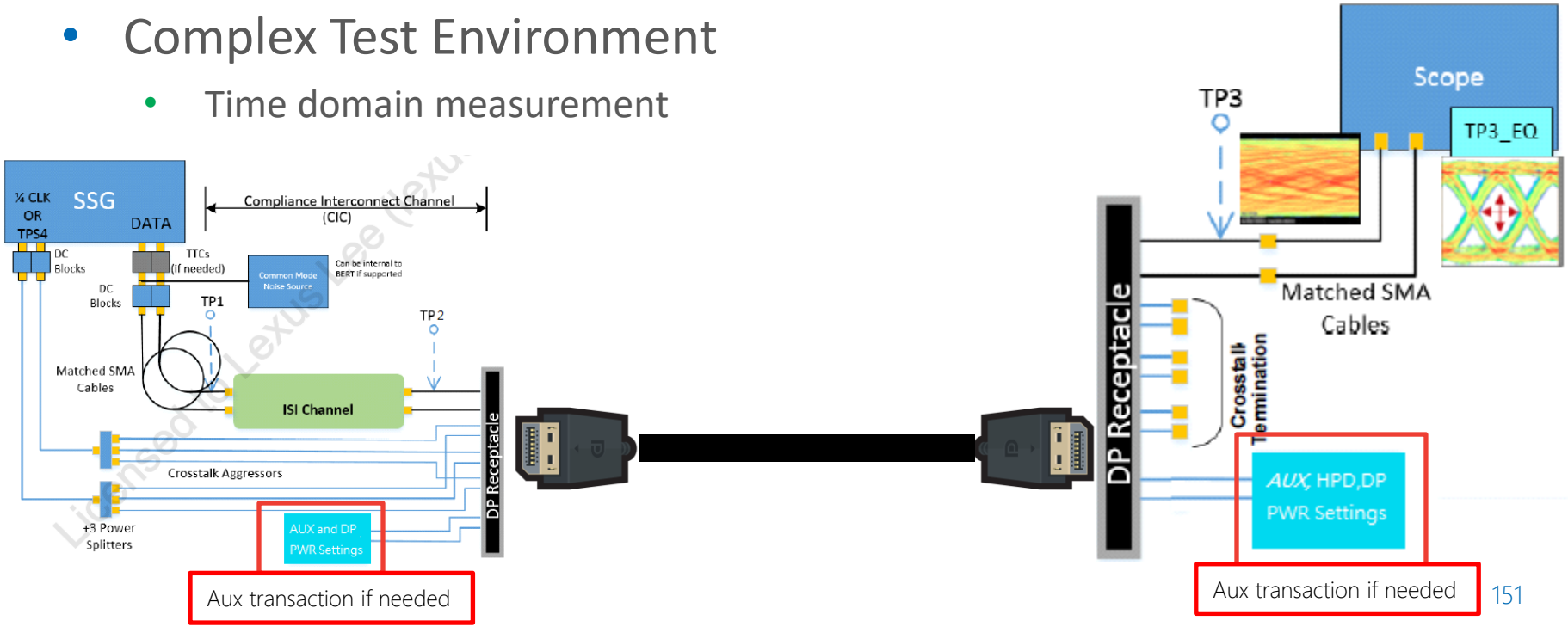
CTS Testing Challenges Cont’

- Know how the wires inside a DP cable are connected at both ends.
  - Look at high speed pairs, please



CTS Testing Challenges Cont’

- Complex Test Environment
  - Time domain measurement

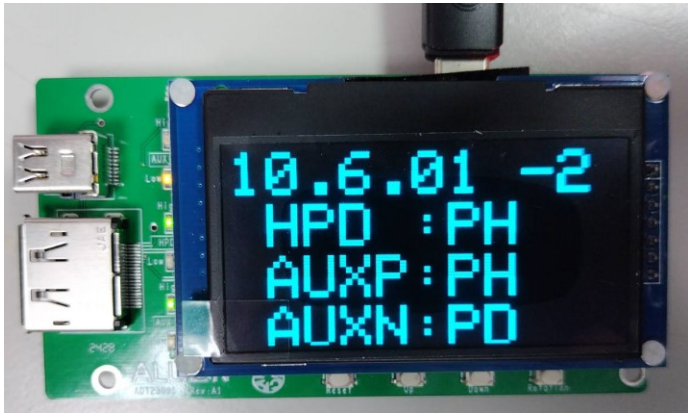


CTS Testing Challenges Cont’

- Complex Test Environment
  - Frequency domain measurement

CTS Testing Challenges Cont’

- Allion Test Fixture
  - Help to reduce the complex connection for your LRD cable testing.
    - Powered by USB-C port
    - Controllable HPD, AUX_P, and AUX_N

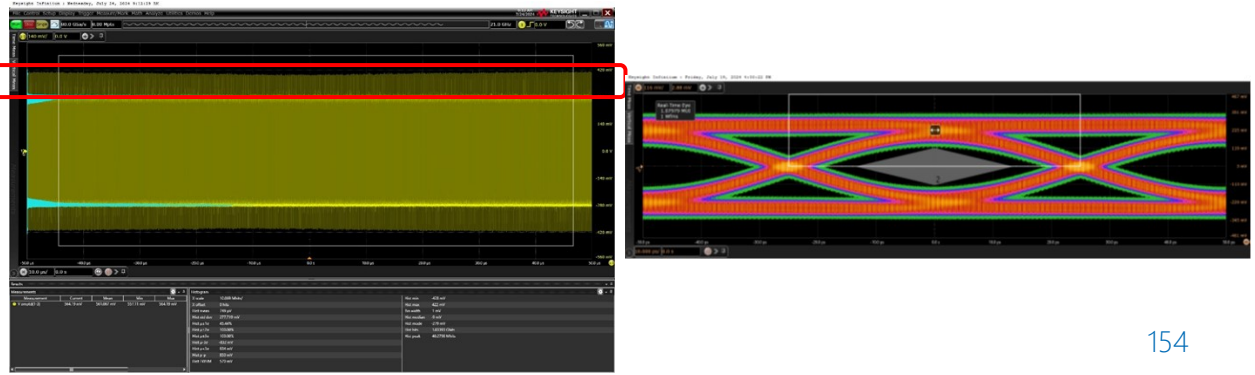


CTS Testing Challenges Cont’

- Stressed Signal Generator
  - Preset Calibration
    - Very important to stressed signal defined by DP spec.
    - Inaccurate preset number gets your stressed signal to highly not meet the expected ISI jitter, Eye Height, and Eye width.

Table 3-57: Preset FFE Coefficients[a] [b]

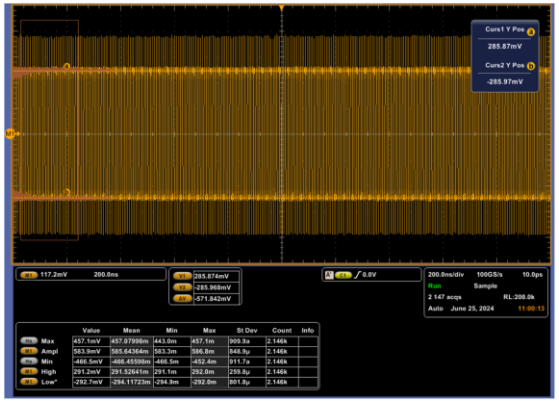
Preset Configuration #	Preshoot (dB)	De-emphasis (dB)	Informative Filter Coefficients		
			C_{-1}	C_0	C_{+1}
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0

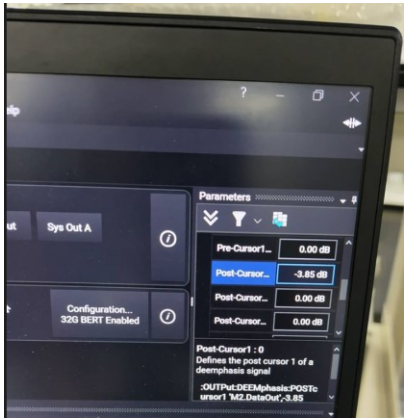


CTS Testing Challenges Cont’

- Stressed Signal Generator Cont’
  - Preset Calibration Cont’
    - Do not just enter the number that you want into your SSG FFE setting.

(SQ128) Rough De-emphasis: 20 log(585.6/923.4)=-3.95dB





Overview

- VESA LRD Active Cable Testing Challenges
- VESA Enhanced Connector Compliance Test Introduction

Latest DisplayPort Connector Spec Cont'

- Connector Types:

Type	Definition
Legacy	• Supports up to 8.1Gbps/lane(HBR) • Includes both an fsDP and an mDP version
Enhanced	• Enhanced fsDP Type 1 connector supports up to 13.5Gbps/lane(UHBR13.5) • Enhanced fsDP Type 2 connector supports up to 20Gbps/lane(UHBR20) • Enhanced mDP connector supports up to 20Gbps/lane(UHBR20)

Latest DisplayPort Connector Spec Cont'

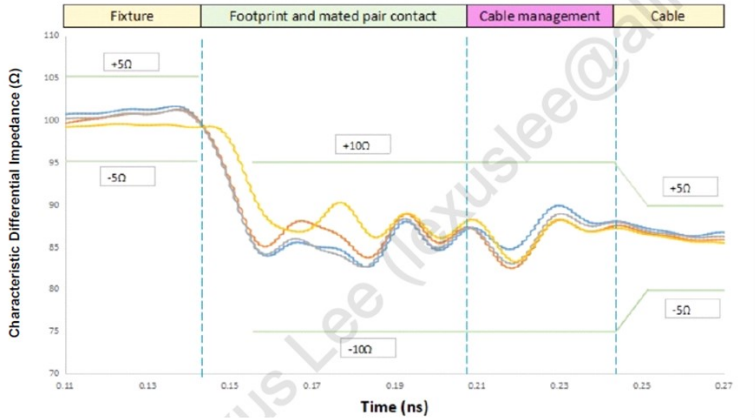
- Footprint Compatibility Matrix:

fsDP Conn/Footprint Type	Legacy PCB Footprint	Enhanced PCB Footprint Type 1	Enhanced PCB Footprint Type 2
Legacy	OK with HBR3	OK with HBR3	Ok with HBR3
Enhanced Type 1	N/A	OK with UHBR13.5	N/A
Enhanced Type 2	N/A	N/A	OK with UHBR20

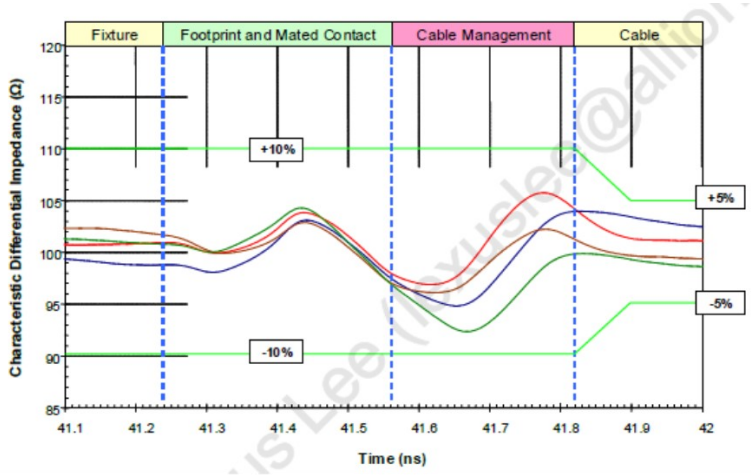
mDP Conn/Footprint Type	Legacy PCB Footprint	Enhanced PCB Footprint
Legacy	OK with HBR3	N/A
Enhanced	N/A	OK with UHBR20

Latest DisplayPort Connector Spec Cont'

- Discrepancy of Impedance:



Enhanced DP/mDP Connector

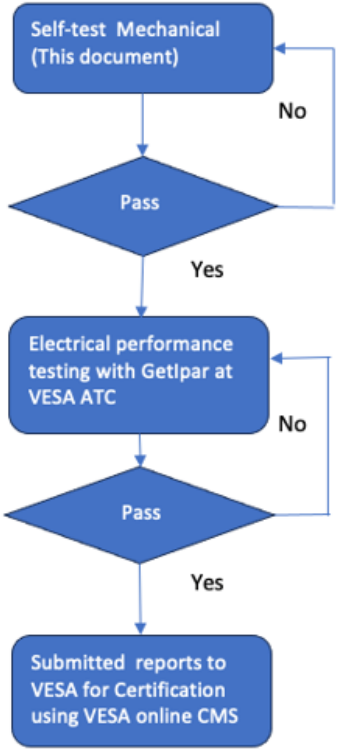


Legacy fsDP Connector

DP Enhanced Connector Compliance program

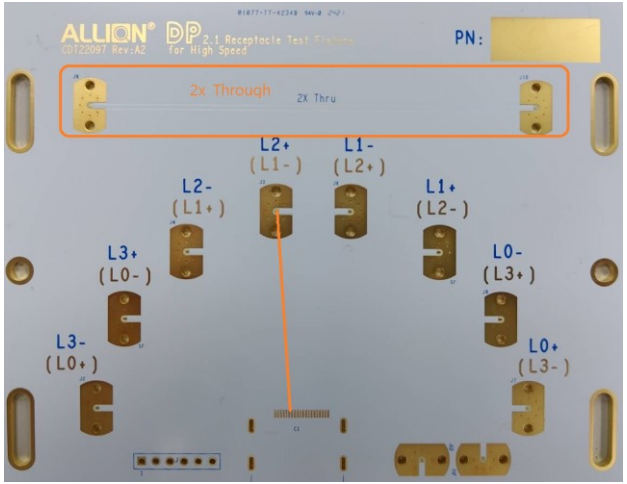
- Certification Flow:

VESA® DisplayPort™ Self-Test Report for Connectors
v2.1



DP Enhanced Connector Compliance Program Cont'

- Test Fixture Check:
  - Intra-pair skew < or = 2ps
  - 1x&2x thru accuracy check
    - (2x through length)/2 < or = 1x through length
    - In order to avoid compensating too much.



DP Enhanced Connector Compliance Program Cont'

- Test Concept:
  - Test the Connector DUT with a certified cable
    - Pass/ Fail Criteria based on the "cable" requirement defined in the DP2.1a spec.
  - Test the certified cable with one of the Known Good Receptacle fixtures(KGF)
    - KGF1 and KGF2 are Bizlink and Wieson respectively
    - Test data submitted as a reference

Thank you

DP 2.1a Design Notes

Jay Lin
Senior Technical Manager
Realtek Semiconductor Corp
linsp@realtek.com

Improvements in DP 2.1a

- Improved Cable program
  - DP54 for UHBR13.5
    - Passive cable up to 2m
  - DP80 for UHBR20
    - Passive cable up to 0.8m
- Refined new features
  - LTTPR
  - AUX-less ALPM and Panel Replay
  - DP Tunneling over USB4 v2

Utilize More BW - Gaming

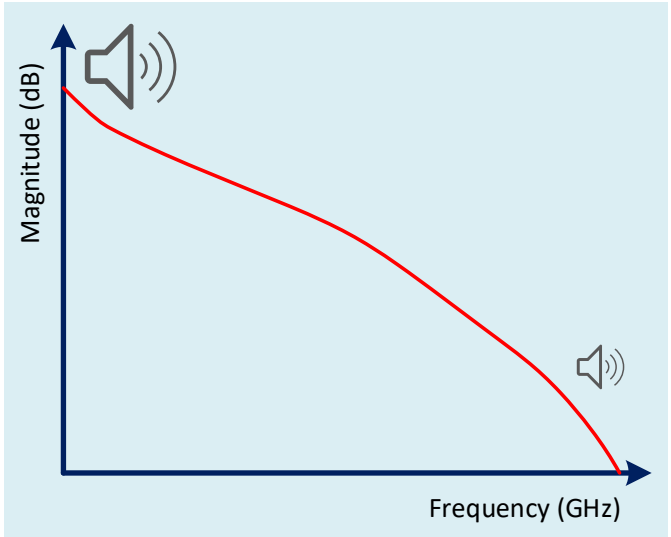
- Higher refresh rate gaming made possible
  - Improved motion blur
- Note
  - The portion of Vblank period increases along with the refresh rate
  - CVT 2.1 spec has minimum Vblank requirement to ensure Source and Sink interop
    - 460us in general
    - 300us if Adaptive Sync is support
  - Panel vendors may not be aware of this limitation
    - Scaler may not be able to cover the conversion from a large Vblank to small Vblank

Utilize More BW – Multi-Stream Transmission

- UHBR operation is a lot different from HBRx operation
  - 128b/132b channel coding vs 8b10b channel coding
  - Inherent MST capable framework
- Note
  - UHBR MST hub or Daisy-Chaining monitors need to support down-conversion
    - The number of streams that can be handled could be limited
  - Features are handled differently
    - DSC
    - Adaptive Sync
    - Panel Replay
  - Need comprehensive validation coverage

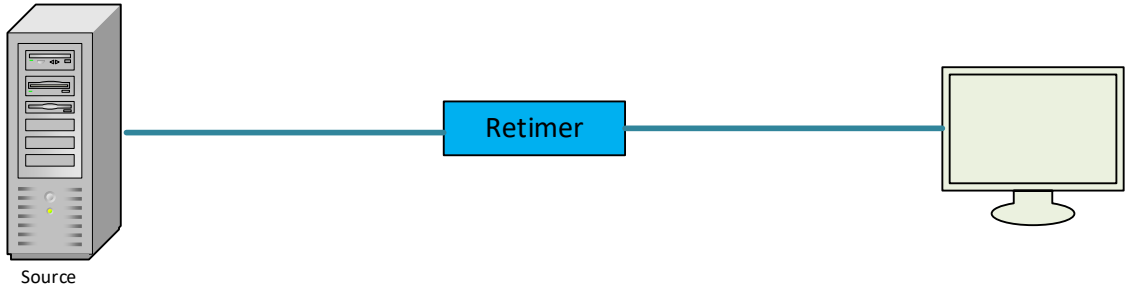
Utilize More BW – Signal Integrity

- Loss budget is very limited
  - Loss per inch of PCB is higher
- Note
  - PCB routing
  - PCB material
  - Choice of components
    - Be sure to check the device characteristic
      - Capacitive and inductive effects
  - Some sort of redriver/ retimer device may be needed



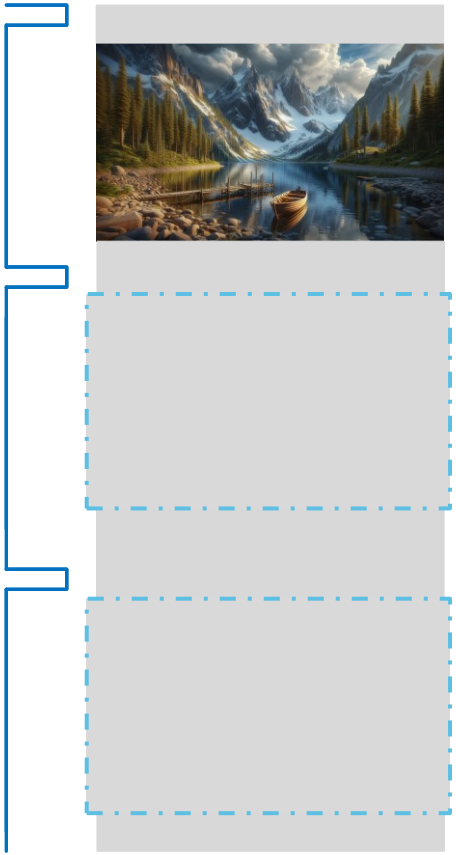
Link Training Tunable PHY Retimer (LTTPR)

- Each hop along the path can be trained to the required swing/ pre-emp setting
- The spec allows up to 6 LTTPRs along the path
  - Source/ Cable/ U4 dock/ Sink
- Note
  - LTTPR is crucial in building a stable link. Make sure the LTTPR passed all CTS requirements
  - Both 8b10b and 128b132b mode link training should be verified



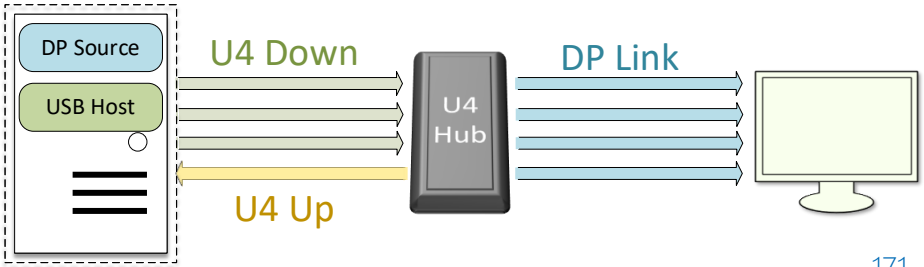
AUX-less ALPM Plus Panel Replay and Adaptive Sync

- Reduce system power consumption
  - Advanced Link Power Management
    - Turn off main link to save power
  - Panel Replay
    - Monitor replay previously stored image
  - Adaptive Sync
    - Varying refresh rate
  - Combining all three features achieves best power saving
- Note
  - Devices should comply with DP 2.1a spec instead of reuse of similar eDP IP



DP Tunneling over USB4

- USB4 v2 supports DP tunneling UHBR rate
  - Asymmetric mode of operation provides sufficient bandwidth for UHBR20 plus high-speed USB data
  - BW management with finer granularity
- Note
  - Dock design shall consider working in native DP mode as well
    - LTTPR like behavior
  - Design validation should cover all possible scenarios
    - Channel coding
    - SST vs MST
    - DP tunneling vs native DP
    - C to C vs. C to DP connection



Realtek's Worldwide 1st UHBR20 Solutions

- Realtek released worldwide 1st UHBR20 capable Tx and Rx solution and certified as reference design back in 2022
  https://vesa.org/featured-articles/first-vesa-displayport-2-0-video-source-and-sink-devices-complete-displayport-uhbr-ultra-high-bit-rate-certification/
- Realtek's scaler solution is adopted in the worldwide 1st UHBR20-capable monitor
- UHBR20 capable Source is still limited but expect to see increase in 2025

Realtek Solution Lineup

RTD2739
- DP 2.1 UHBR20
- 8K60/ UHD240
- 5K+ Zone Local Dimming
- Owl Sight II
- Eagle Sight II

MP

RTD2190E / RTD2180E
- Receiver:
  DP2.1 UHBR20
- Transmitter 3x DFP:
  2x DP2.1 UHBR20/HDMI2.1 FRL 12G combo (2190E)
  2x DP1.4 HBR3/HDMI2.1 FRL 12G combo (2180E)
  1x HDMI2.1 FRL 12G
- OSD
- Aux/I2C Sniffer
- Video Splitter
- USB2 FW update
- 9.5x9.5mm BGA

MP

RTD2151E
- FRL 12G retimer
- Advanced error handling
- Ultra low power

MP

RTD2156
- USB4 Version 1 retimer
- USB4 Gen 3×2 (40Gbps x 2 lanes)
- DP2.1/TBT Alt-mode
- 3.3V/0.9V (& 1.8V optional)
- 6.5x4.5mm CFP 104-ball BGA

ES: Q4'24
MP: Q1'25

RTD2158
- DP2.1a retimer
- UHBR20
- LTTPR
- 7x7mm QFN56

ES: Q4'24
MP: Q1'25

VESA

GET READY!!

Compliance Testing

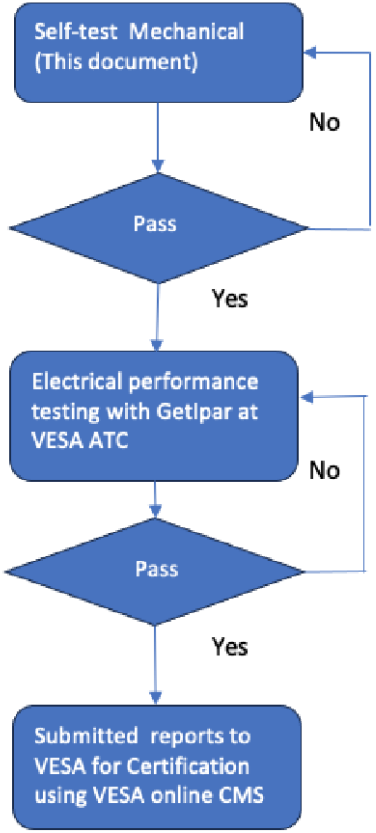
Compliance Test Specification Updates

VESA has updated base specification and CTS documents in past two years

- DP 2.1a Spec update – released 12/2023
- DP 2.1 PHY CTS v1.0 – released 6/23
- DP 2.1 Link CTS v1.0 – released 11/2023
- Enhanced DP Connector Self-Test v2.1 – 8/2024
- DP Alt Mode CTS v2.1 – 8/2024
- Embedded DP (eDP) – 9/2024

Enhanced Connectors

- UHBR rates = the need for high performance DP connectors
- VESA created specification and test requirements for Enhanced DP connectors (fsDP and mDP)
- This includes both right angle and vertical mount connectors



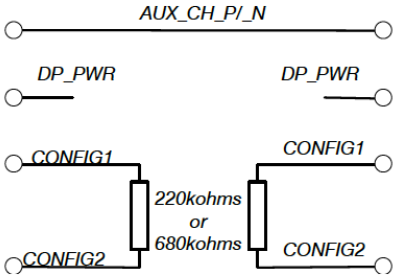
DP40, DP54 and DP80 Cable Specification and Certification program

- Work on Enhanced DP cable and connector specifications and test requirements started in 2021 to ensure high performance connectors and cables would be available for products supporting UHBR rates
- DP40, DP54 and DP80 Certified cables provide added assurance of proper operation at the highest link rates (UHBR10, UHBR13.5 and UHBR20 Gbps)
- Over 150 Enhanced DP cables and connectors have been certified since launch of the Enhanced DP cable and connector certification programs
- DP40 cable performance tier replaced with DP54 in 2024
- DP54 cables are required to support UHBR10 and UHBR13.5 link rates, enabling longer cables for sources and sinks that implement 13.5Gbps as highest link rate

DP54 cables replace DP40

DP40	DP80	
UHBR10	UHBR13.5	UHBR20
10GbpsX4 lanes	13.5GbpsX4 lanes	20GbpsX4 lanes
~3 meters max	~1 meter max length	
DP54 (DP 2.1a specification)		**DP80**
UHBR10	UHBR13.5	UHBR20
10GbpsX4 lanes	13.5GbpsX4 lanes	20GbpsX4 lanes
~3 meters max length		~1 meter max

Cable ID used to detect cable caps



Product certifications* 2022/2023/2024

Products	2022	2023	2024
DP Sources	141	99	60
DP Sinks	339	277	320
DP Cables	42	59	56
DisplayHDR	388	397	369
ClearMR	14	45	30
AdaptiveSync	25	80	48

*Note: numbers are base model certs not including family models

VESA PlugTest Events

- Provide significant value to member companies, particularly as new capabilities and products are deployed.
- Demonstrate and improve Traditional Interoperability
- Test Native DP and DP Alt Mode over USB Type-C™ products
  - UHBR rates, DSC, FEC, DisplayHDR and other new capabilities
  - Verify Test Equipment Correlation
- VESA hosted two successful PlugTests in 2023 (Taiwan and US)
- VESA hosts two PlugTests in 2024
  - Hawaii, USA: **Q1 2024 (completed)**
  - Taipei, Taiwan: **Q4 2024 (Oct 14-18th Taiwan)**

PlugTest Updates - be ready

- Preset calibration and checks
- Minimum Vblank/Hblank tests
- Audio test updates
- DP VIF tool and TE correlation
- DP 2.1 LL test equipment correlation
- DPAM TE correlation

DP Specification & CTS versions

- Many product developers incorrectly use DP specification version to mean max link rate:
  - DP 1.2 (HBR2) , DP 1.4 (HBR3) and DP 2.1 (UHBR rates)
- Technically this is incorrect but easy to understand
- However, VESA certification will require all new product certifications to use latest CTS requirements for any product regarless of max link rate
- This is most important for DP 2.1 Link CTS & DP Alt Mode CTS which includes many updates and corrections to fix product interop issues
- Timeline for enforcement of this requirement is under discussion in VESA compliance team – current proposal is Q1 2025

DP 2.1 Audio CTS Challenges

Sergey Grushin
Unigraf
9.10.2024

Audio CTS Challenges

1. Streaming high sample rate audio at RB timings
2. Audio test time
3. Audio samples distribution during blanking period

Audio CTS (Challenge #1 – 192Khz 8ch)

						SSC	TRUE	0,994					
				(Hz)	(MHz)	FEC	TRUE	0,97			SST		
Hactive	Vactive	Htotal	Hblank	V Freq	Pixel Freq	lane	link_rate	symbol size	2ch, SST AudioSymbolCntReqPerHBlank	8ch, SST AudioSymbolCntReqPerHBlank	StrmSymbolCntAvailPerHBlank	2ch, isValid	8ch, isValid
1920	1080	2000	80	30	65,76	1	162	8	65	254	165	TRUE	FALSE
1920	1080	2000	80	60	133,32	1	162	8	44	127	66	TRUE	FALSE
1920	1080	2000	80	144	333,216	4	162	8	24	88	92	TRUE	TRUE
1920	1080	2000	80	144	333,216	2	270	8	22	86	92	TRUE	TRUE
1920	1080	2000	80	144	333,216	1	540	8	22	85	98	TRUE	TRUE
3840	2160	3920	80	30	257,661	4	162	8	48	128	136	TRUE	TRUE
3840	2160	3920	80	30	257,661	2	270	8	44	128	130	TRUE	TRUE
3840	2160	3920	80	30	257,661	1	540	8	44	127	136	TRUE	TRUE
3840	2160	3920	80	60	522,614	4	162	8	24	88	36	TRUE	FALSE
3840	2160	3920	80	60	522,614	2	540	8	22	86	128	TRUE	TRUE
3840	2160	3920	80	60	522,614	1	810	8	22	85	93	TRUE	TRUE
3840	2160	3920	80	144	1306,206	4	540	8	24	44	68	TRUE	TRUE
3840	2160	3920	80	144	1306,206	2	810	8	22	44	62	TRUE	TRUE
5120	2160	5200	80	30	341,796	4	162	8	48	128	88	TRUE	FALSE
5120	2160	5200	80	30	341,796	2	270	8	44	128	88	TRUE	FALSE
5120	2160	5200	80	30	341,796	1	540	8	44	127	95	TRUE	FALSE
5120	2160	5200	80	60	693,264	4	270	8	24	88	60	TRUE	FALSE
5120	2160	5200	80	60	693,264	2	540	8	22	86	86	TRUE	FALSE
5120	2160	5200	80	60	693,264	1	810	8	22	85	62	TRUE	FALSE
5120	2160	5200	80	120	1427,088	4	540	8	24	44	60	TRUE	TRUE
5120	2160	5200	80	144	1732,723	4	540	8	24	44	36	TRUE	FALSE
7680	4320	7760	80	30	1019,896	4	540	8	24	88	108	TRUE	TRUE
7680	4320	7760	80	30	1019,896	2	810	8	22	86	90	TRUE	TRUE
7680	4320	7760	80	60	2068,66	4	810	8	24	44	64	TRUE	TRUE
10240	4320	10320	80	30	1356,357	4	540	8	24	88	64	TRUE	FALSE
10240	4320	10320	80	30	1356,357	2	810	8	22	86	58	TRUE	FALSE
10240	4320	10320	80	60	2751,105	4	810	8	24	44	32	TRUE	FALSE

Audio tests (Challenge #2 – Test Time)

- Source DUT
  - No Sources supporting DP Test Automation for Audio.
  - Around 2h to execute Audio tests for Source devices at non-UHBR link rates. (test 4.4.4.5 requires around 30 minutes of test operator time).
- Sink DUT
  - Listening check is required when test Sink devices.
  - Around 2h to execute Audio tests for Sink devices at non-UHBR link rates.
- Extending test procedures to cover UHBR link rates and DSC configurations estimated to double test time.

Audio CTS (Challenge #3)

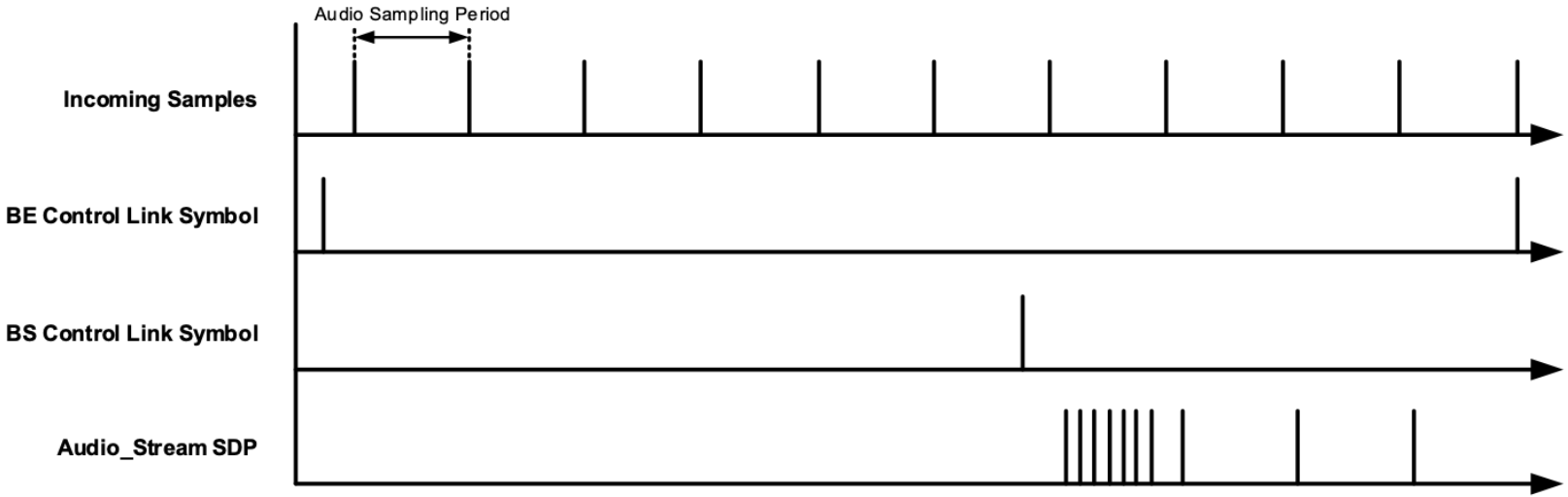


Figure A-2: Audio_Stream SDPs Transfer with Video during Video VActive Period

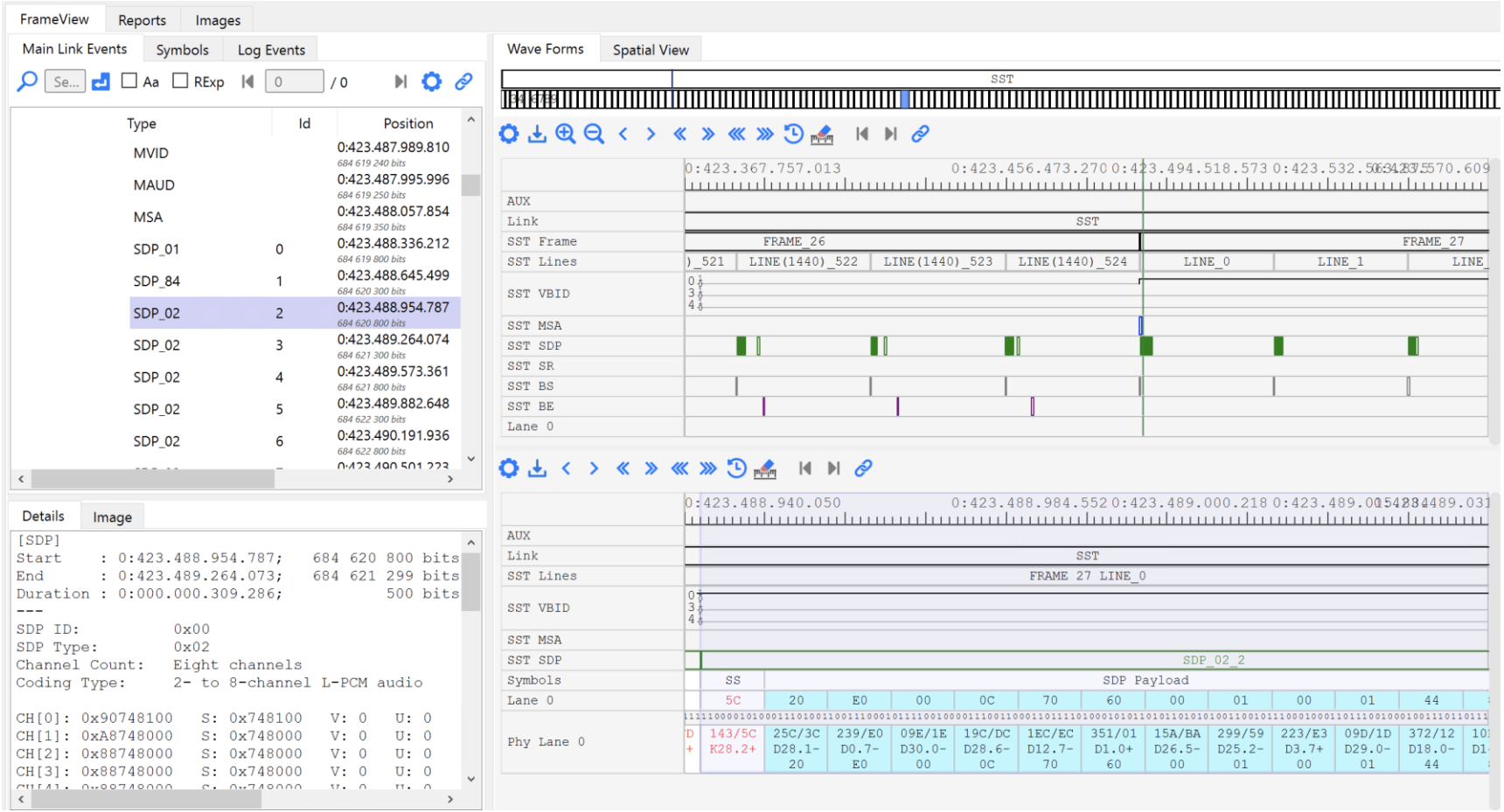
Audio CTS (Challenge #3) continued

$$floor(\frac{nF_s H_{total}}{F_p}) - 4 \le S_{tx} \le floor(\frac{nF_s H_{total}}{F_p}) + 4$$

where:

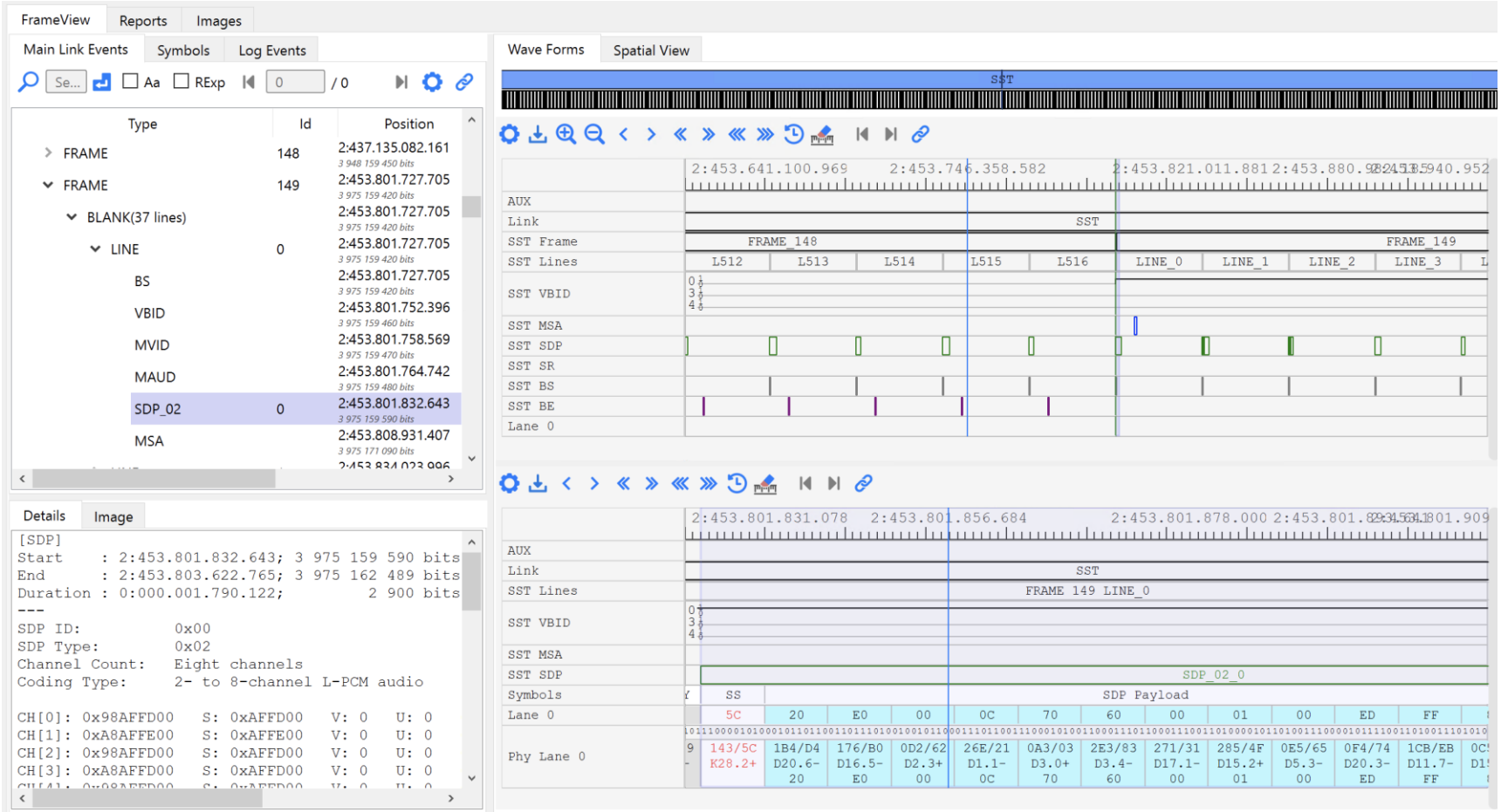
- S_{tx} is the number of audio samples received from the Source DUT over n consecutive lines
- F_s is the nominal audio sampling rate
- H_{total} is the horizontal total
- F_p is the pixel rate
- n is the number of lines

Source #1

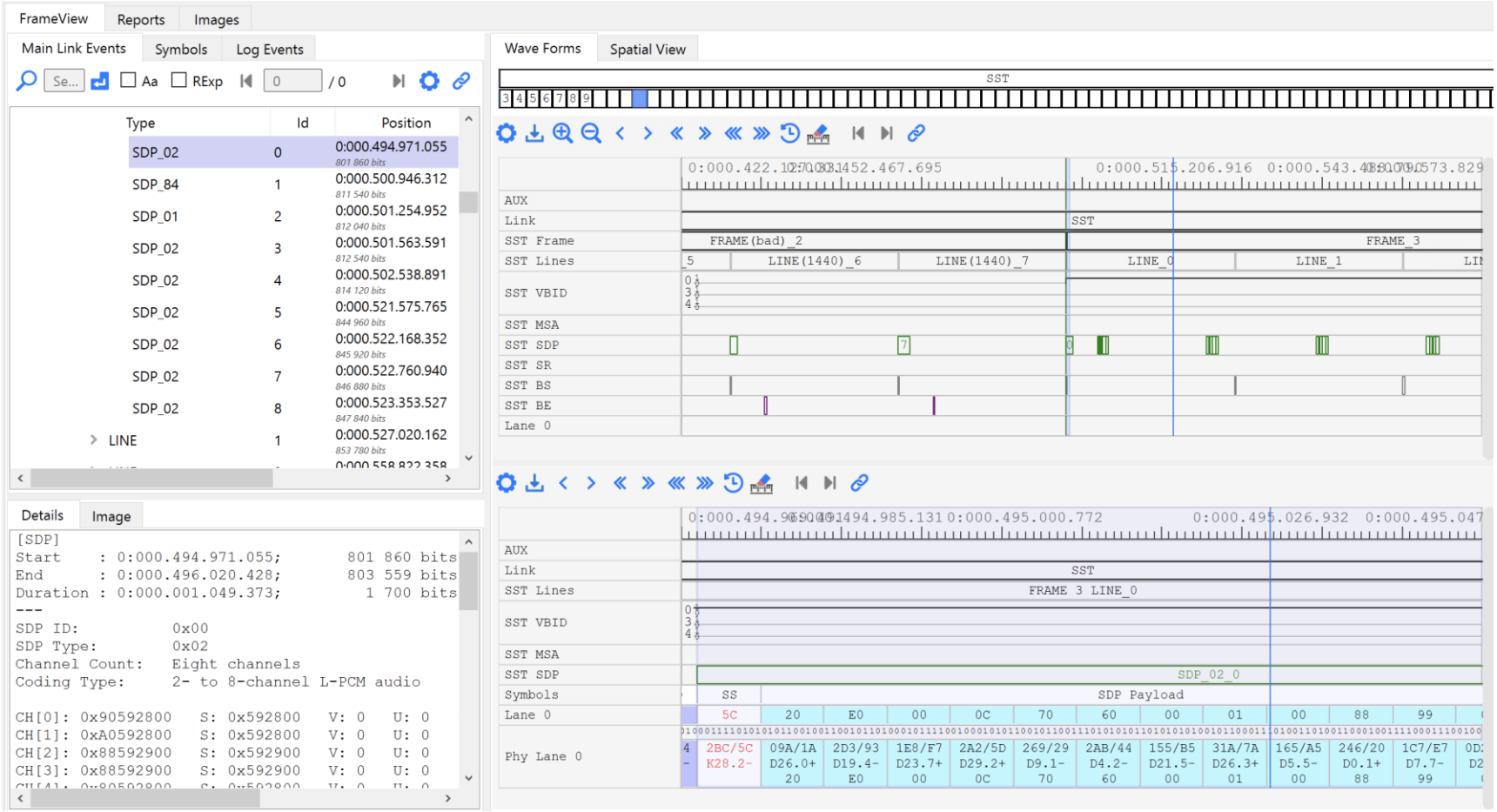

FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Se...
Aa
RExp
0
/ 0
Type
Id
Position
MVID
0:423.487.989.810
684 619 240 bits
MAUD
0:423.487.995.996
684 619 250 bits
MSA
0:423.488.057.854
684 619 350 bits
SDP_01
0
0:423.488.336.212
684 619 800 bits
SDP_84
1
0:423.488.645.499
684 620 300 bits
SDP_02
2
0:423.488.954.787
684 620 800 bits
SDP_02
3
0:423.489.264.074
684 621 300 bits
SDP_02
4
0:423.489.573.361
684 621 800 bits
SDP_02
5
0:423.489.882.648
684 622 300 bits
SDP_02
6
0:423.490.191.936
684 622 800 bits
Details
Image
[SDP]
Start : 0:423.488.954.787; 684 620 800 bits
End : 0:423.489.264.073; 684 621 299 bits
Duration : 0:000.000.309.286; 500 bits

SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x90748100 S: 0x748100 V: 0 U: 0
CH[1]: 0xA8748000 S: 0x748000 V: 0 U: 0
CH[2]: 0x88748000 S: 0x748000 V: 0 U: 0
CH[3]: 0x88748000 S: 0x748000 V: 0 U: 0
Wave Forms
Spatial View
SST
0:423.367.757.013
0:423.456.473.270
0:423.494.518.573
0:423.532.563.875
0:423.570.609
AUX
Link
SST
SST Frame
FRAME_26
FRAME_27
SST Lines
)_521
LINE(1440)_522
LINE(1440)_523
LINE(1440)_524
LINE_0
LINE_1
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
0:423.488.940.050
0:423.488.984.552
0:423.489.000.218
0:423.489.031
SST
FRAME 27 LINE_0
SDP_02_2
Symbols
SS
SDP Payload
5C
20
E0
00
0C
70
60
00
01
00
01
44
Phy Lane 0
143/5C K28.2+
25C/3C D28.1- 20
239/E0 D0.7- E0
09E/1E D30.0- 00
19C/DC D28.6- 0C
1EC/EC D12.7- 70
351/01 D1.0+ 60
15A/BA D26.5- 00
299/59 D25.2- 01
223/E3 D3.7+ 00
09D/1D D29.0- 01
372/12 D18.0- 44

Source #2

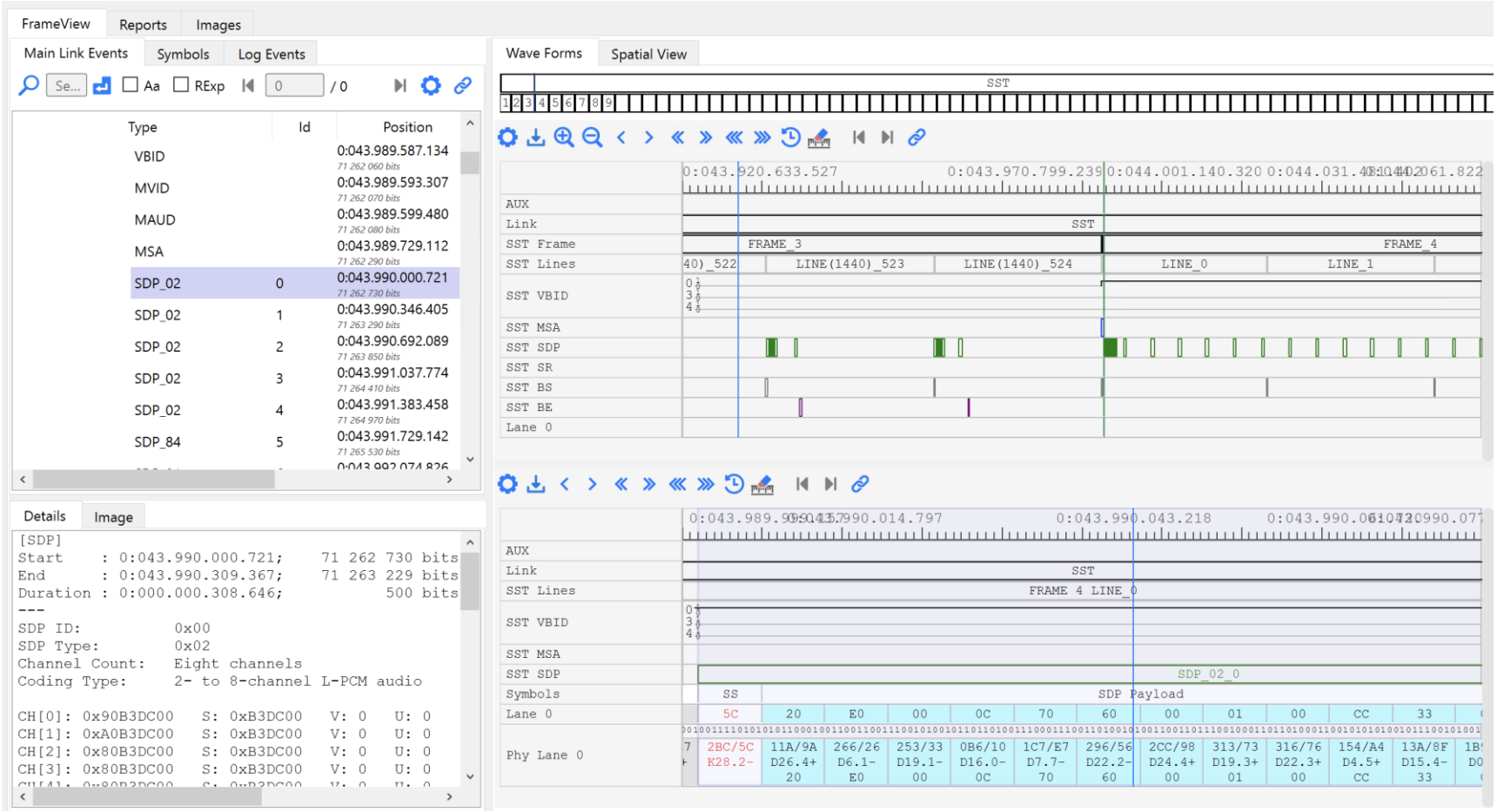

FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Aa
RExp
/ 0
Type
Id
Position
FRAME 148 2:437.135.082.161
FRAME 149 2:453.801.727.705
BLANK(37 lines) 2:453.801.727.705
LINE 0 2:453.801.727.705
BS 2:453.801.727.705
VBID 2:453.801.752.396
MVID 2:453.801.758.569
MAUD 2:453.801.764.742
SDP_02 0 2:453.801.832.643
MSA 2:453.808.931.407
Details
Image
[SDP]
Start : 2:453.801.832.643; 3 975 159 590 bits
End : 2:453.803.622.765; 3 975 162 489 bits
Duration : 0:000.001.790.122; 2 900 bits
SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x98AFFD00 S: 0xAFFD00 V: 0 U: 0
CH[1]: 0xA8AFFE00 S: 0xAFFE00 V: 0 U: 0
CH[2]: 0x98AFFD00 S: 0xAFFD00 V: 0 U: 0
CH[3]: 0xA8AFFD00 S: 0xAFFD00 V: 0 U: 0
Wave Forms
Spatial View
SST
AUX
Link
SST Frame
SST Lines
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
FRAME 148
FRAME 149
L512
L513
L514
L515
L516
LINE_0
LINE_1
LINE_2
LINE_3
2:453.641.100.969
2:453.746.358.582
2:453.821.011.881
2:453.801.831.078
2:453.801.856.684
2:453.801.878.000
FRAME 149 LINE_0
SDP_02_0
Symbols
Phy Lane 0
SS
SDP Payload
5C
20
E0
00
0C
70
60
00
01
00
ED
FF
143/5C K28.2+
1B4/D4 D20.6- 20
176/B0 D16.5- E0
0D2/62 D2.3+ 00
26E/21 D1.1- 0C
0A3/03 D3.0+ 70
2E3/83 D3.4- 60
271/31 D17.1- 00
285/4F D15.2+ 01
0E5/65 D5.3- 00
0F4/74 D20.3- ED
1CB/EB D11.7- FF

Source #3


FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Se...
Aa
RExp
0
/ 0
Type
Id
Position
SDP_02 0 0:000.494.971.055 801 860 bits
SDP_84 1 0:000.500.946.312 811 540 bits
SDP_01 2 0:000.501.254.952 812 040 bits
SDP_02 3 0:000.501.563.591 812 540 bits
SDP_02 4 0:000.502.538.891 814 120 bits
SDP_02 5 0:000.521.575.765 844 960 bits
SDP_02 6 0:000.522.168.352 845 920 bits
SDP_02 7 0:000.522.760.940 846 880 bits
SDP_02 8 0:000.523.353.527 847 840 bits
LINE 1 0:000.527.020.162 853 780 bits
Details
Image
[SDP]
Start : 0:000.494.971.055; 801 860 bits
End : 0:000.496.020.428; 803 559 bits
Duration : 0:000.001.049.373; 1 700 bits

SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x90592800 S: 0x592800 V: 0 U: 0
CH[1]: 0xA0592800 S: 0x592800 V: 0 U: 0
CH[2]: 0x88592900 S: 0x592900 V: 0 U: 0
CH[3]: 0x88592900 S: 0x592900 V: 0 U: 0
Wave Forms
Spatial View
SST
AUX
Link
SST Frame
SST Lines
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
FRAME(bad)_2
FRAME_3
LINE(1440)_6
LINE(1440)_7
LINE_0
LINE_1
SDP_02_0
Symbols
SS
SDP Payload
Phy Lane 0

Source #4


FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Se...
Aa
RExp
0
/ 0
Type
Id
Position
VBID
0:043.989.587.134
71 262 060 bits
MVID
0:043.989.593.307
71 262 070 bits
MAUD
0:043.989.599.480
71 262 080 bits
MSA
0:043.989.729.112
71 262 290 bits
SDP_02
0
0:043.990.000.721
71 262 730 bits
SDP_02
1
0:043.990.346.405
71 263 290 bits
SDP_02
2
0:043.990.692.089
71 263 850 bits
SDP_02
3
0:043.991.037.774
71 264 410 bits
SDP_02
4
0:043.991.383.458
71 264 970 bits
SDP_84
5
0:043.991.729.142
71 265 530 bits
Details
Image
[SDP]
Start : 0:043.990.000.721; 71 262 730 bits
End : 0:043.990.309.367; 71 263 229 bits
Duration : 0:000.000.308.646; 500 bits

SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x90B3DC00 S: 0xB3DC00 V: 0 U: 0
CH[1]: 0xA0B3DC00 S: 0xB3DC00 V: 0 U: 0
CH[2]: 0x80B3DC00 S: 0xB3DC00 V: 0 U: 0
CH[3]: 0x80B3DC00 S: 0xB3DC00 V: 0 U: 0
Wave Forms
Spatial View
SST
0:043.920.633.527
0:043.970.799.239
0:044.001.140.320
AUX
Link
SST
SST Frame
FRAME_3
FRAME_4
SST Lines
LINE(1440)_523
LINE(1440)_524
LINE_0
LINE_1
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
0:043.990.014.797
0:043.990.043.218
FRAME 4 LINE_0
SDP_02_0
Symbols
SS
SDP Payload
5C
20
E0
00
0C
70
60
00
01
00
CC
33
Phy Lane 0
2BC/5C K28.2-
11A/9A D26.4+ 20
266/26 D6.1- E0
253/33 D19.1- 00
0B6/10 D16.0- 0C
1C7/E7 D7.7- 70
296/56 D22.2- 60
2CC/98 D24.4+ 00
313/73 D19.3+ 01
316/76 D22.3+ 00
154/A4 D4.5+ CC
13A/8F D15.4- 33

Audio CTS (Conclusions)

- No easy way to upgrade DP 1.4 8b/10b SST Audio tests to cover DP 2.1 requirements
- Due to test time increase, it is suggested to test Audio at UHBR rates under separate tests. Under discussion
- It is suggested to test Audio at 8b/10b link rates also in MST mode. Not covered yet by SCR under review. To be discussed

VESA Technology Development Areas

VESA technology development

VESA members are collaborating on several key technology areas

- Embedded DisplayPort - v2.0 (published Sept 2024)
- DP Tunneling over USB4 – compliance testing has begun
- AR/VR Task Group
  - Focused on creating solutions roadmap to meet performance, power and implementation requirements for future AR/VR needs. Specification is released. Work on CTS underway
- DP Automotive Extension Task Group
  - Working with automotive industry to address needs for high-resolution performance in this market segment
  - Working on DP AE CTS and testing
- Bulk Display Protocol
  - BDP specification and CTS nearing release
- Display Performance Metrics Task Group
  - DisplayHDR, ClearMR, AdaptiveSync

Summary

Summary

- Product shipments and certifications on based on VESA technologies continue to grow
- DP 2.1 UHBR capable product development and certifications have ramped up in 2024
- VESA Enhanced cable and connector certification programs have been very successful with significant numbers of DP40, DP54 and DP80 cables certified
- DisplayPort over USB-C is a game changer for small form factor and portable products and is now the defacto standard for laptops, tablets and handheld devices
- Display Performance Standards adoption and certification have been extremely successful the last several years
- Development and adoption of new technologies continues to drive increases in VESA membership growth

THANK YOU

DisplayPort.org
DisplayHDR.org
ClearMR.org
AdaptiveSync.org
VESA.org

Questions?

Teledyne LeCroy Test Solutions for DisplayPort v2.1

M42de 80G Video Analyzer/ Generator

TELEDYNE LECROY
Everywhereyoulook™

Contacts:
Protocol Test: Henry.Tsai@Teledyne.com
Electrical Test: Sam.Ho@Teledyne.com

Teledyne LeCroy Taiwan
7F., No. 667, Bannan Road
Zhonghe Dist.
New Taipei City 235
Phone: +886-2-8228-6100
Website: http://www.teledyne.com

Teledyne LeCroy DisplayPort Test Platforms

- **Quantumdata M42de Analyzer / Generator**
  - DisplayPort 2.1 UHBR Lane Rates
  - Deep Capture / Analysis
  - T.A.P.4™ Passive Monitoring
  - Comprehensive DP 1.4 & 2.1 Compliance Coverage
  - qdPrime™ Automated Test Suite

- **Quantumdata M21 Analyzer**
  - Portable DP Analyzer (up to UHBR 13.5Gb/s)
  - Aux Channel Monitoring

GRL
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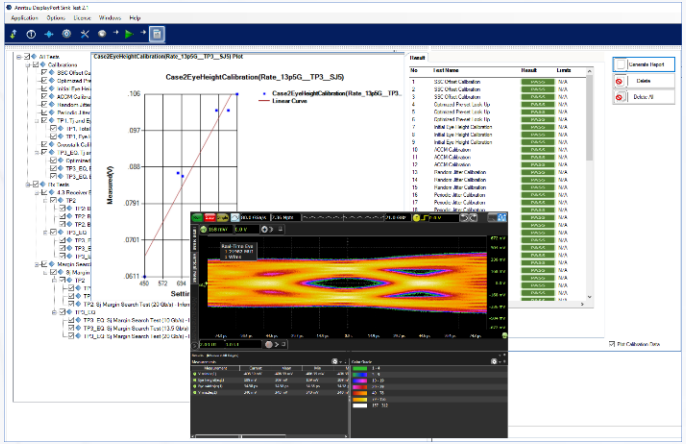
graniteriverlabs.com

GRL DisplayPort

2.1 Tx PHY Test Solution

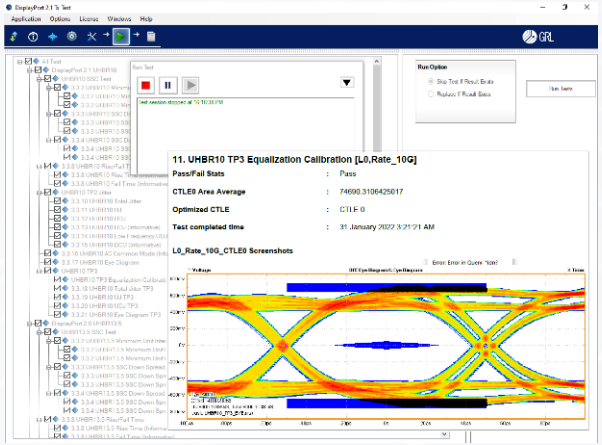
1.4/2.1 Rx PHY Test Solution



DisplayPort 1.4/2.1 Receiver Calibration and Test Automation

An automated and efficient way to test your DisplayPort 2.1 Sink Device (GRL-DP21-SINK-AN, GRL-DP14-SINK-AN)

24Q4 Note: The Preset calibration feature based on “SCR_DP 2.1 PHY CTS Preset Calibration d3” is planned to be added in the next SW release.



DisplayPort 2.1 Transmitter Test Automation Solution

A quick and straightforward way to test and debug your DisplayPort 2.1 transmitter products efficiently (GRL-DP21-TX)

UNIGRAF

DisplayPort

USB Type-C

sales.asia@unigraf.fi

UCD-500 Gen2

DP 2.1 Generator & Analyzer

- DP 2.1 and DP 1.4a Link Layer CTS Tool
- DP 2.1 Sinks and Sources up to 8K@60Hz (UHBR 20Gbps / Lane) and 16K@60Hz with DSC
- Supports DP and USB-C connectivity
- DP TX/RX Link Training, Power Delivery(USB-C), DSC, FEC, DPCD/EDID editor, Adaptive-Sync, HDCP 2.3, etc.
- Capture and logging functions
- Now featuring Link Analyzer, Panel Replay and eDP test functions

USB Type-C

DisplayPort

UNIGRAF

DisplayPort Alt Mode Compliance Testing and Analysis solutions

SYMBIOSYS ALLIANCE

Ellisys USB/DPAM Test and Analysis Solutions

USB Explorer™ 350

Multi-function USB Type-C®, USB 3.2, and Power Delivery Protocol Test Platform

VESA-Approved Tester for DisplayPort ALT Mode

Type-C Tracker™

Protocol and Electrical Analysis Tool for USB Type-C® Standards

Includes DP AUX and DP ALT Support

ellisys
Better Analysis

KEYSIGHT

Measurement Disaggregation

Contact Information
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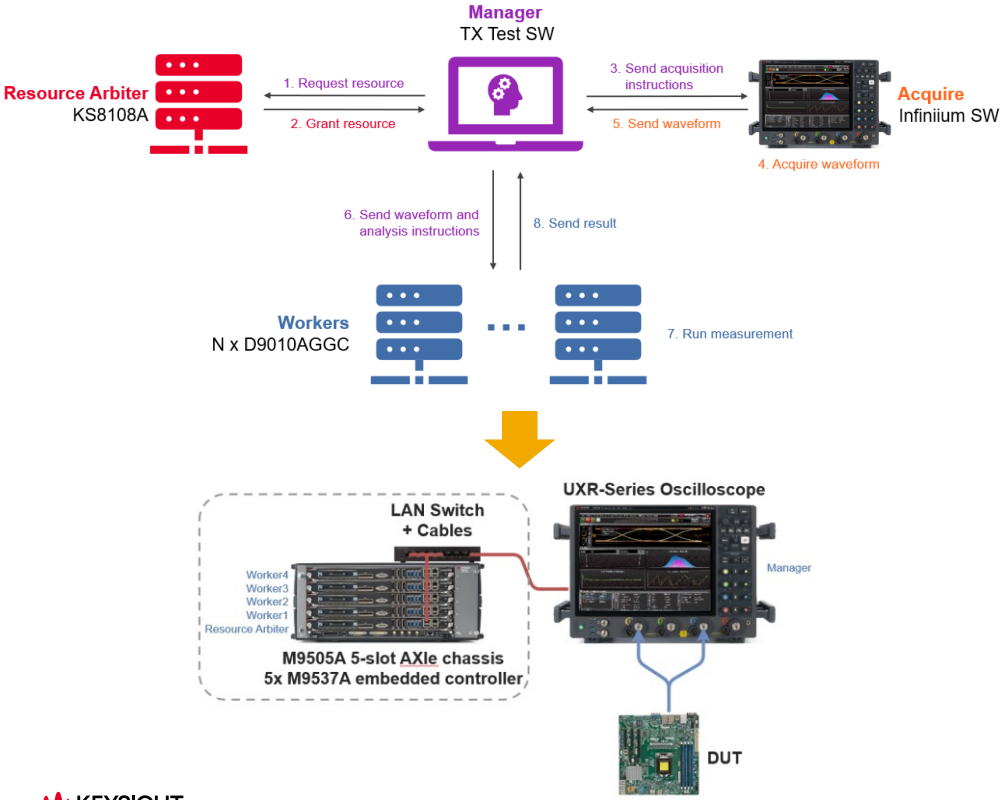
Abhijeet.Shinde@keysight.com

Keysight Technologies

Challenge: DisplayPort Test Time Optimization

Solution: Measurement Disaggregation

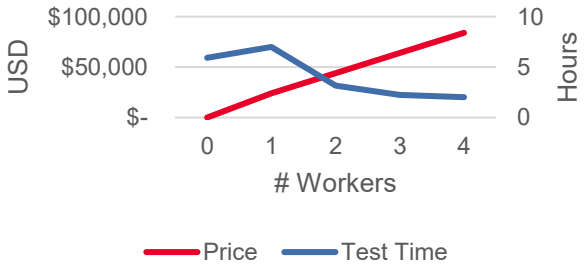


What is it costing you?

- Extensive test plan requires long test time
- 75% of test time is spent processing data

What is an ideal solution?

- Significant test time improvement using Measurement Disaggregation
- Re-use of your invested solution
  - Saves $$$
  - Builds on your present equipment and knowledge



Tektronix VESA Workshop Taipei

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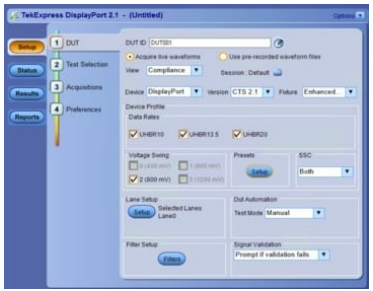
Tektronix DisplayPort Tx Compliance Solution

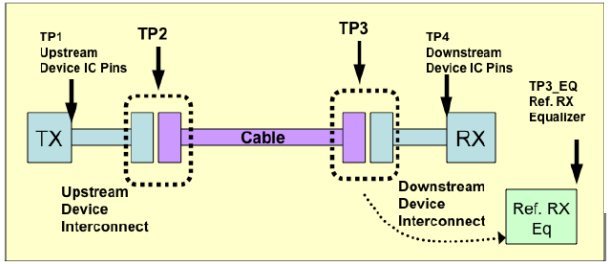
TekExpress DP2.1

- **Fully Automated Software**
- **Supports UHBR rates UHBR10, UHBR135 & UHBR20**

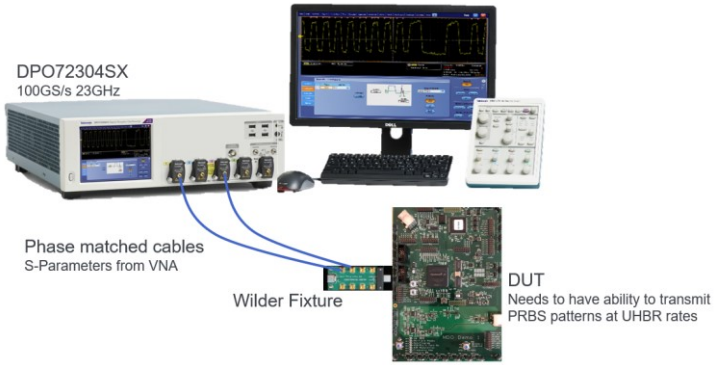


Compliance Test Points

- **Supports both TP2 & TP3EQ (CTLE) test points**
- **USB4 cable model are used in the TP3EQ tests**



DisplayPort Test Setup



Advanced Debugging

DPOJET and SDLA
Jitter, Noise, CTLE

Signal Validation

PRBS15 pattern for the UBHR testing
Pattern Validation

Pre Recorded

Offline Mode
Cross Geo collaboration

DUT control

Automation with UCD323 and DPR100

Signal Acquisition

P76XX Series Probe in absence of fixture

DisplayPort Protocol Analyzer In Action!

FuturePlus Systems

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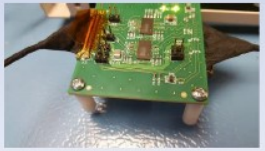
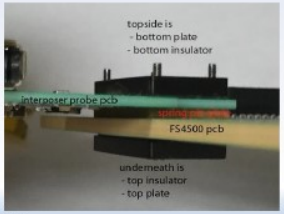
Advancing Technology Development



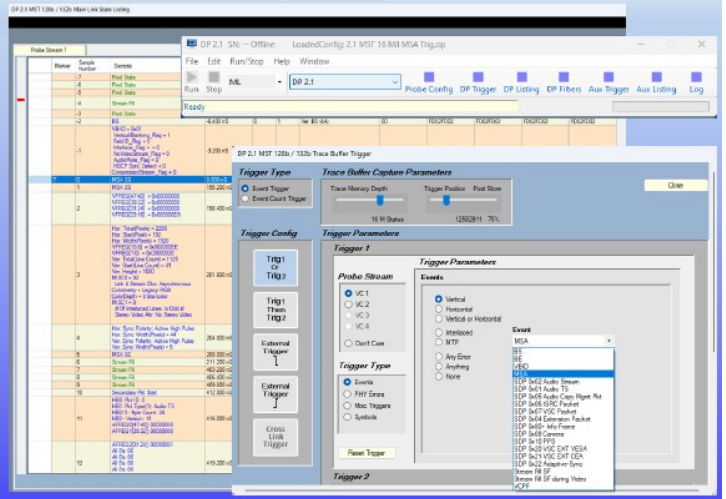
40 pin eDP Repeater

USB Type C Repeater



Regular DP Snooper

- Connects between ANY Source and ANY Sink
  - Supports 8b/10b, eDP, FEC/DSC, DP1.2b DP 1.4b, DP2.1
  - Supports 128b/132b DP2.1
  - Probe, Decode, and Time Correlate High Speed Main Link and Aux Channel
  - Snooper and Repeater Probing Solutions Available

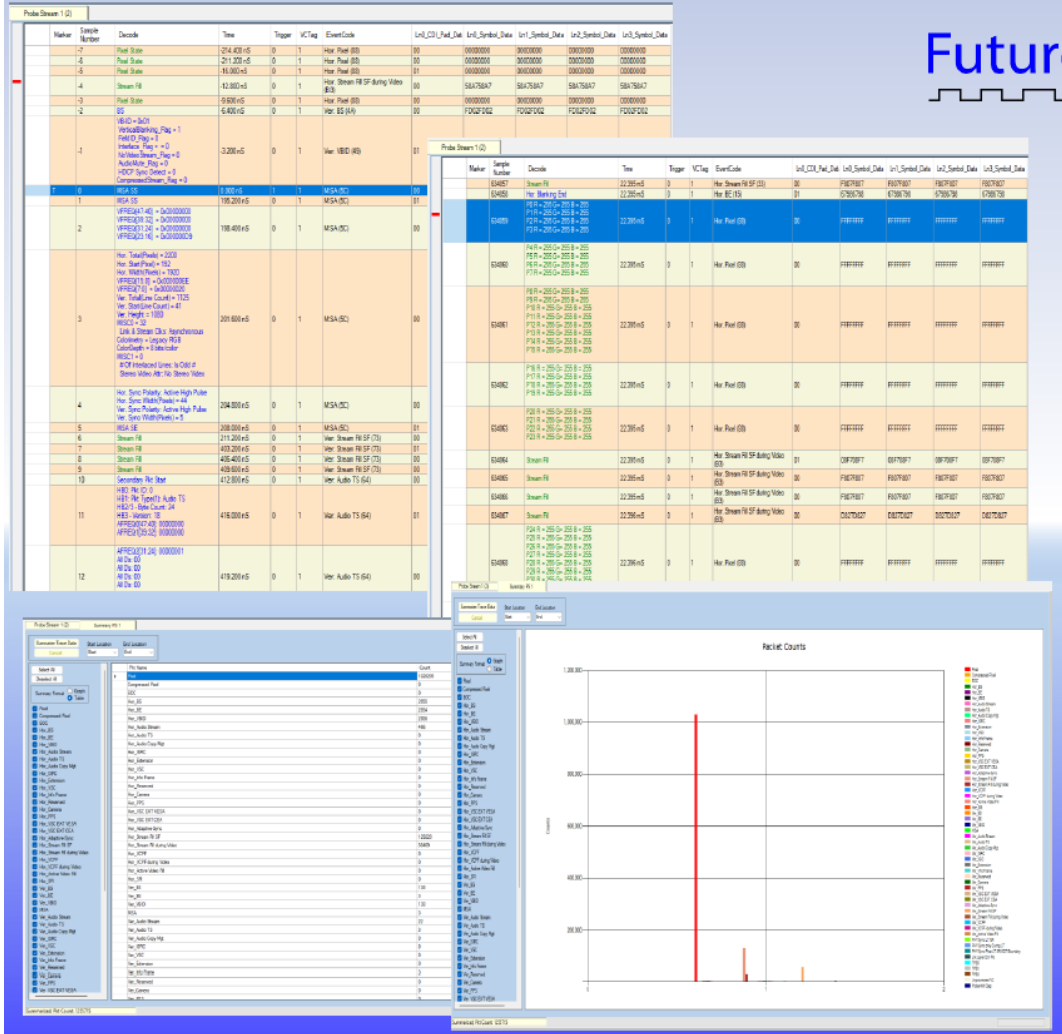


See our Rep in Taiwan

SuperLink Technology Corporation

FuturePlus Systems

Advancing Technology Development

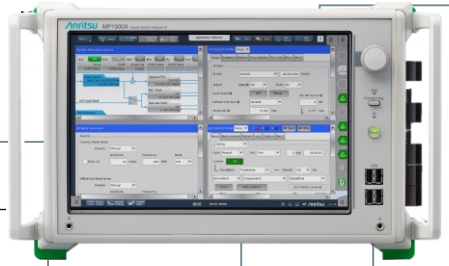


- DP 2.1 Color Bar Test
- 16 Million States
- Captured Complete Frame
- Data Includes video resolutions and frame settings shown in MSA.
- Detailed Decodes of SDP
- Decoded Pixel information
- 128/132 raw data traffic for each lane
- Summary Window containing all packet counts

MP1900A Signal Quality Analyzer
High Speed Bus SINK Compliance Solution

Anritsu
Advancing beyond

MP1900A Standalone
Multi-channel BER Measurement
High-quality PPG
High-input-sensitivity ED
PAM3/4 BER Measurements



Jitter Tolerance Test
SJ/RJ/BUJ Injection
Low-rate estimated BER measurement

Thunderbolt
4/5&DP1.4/2.1 Rx Test
Stressed Signal Calibration and
Stressed Signal Input Test

USB Link Sequence Generation
Transition to Loopback mode

Stressed Signal Calibration
PCI Express Link Sequence Generation
Transition to Loopback Mode
Pass/Fail evaluation using BER measurement

Calibration of stressed signal* → Transition DUT state to Loopback → Stressed Receiver Testing

MX183000A Software

Stressed Signal Calibration*	USB Link Sequence Generation Function PCI Express Link Sequence Generation Function	Stressed Signal Input Test Function Jitter Tolerance Test Auto-receiver Test Function

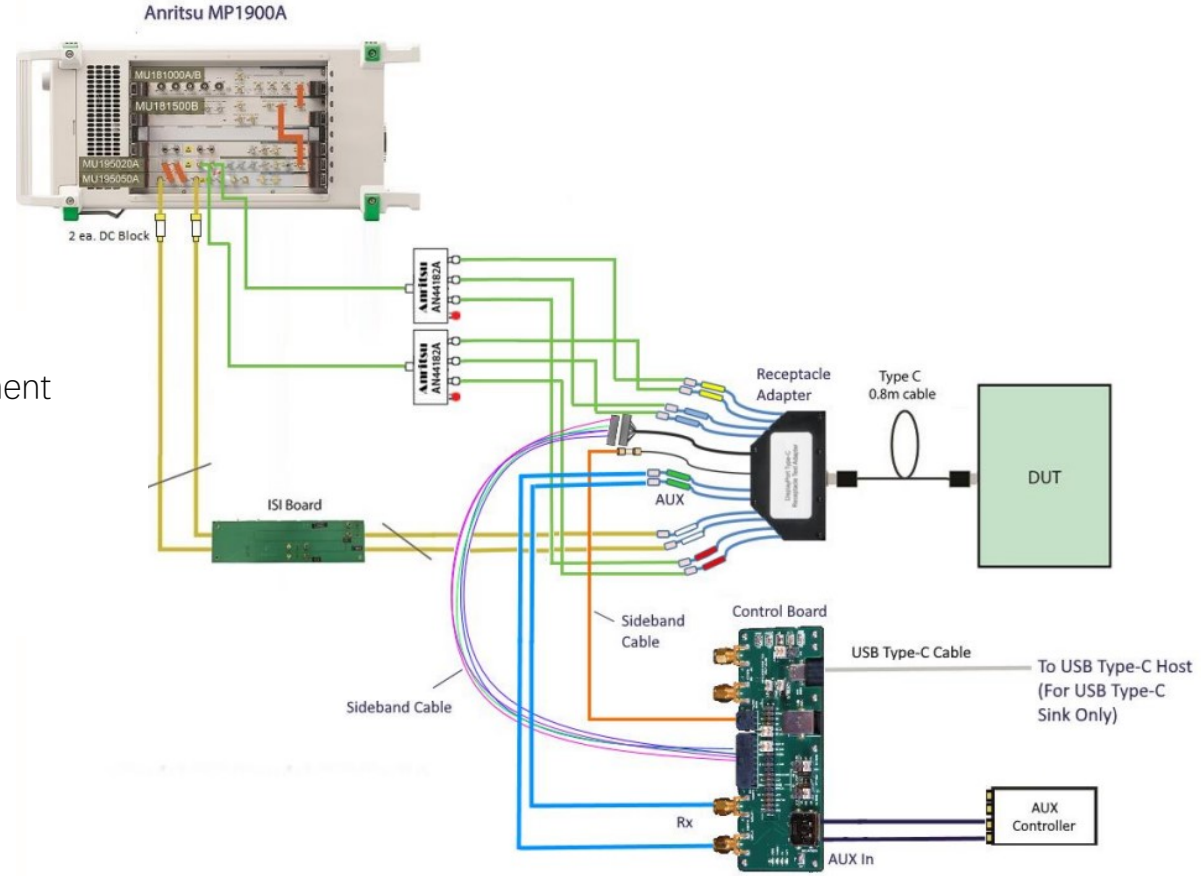
MP1800A Hardware

Up to 32 Gbit/s, 8ch	High Quality Signal	Jitter Emphasis

MP1900A Signal Quality Analyzer
DP1.4/2.1 SINK Compliance Test Structure

MP1900A Standalone

- Multi-channel BER Measurement
- High-quality PPG
- High-input-sensitivity ED
- PAM3/4 BER Measurements
- DP1.4/2.1 and USB4v1&v2 Compliance test Support



Faster, Easier, Better !
The Most Trusted Display Product Testing Consultant

Allion is the VESA Authorized Test Center (ATC) to provide DisplayPort Compliance testing which aims to ensure your products compliant with the VESA standards.

We have deep expertise in display technology and technical support to provide a faster, easier and better integrated consulting services and solutions.

We will show our display product testing solution and Allion's exclusively developed text fixtures at VESA Taipei Workshop 2024.

For more information, please visit

- Display Ecosystem Validation
- Allion Test Fixtures
- Success Stories

Insight Test Labs

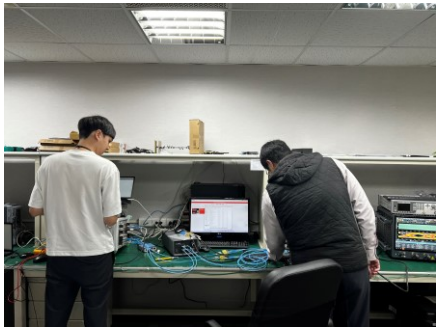
+886 2 2627 2946

4F.-3, No. 36, Alley 38, Lane 358, Ruiguang Rd, **Neihu District, Taipei City**

Services Consult - How Wu (how@labs-insight.com)

Technical Consult - Jerry Sung (jerry@labs-insight.com)

labs-insight.com



Insight Services

Compliance Test for Certification

Official certification/logo testing for **DisplayPort, DisplayHDR**, USB, USB PD, HDCP, HDMI, and IEC 62680 specifications.

Signal Integrity Measurement

Custom testing to meet your clients' needs for PCI Express, DDR, MIPI, SATA, SAS, and more.

Debugging Support

Professional environment and experienced experts assist you in overcoming various challenges.

System **Integration**

Providing support in software development for automation testing and calibration.

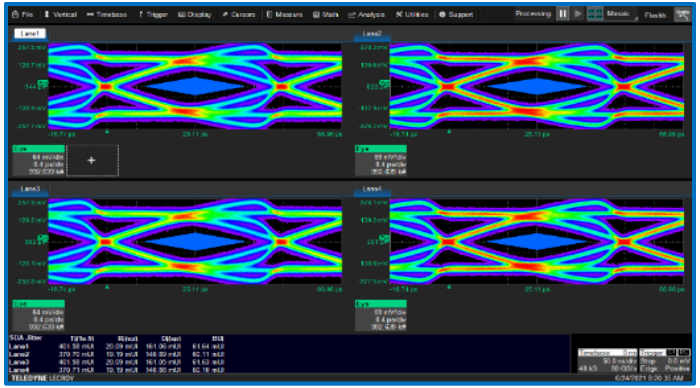
Technical **Consultant**

Experienced team will address the technical issues you encounter and provide the latest updates.

DisplayPort 2.x Source (Tx) Testing

leon.lin@teledyne.com

DisplayPort 2.x Source CTS



QPHY-DP2-Source

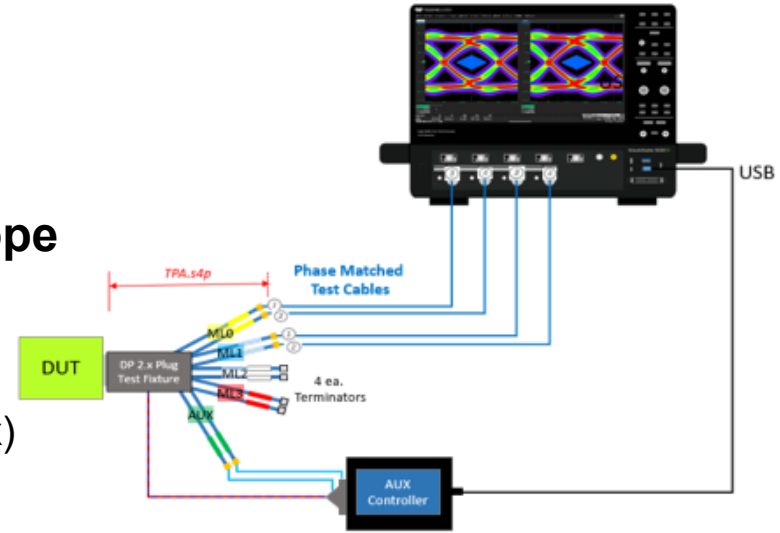
Automation software provides the fastest way to perform compliance testing on DP2.x Source devices. All tests provide a user guided setup including connection diagrams and a comprehensive test report

High Performance Real-Time Oscilloscope

DisplayPort 2.x PHY CTS Requirements

- UHBR20, UHBR13.5: 25 GHz Minimum BW
- UHBR10: 16 GHz Minimum BW

Source (Tx), Sink (Rx) Calibration, Active Cable (Tx)



Thank you for attending the VESA Workshop Taipei, Taiwan 2024