Welcome
VESA Workshop Tokyo, Japan 2024

VESA Workshop Agenda

Time	Topic	Speaker
9:00am	VESA Overview and Standards Updates, Including DisplayPort v2.1a	Alan Kobayashi, VESA Board and DisplayPort Task Group Chair
9:30am	VESA Technologies and Display Panel Standards updates	Jim Choate, Compliance Program Manager
9:45am	DP 2.1 Link Layer CTS testing challenges and requirements	Koji Okazawa, Head of Sales, Unigraf
10:15am	LRD/Active cable testing and DP 2.1 enhanced connector certification	Lexus Lee, Technical Program Manager, Allion Labs
10:45am	VESA Compliance Program	Jim Choate, Compliance Program Manager
	Summary, Questions & Answers	

VESA's Mission and Latest/Upcoming DP Standards Family

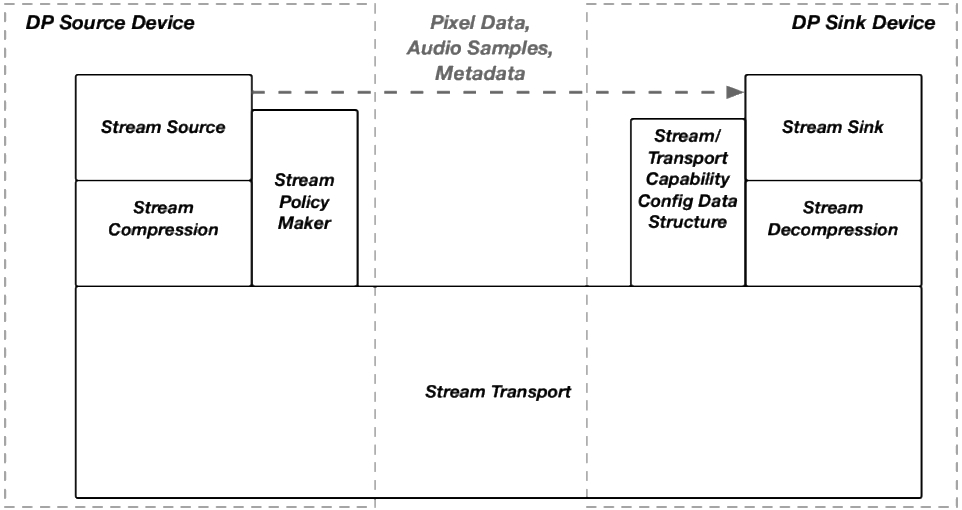
Alan Kobayashi

VESA Board Chair, VESA DisplayPort Task Group Chair

21-OCT-2024

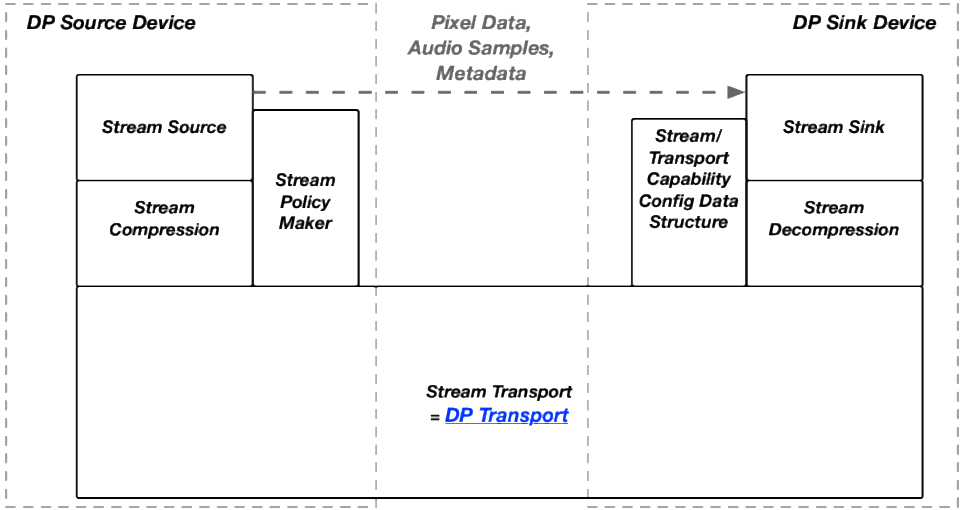
Interoperable End-to-End Visual Ecosystem

- Ensuring interoperability of display stream transport from Stream Source (e.g., GPU) to Stream Sink (e.g., Monitor)



Interoperable End-to-End Visual Ecosystem

- Ensuring interoperability of display stream transport from Stream Source (e.g., GPU) to Stream Sink (e.g., Monitor)
  - Stream Transport
    = DisplayPort (DP) via DP, USB-C, or USB-C-to-DP cable
    - Main Link for Pixel Data, Audio samples, and Metadata transport
    - AUX_CH and HPD for a sideband communication for plug/unplug detection, capability discovery, and configuration



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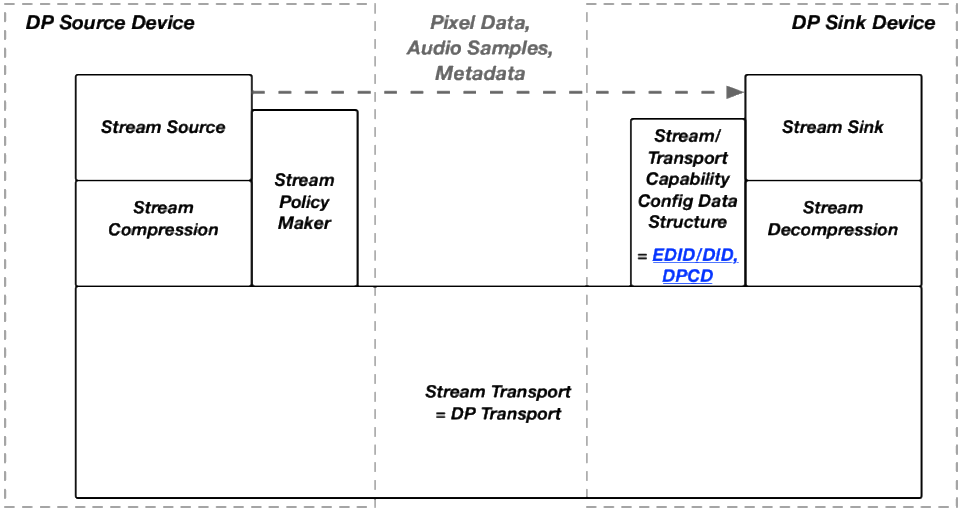
  - Capability/Config Data Structure
    = EDID/DisplayID for Stream and DPCD for Transport



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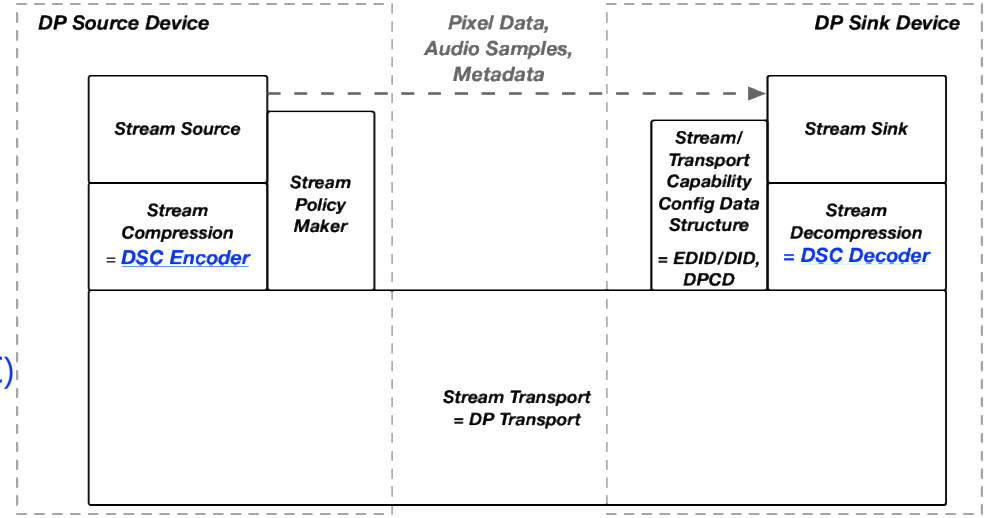
  - Stream Compression
    = Display Stream Compression (DSC)



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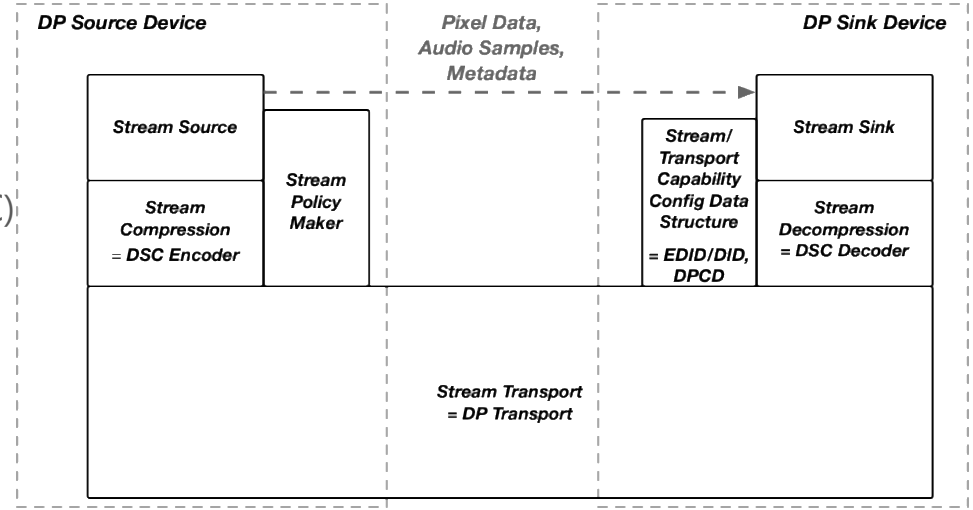
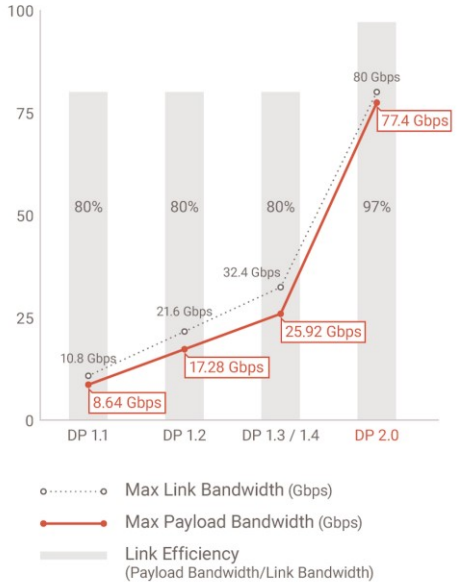
- Visual performance accountability
  - Display Performance Metrix (DPM)



Stream Transport Headroom Provided by DPv2.x

- UHBR20 added in DPv2.x provides for 3x payload (= usable) bandwidth of HBR3
  - Link rate increase + channel coding efficiency improvement (from 8b/10b to 128b/132b)
- "DSC mandate" added in DPv2.x significantly increases the transportable stream bandwidth
  - 4-lane HBR3 with DSC sufficient for 4K2K240
  - 4-lane UHBR20 with DSC sufficient for 12K2K240
    - A single 12K2K240 panel or 3x 4K2K240 panels cascaded



DP Standard Version Number…

- It is a “never dying” habit to associate DP Standard version number to the maximum link rate supported…
  - DPv1.1 = HBR (2.7 Gbps/lane)
  - DPv1.2 = HBR2 (5.4 Gbps/lane)
  - DPv1.4 = HBR3 (8.1 Gbps/lane)
  - DPv2.x = UHBR rates (10/13.5/20 Gbps/lane)

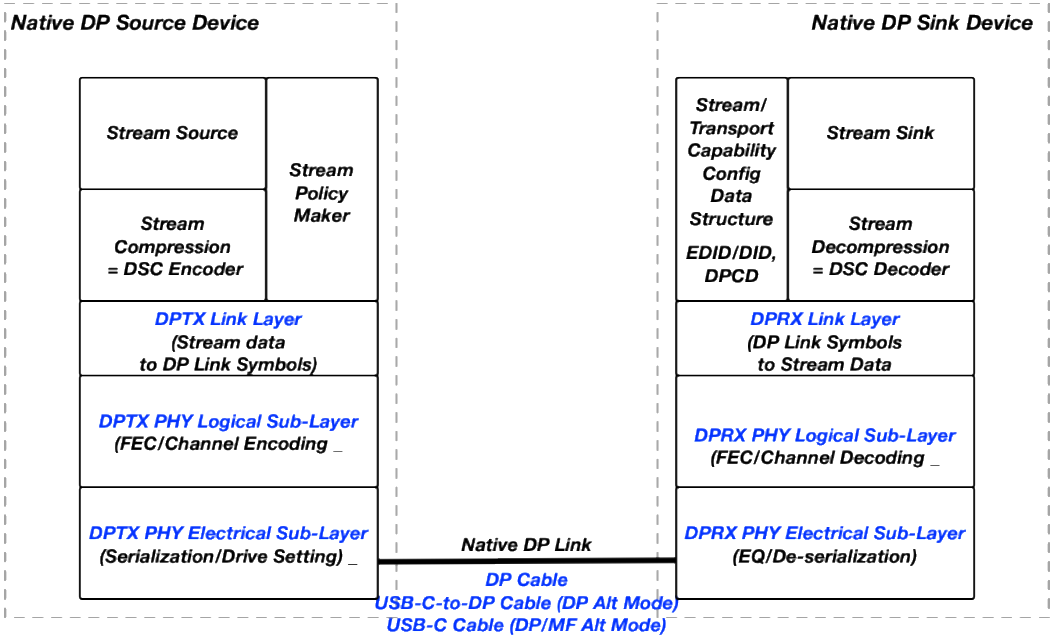
DP Standard Version Number…

- However, only the latest version is active per VESA policy
  - The latest, and, thus, active, version is DPv2.1a released December 2024
  - A new standard version comes with:
    - New features not related to link rate (e.g., Panel Replay, Adaptive-Sync SDP payload extension in v2.x)
    - Interop improvement policy updates
- "My device supports up to 4-lane HBR2 with DSC and Panel Replay support"
  - HBR2 introduced in DPv1.2
  - DSC introduced in DPv1.4
  - Panel Replay introduced in DPv2.0

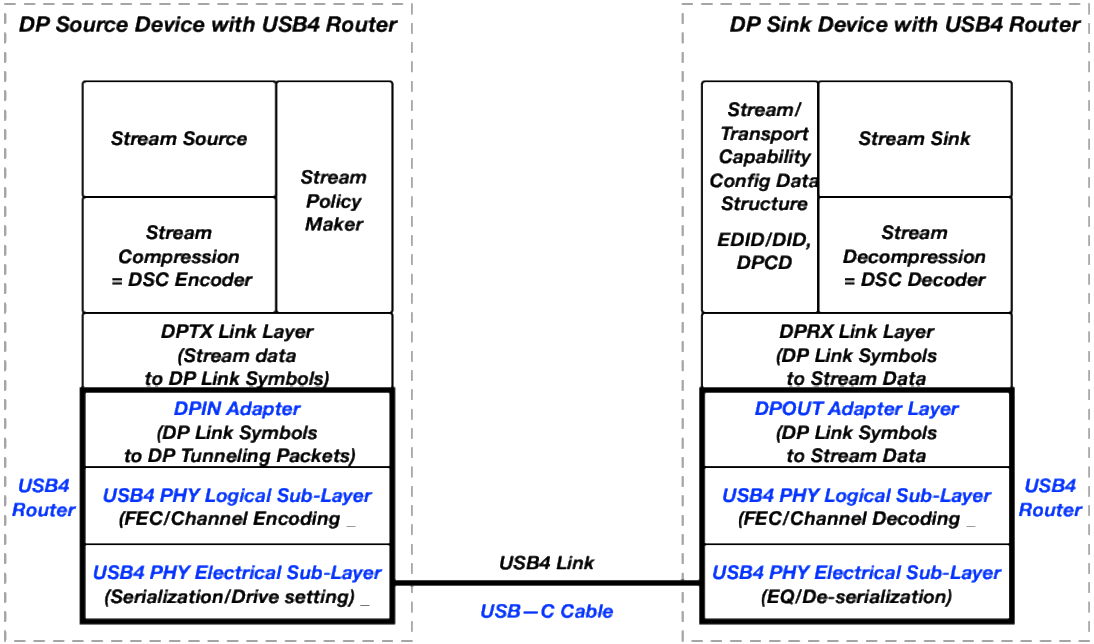
Two Types of DP Transport

- Native DP Transport
  - Not to be confused with “DP Cable vs. USB-C Cable (= DP Alt Mode)”
  - Uses DP PHY Layer to transport DP Link Symbols carrying stream data
  - Cable types
    - A DP cable
    - A USB-C cable or a USB-C-to-DP cable: DP/Multi-Function (MF) Alt Mode
- Tunneled DP Transport
  - Encapsulates DP Link Symbols into USB4 DP Tunneling Packets
  - Cable type
    - A USB-C cable

Native DP Transport

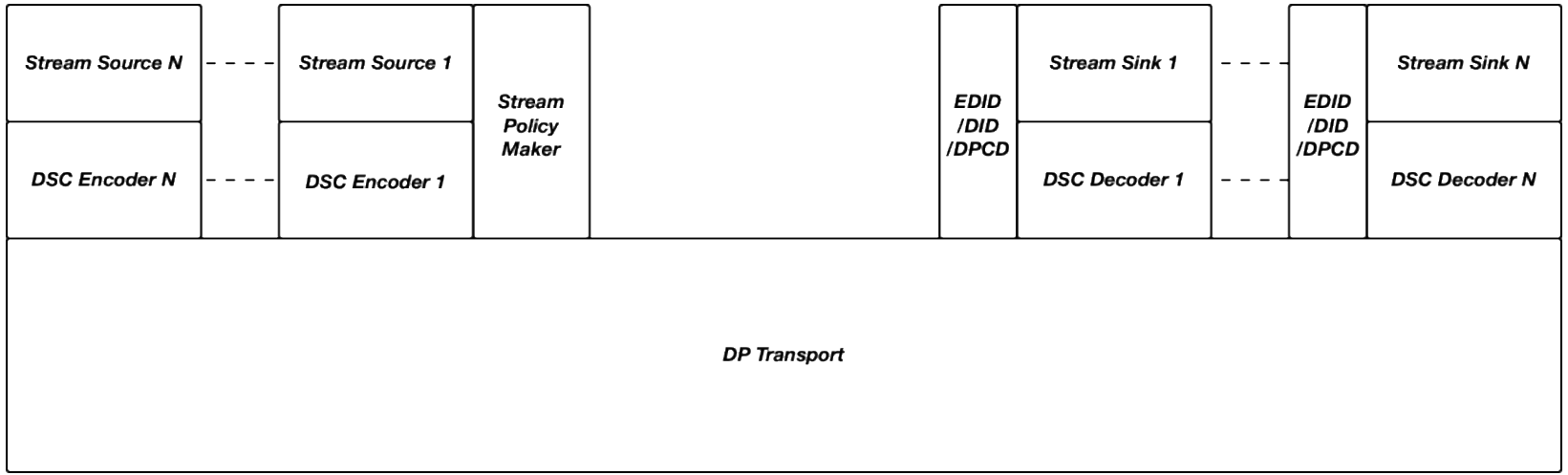


Tunneled DP Transport



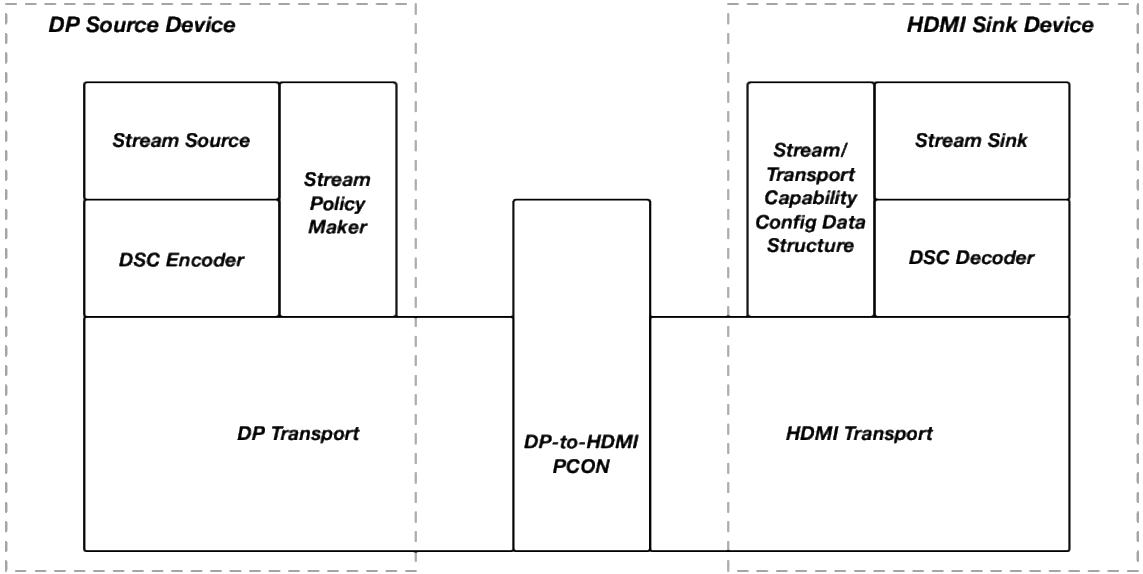
Supporting Transport of Multiple Streams

- Native DP Transport: DP MST (Multi-Stream Transport)
- Tunneled DP Transport: Tunneling of DP MST link or multiple DP SST (Single Stream Transport) links



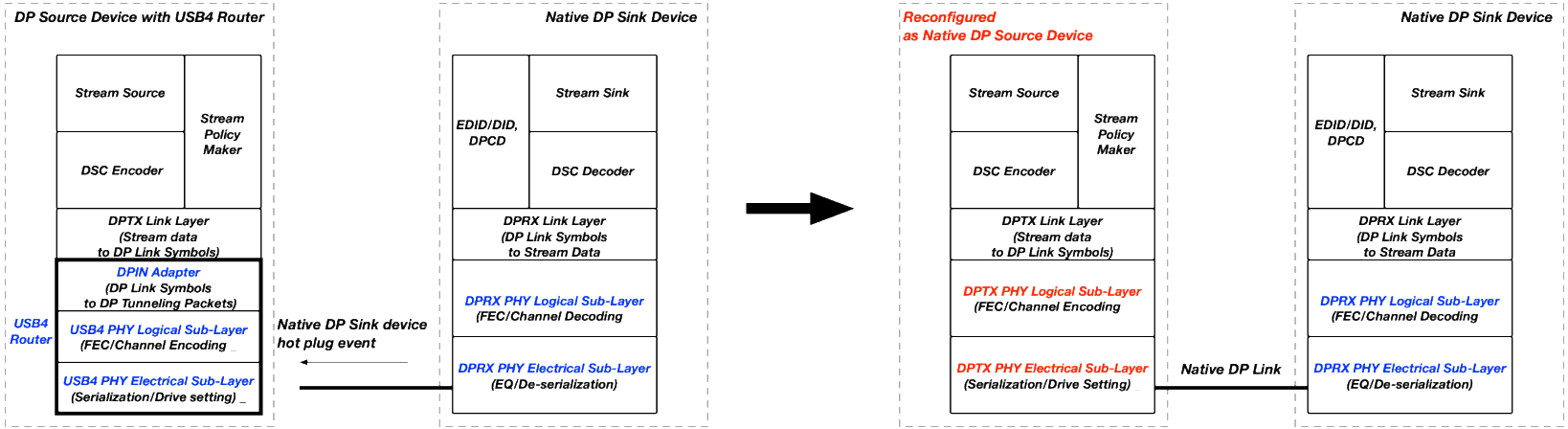
Supporting Non-DP Stream Transport

- Via PCON (Protocol Converter): E.g., DP-to-HDMI PCON
  - DP Standard defines PCON specification



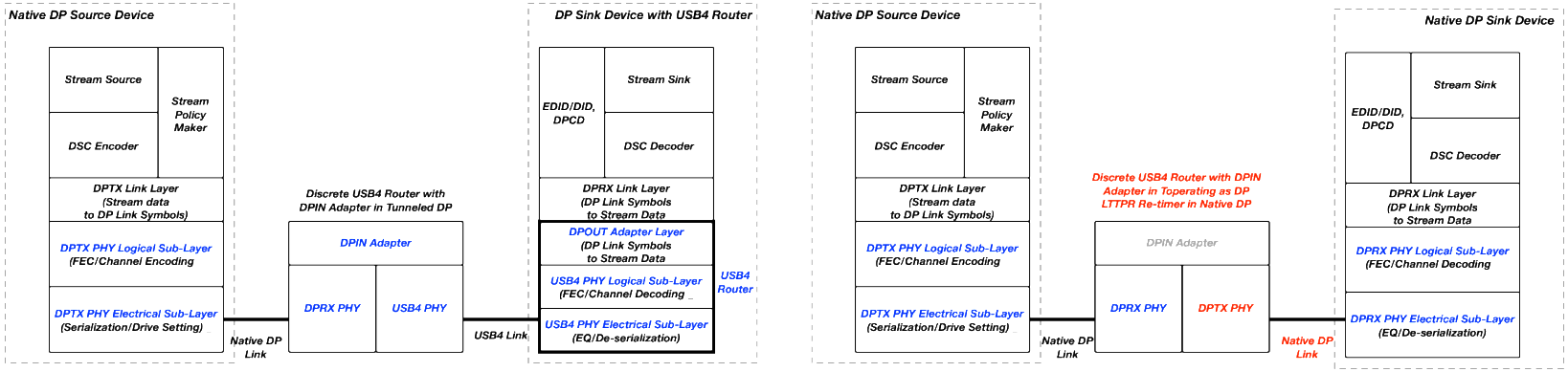
Native/Tunneled DP Dual Support Requirement

- A DP Source device with USB4 router is required to reconfigure itself as a Native DP Source device when connected to a Native DP Sink device
  - The same requirement exists for a DP Sink device with USB4 router



Native/Tunneled DP Dual Support Requirement

- A discrete USB4 router chip becomes an LTTPR re-timer in Native DP Transport



Native/Tunneled DP Dual Support Facilitation

- Goal
  - Facilitate an implementation that supports both Native DP Transport and Tunneled. DP Transport
- UHBR link rates added in DPv2.x Standard leverage USB4 PHY spec to the maximum extent feasible
  - 128b/132b channel coding
  - Link rates: UHBR10/UHBR20 = USB4Gen2/Gen3
    - UHBR13.5 unique to DP
  - TX FFE presets
  - Reference RX EQ
  - End-to-end channel loss budget assumptions

Helping USB4 Be More Efficient

- DP tunneling is typically the largest USB4 link bandwidth consumer, but USB4 carries non-DP tunneling traffic
  - E.g., PCIe tunneling, USB3 tunneling
- DSC mandate reduces the DP tunneling bandwidth consumption
  - E.g.: 67% reduction for 36 bpp uncompressed HDR to 12 bpp DSC compression
- Panel Replay also reduces DP tunneling bandwidth consumption when a static image is displayed on a monitor screen
  - 99%+ reduction when Panel Replay operation is activated
- DP BW Allocation Management avoids wasted BW allocation to DP tunneling
  - BW allocation based on the stream bandwidth (= pixel rate * pixel bit depth) instead of the maximum DP link payload bandwidth

DP Cable Logos

- Either a DP cable or a USB-C-to-DP cable (DP Alt Mode)
- DP8K
  - Up to 4-lane HBR3 without a DP cable identification mechanism
- DP54
  - Up to 4-lane UHBR13.5 with a DP cable identification mechanism
- DP80/DP80LL
  - Up to 4-lane UHBR20 with a DP cable identification mechanism

DP54 Cable

- Originally DP40 cable in DPv2.1 supporting up to 4-lane UHBR10
- Updated to DP54 supporting up to 4-lane UHBR13.5 in DPv2.1a
- Feasible of ~ 2-meter passive cable

DP80LL (Low Loss) Cable

- To be added in DPv2.1b targeted Q1 2025 release
- Lower loss than DP80 cable
  - DP80LL: -6.5 dB of loss at 10 GHz
  - DP80: -8.5 dB of loss at 10 GHz
- Feasible of ~ 3-meter LRD active cable
  - Leverages USB4 LRD active cable spec and compliance test methodology
- DP80 cable not deprecated, but LRD active cable required to meet DP80LL budget
  - DP80 passive cable length is limited to ~ 1 meter

Next DP Link Rate Increase?

- USB4v2 added USB4 Gen4 link rate of 40 Gbps/lane
  - Doubled USB4 Gen3 link rate of 20 Gbps/lane
- Currently, no DP link rate increase beyond UHBR20 considered
  - No clear use case merit beyond 80 Gbps of 4-lane UHBR20 identified

eDP Standard

- eDP2.0 released in September 2024
- More convergence with DP Standard
  - Making a reference to DP Standard
    - 128b/132b DP (new in eDP2.0)
    - Panel Replay
    - AUX-less ALPM (Advanced Link Power Management)

DP Alt Mode Standard

- DP Alt Mode v2.1a released in August 2024
- Main update = Cable identification flow clarification for interop improvement

DP Automotive Extension Services

- DP Automotive Extension Services v1.0 released in December 2023
- Safety and security extension for DP use case for automotive

Making a Difference to VESA Standards

- Become a VESA member
- Review documents of interest in VESA Causeway site
  - Each VESA member can add himself/herself to any VESA Task Group (TG) /Subgroup (SG) roster via Self-Add
- Join in VESA TG/SG WebEx conf calls and/or review meeting minutes documents
  - VESA's meeting minutes documents are very detailed
- Even if not being able to join in VESA conf calls, submit comments/questions using VESA Causeway "Discussions" and "Commenting" features

VESA Display Standards Updates

Jim Choate
VESA Compliance Program Manager
October 21, 2024

Agenda

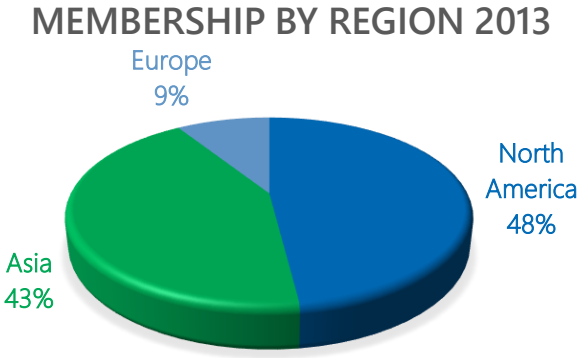
- VESA Overview
- VESA Certified DisplayHDR, ClearMR and Adaptive-Sync

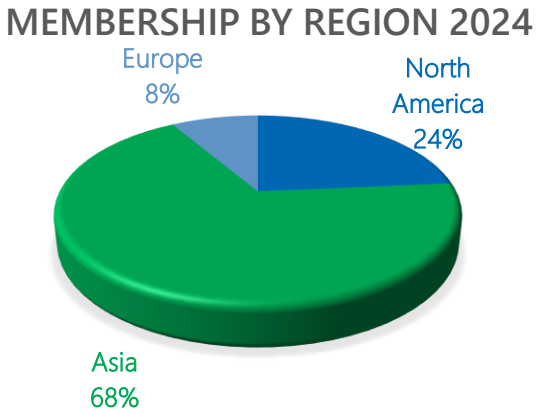
VESA OVERVIEW

About VESA

- A growing global industry alliance with nearly 340 members in 2024. Strong growth in membership over 10 years.
- Mission to develop, promote and support ecosystem of vendors and certified interoperable products for the electronics industry.
- *Develops OPEN standards, contribution is open to all companies at all stages of development*

VESA Membership Growth





Changes from 2013:
Asia + 25%

VESA Standards Enable Many Market Segments…

Monitors, PCs and laptops

Gaming consoles and headsets

Digital signage / kiosks

Smartphones and tablets

Automotive

Digital projectors

...As Well as Many Aspects of Display Technology

Display Interfaces

- DisplayPort
- Embedded DisplayPort
- DisplayPort Alt Mode (Native DisplayPort over USB-C connector)
- DisplayPort Tunneling (USB4 and Thunderbolt)
- Automotive Extensions Services (DP AE specification)

Display Data Compression

- Display Stream Compression (DSC)
- VESA Display Codec for Mobile (VDC-M)

Display Metrology

- Standardized Display Performance Measurement
- DisplayHDR Certification (High Dynamic Range)
- ClearMR Certification
- AdaptiveSync Display Certification

Display Capability Parameters

- DisplayID
- Extended Display Identification Data (EDID)
- Multi-Display Interface (MST)

35

VESA Local Asian Support Capability

- VESA continues to provide local support to Asia to address growing regional membership needs
- China (Mainland) and Taiwan are the fastest growing areas for VESA's membership.
- **Kellen** is VESA's Representative in Asia
- This partnership provide members with a communication option in their native language. Kellen handles membership related activities including, new membership requests, renewals, event support and translation of VESA member messaging, etc.
- AsiaVESA@kellencompany.com or at +86 10 6580 0670

VESA Certified DisplayHDR, ClearMR and AdaptiveSync

VESA Display Performance Standards

VESA's display performance work group has been busy since the initial release of the DisplayHDR CTS in 2017.

- VESA Certified DisplayHDR r1.2
- VESA Certified Clear Motion Ratio (CMR) r1.1
- VESA Certified AdaptiveSync r1.1

VESA Display Performance Metrics

1

VESA CERTIFIED DisplayHDR™

It ensures **better brightness**, **contrast**, and color **accuracy**, making content look more vibrant and realistic.

2

VESA CERTIFIED AdaptiveSync DISPLAY 144

It ensures that monitors can dynamically adjust their refresh rates to match the frame rates produced by the GPU.
To prevent screen tearing and stuttering.

3

VESA CERTIFIED ClearMR

Easily compare motion quality of certified displays with a clear numerical value based on the ratio of clear pixels to blurry pixels.

DisplayHDR Summary

- Industry's first open HDR specification for LCD and emissive (OLED/microLED) displays with a fully transparent testing methodology
- More than 3000 display models certified under logo program to date makes VESA Certified DisplayHDR one of the most successful logo programs in VESA history.
- More details available at https://displayhdr.org

VESA Defines New Standard to Help Speed PC Industry Adoption of High Dynamic Range Technology in Laptop and Desktop Monitor Displays

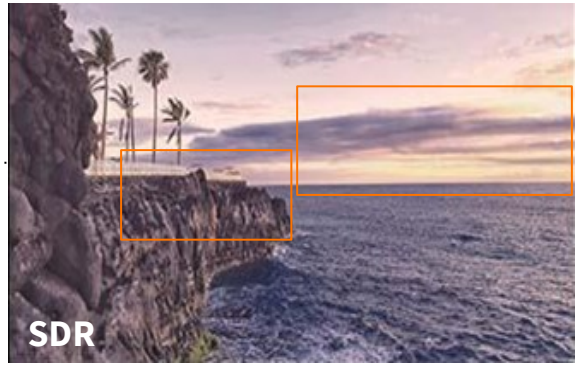
DisplayHDR is industry's first open HDR specification with a fully transparent testing methodology

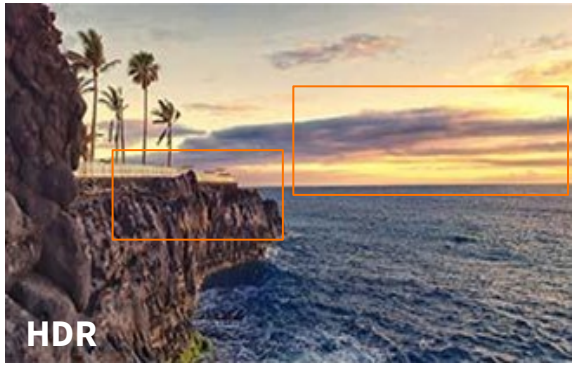
SAN JOSE, Calif. – December 11, 2017 – The Video Electronics Standards Association (VESA®) today announced it has defined the display industry's first fully open standard specifying high dynamic range (HDR) quality, including luminance, color gamut, bit depth and rise time, through the release of a test specification. The new VESA High-Performance Monitor and Display Compliance Test Specification (DisplayHDR) initially addresses the needs of laptop displays ar

High Dynamic Range (HDR)

Gaming

Photography,
Television,
Film…and so on

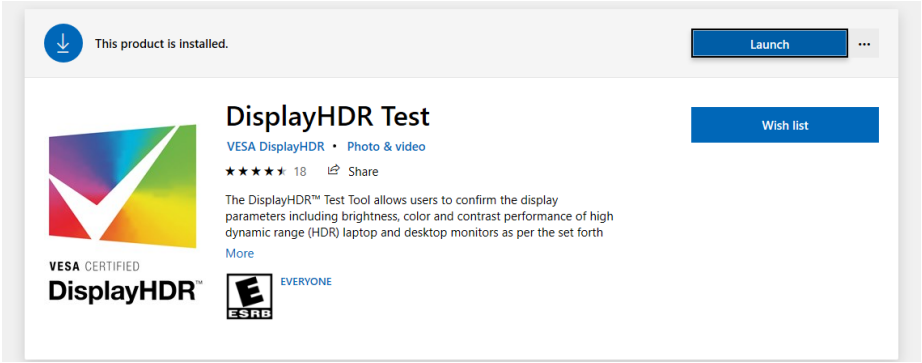




- ✓ **Greater Brightness**
- ✓ **Better Contrast**
- ✓ **Vibrant colors**
- ✓ **More Lifelike**

DisplayHDR Certified Products

- Certified DisplayHDR performance tiers
  - DisplayHDR 400
  - DisplayHDR 500
  - DisplayHDR 600
  - DisplayHDR 1000
  - DisplayHDR 1400
  - DisplayHDR True Black 400
  - DisplayHDR True Black 500
  - DisplayHDR True Black 600



- DisplayHDR CTS and test tool are available to all companies
- Test tool app available on Microsoft store for public download

ClearMR Summary

- VESA developed motion blur performance compliance test specification for LCD and emissive (OLED/microLED) displays with a new Clear Motion Ratio (CMR) metric and fully transparent testing methodology
- More than 116 display models certified under ClearMR logo program to date
- More details available at https://www.clearmr.org/

VESA BRINGS CLARITY TO MOTION BLUR IN DIGITAL DISPLAYS WITH NEW COMPLIANCE TEST SPECIFICATION AND LOGO PROGRAM

ClearMR specification and logo program provide consumers with a true quality metric for grading motion blur performance for LCD and OLED panels, TVs, desktop monitors and embedded displays

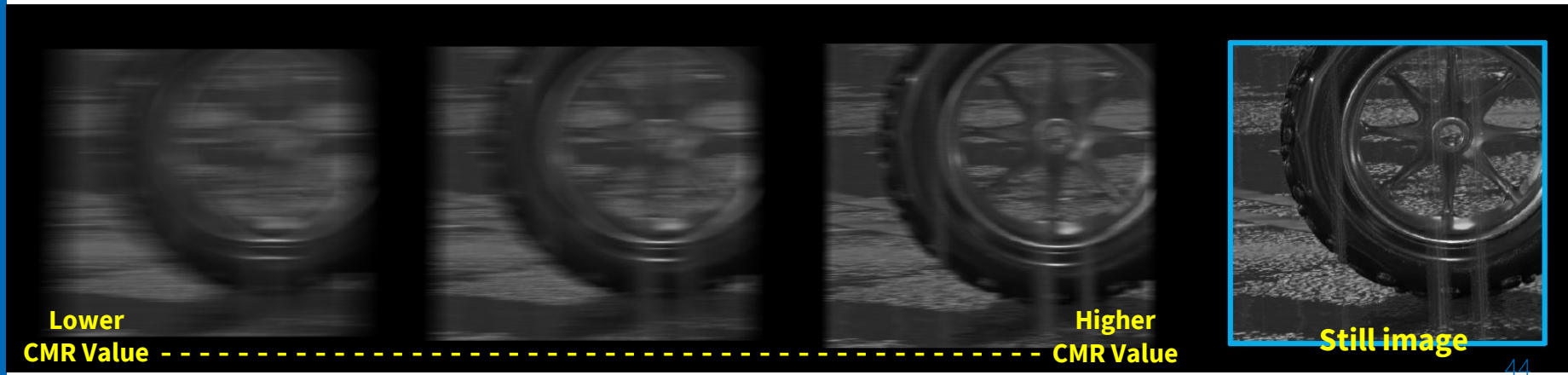
BEAVERTON, Ore. – August 22, 2022 – The Video Electronics Standards Association (VESA®) today introduced the ClearMR Compliance Test Specification (ClearMR), an industry standard and logo program that provides a new quality metric for grading motion blur in digital displays. ClearMR is applicable to both LCD and emissive display products, including display panels, TVs, monitors, and computers with embedded displays, such as all-in-ones, laptops, notebooks and tablets. The new metric Clear Motion Ratio (CMR), as

What is VESA ClearMR?

VESA CERTIFIED ClearMR

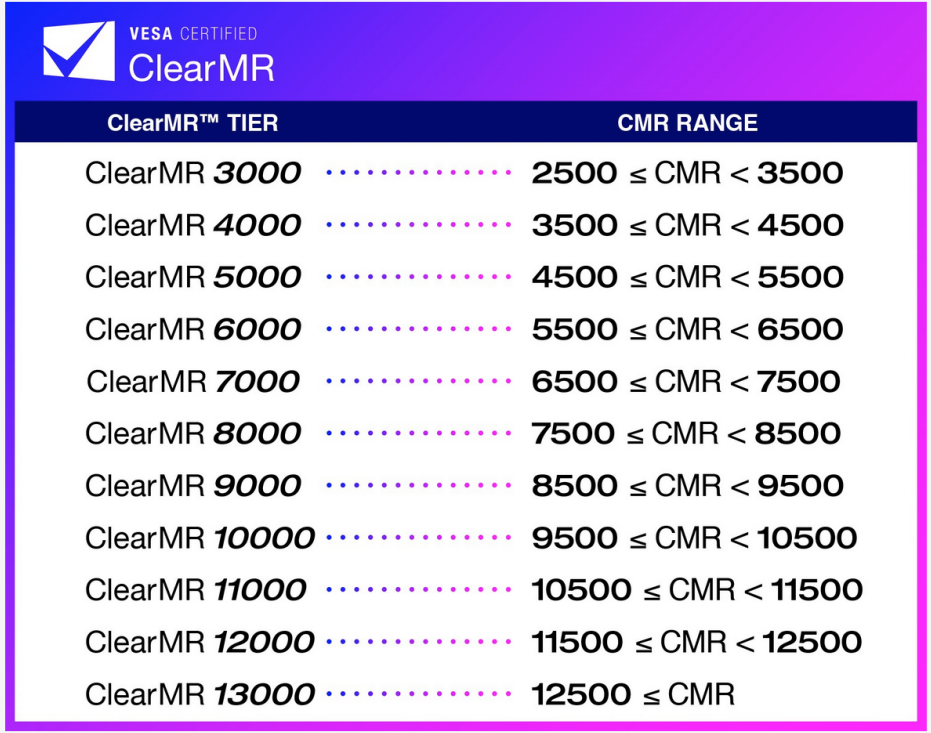
A metric for assessing motion blur in digital display products.

- ✓ **Provides a consistent baseline for motion image quality**
- ✓ **Ensure smoother motion and reduce ghosting**



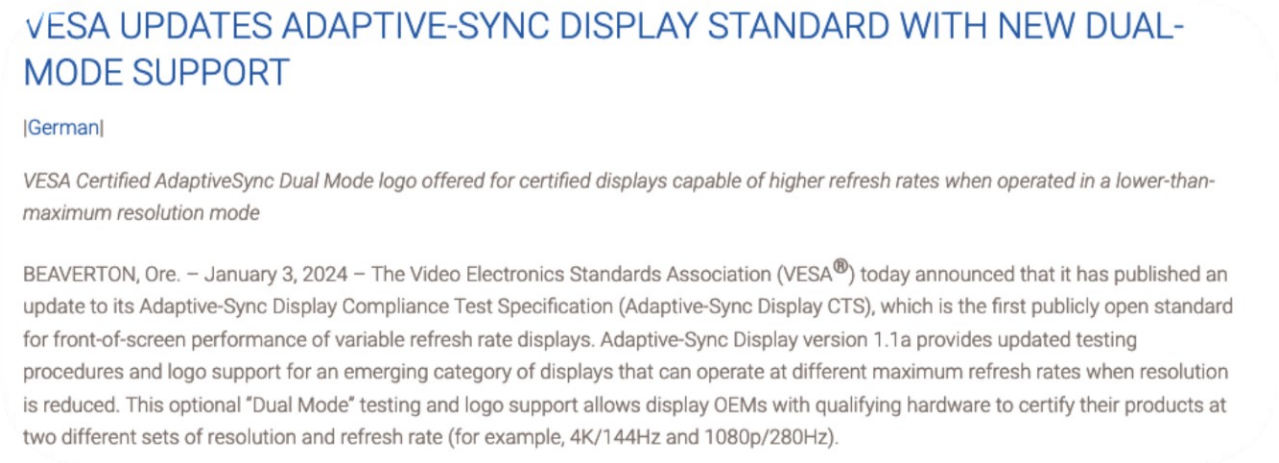
ClearMR Certified Products

- Certified ClearMR performance tiers
  - ClearMR 3000 to ClearMR 13000 Certification Tiers
- ClearMR performance criteria and certified product listing CTS and test tool are available here:
- https://www.clearmr.org/certified-products/



VESA Adaptive-Sync Display Summary

- Industry's first publicly open standard for front-of-screen performance of variable refresh rate displays.
- More details available at https://www.adaptivesync.org/



VESA UPDATES ADAPTIVE-SYNC DISPLAY STANDARD WITH NEW DUAL-MODE SUPPORT

|German|

VESA Certified AdaptiveSync Dual Mode logo offered for certified displays capable of higher refresh rates when operated in a lower-than-maximum resolution mode

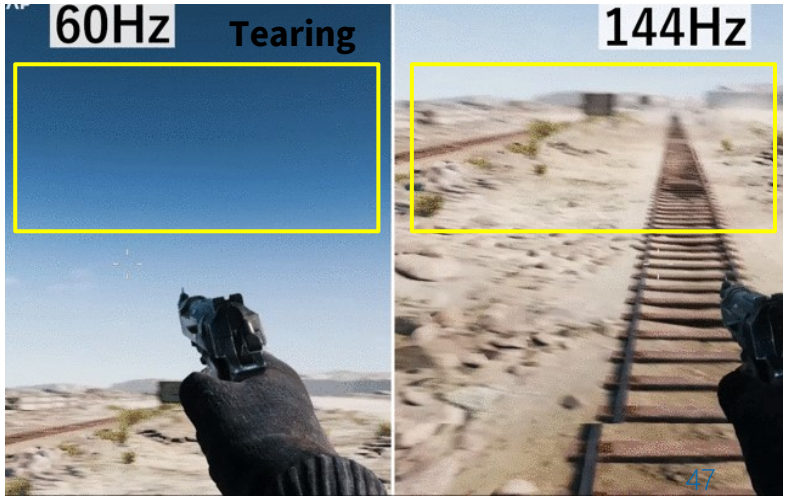
BEAVERTON, Ore. – January 3, 2024 – The Video Electronics Standards Association (VESA®) today announced that it has published an update to its Adaptive-Sync Display Compliance Test Specification (Adaptive-Sync Display CTS), which is the first publicly open standard for front-of-screen performance of variable refresh rate displays. Adaptive-Sync Display version 1.1a provides updated testing procedures and logo support for an emerging category of displays that can operate at different maximum refresh rates when resolution is reduced. This optional "Dual Mode" testing and logo support allows display OEMs with qualifying hardware to certify their products at two different sets of resolution and refresh rate (for example, 4K/144Hz and 1080p/280Hz).

What is VESA AdaptiveSync?

VESA CERTIFIED AdaptiveSync DISPLAY 144

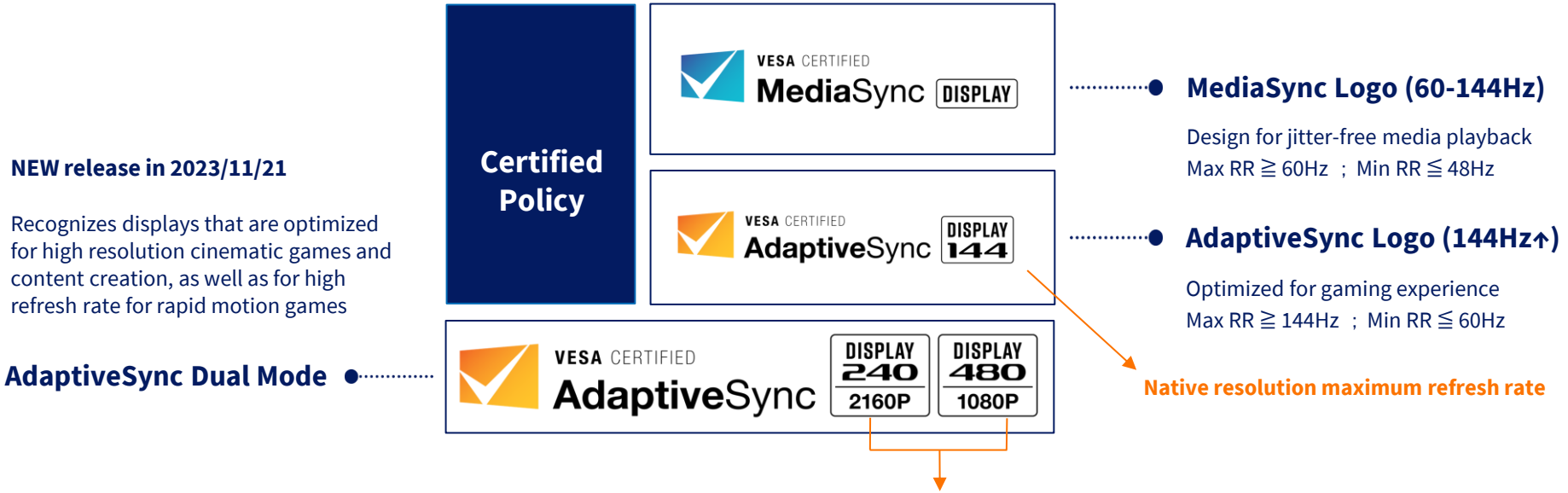
Work by dynamically adjusting the display's refresh rate to match the GPU's frame rate output.

- ✓ **Smooth and responsive gaming experience**
- ✓ **Reduce input lag**
- ✓ **Eliminate screen tearing and stuttering**



VESA Certified — AdaptiveSync

- VESA AdaptiveSync Display Certification is the first open source industry standard for display visual performance on variable refresh rate displays.



DP 2.1 Link Layer CTS Update

Koji Okazawa
Unigraf
21.10.2024

DP 2.1 Link Layer Compliance Testing Update

Agenda

- Native DisplayID
- Audio
- USB4 DP Tunneling
- Updates after rev.1.0
- Planned updates

Native DisplayID Tests (Adopted in March 2024)

- Source DUT
  - Section 4.7.6 Native DisplayID Video Tests
  - Section 4.7.7 Native DisplayID Audio Tests
- Sink DUT
  - Section 5.7.19 Native DisplayID Framework Validation Tests
  - Section 5.7.20 Product Identification Data Block Tests
  - Section 5.7.21 Display Parameters Data Block
  - Section 5.7.22 Display Interface Data Block

Audio CTS (TGR)

- Main Targets:
  - Validate Audio at UHBR link rates
  - Validate Audio with DSC enabled
- Challenges:
  1. Streaming high sample rate audio at RB timings
  2. Audio test time
  3. Audio samples distribution during blanking period
- Draft 4 is under TGR (Task Group Review)

Audio CTS (Challenge #1 – 192Khz 8ch)

						SSC	TRUE	0,994					
				(Hz)	(MHz)	FEC	TRUE	0,97			SST		
Hactive	Vactive	Htotal	Hblank	V Freq	Pixel Freq	lane	link_rate	symbol size	2ch, SST AudioSymbolCntReqPerHBlank	8ch, SST AudioSymbolCntReqPerHBlank	StrmSymbolCntAvailPerHBlank	2ch, isValid	8ch, isValid
1920	1080	2000	80	30	65,76	1	162	8	65	254	165	TRUE	FALSE
1920	1080	2000	80	60	133,32	1	162	8	44	127	66	TRUE	FALSE
1920	1080	2000	80	144	333,216	4	162	8	24	88	92	TRUE	TRUE
1920	1080	2000	80	144	333,216	2	270	8	22	86	92	TRUE	TRUE
1920	1080	2000	80	144	333,216	1	540	8	22	85	98	TRUE	TRUE
3840	2160	3920	80	30	257,661	4	162	8	48	128	136	TRUE	TRUE
3840	2160	3920	80	30	257,661	2	270	8	44	128	130	TRUE	TRUE
3840	2160	3920	80	30	257,661	1	540	8	44	127	136	TRUE	TRUE
3840	2160	3920	80	60	522,614	4	162	8	24	88	36	TRUE	FALSE
3840	2160	3920	80	60	522,614	2	540	8	22	86	128	TRUE	TRUE
3840	2160	3920	80	60	522,614	1	810	8	22	85	93	TRUE	TRUE
3840	2160	3920	80	144	1306,206	4	540	8	24	44	68	TRUE	TRUE
3840	2160	3920	80	144	1306,206	2	810	8	22	44	62	TRUE	TRUE
5120	2160	5200	80	30	341,796	4	162	8	48	128	88	TRUE	FALSE
5120	2160	5200	80	30	341,796	2	270	8	44	128	88	TRUE	FALSE
5120	2160	5200	80	30	341,796	1	540	8	44	127	95	TRUE	FALSE
5120	2160	5200	80	60	693,264	4	270	8	24	88	60	TRUE	FALSE
5120	2160	5200	80	60	693,264	2	540	8	22	86	86	TRUE	FALSE
5120	2160	5200	80	60	693,264	1	810	8	22	85	62	TRUE	FALSE
5120	2160	5200	80	120	1427,088	4	540	8	24	44	60	TRUE	TRUE
5120	2160	5200	80	144	1732,723	4	540	8	24	44	36	TRUE	FALSE
7680	4320	7760	80	30	1019,896	4	540	8	24	88	108	TRUE	TRUE
7680	4320	7760	80	30	1019,896	2	810	8	22	86	90	TRUE	TRUE
7680	4320	7760	80	60	2068,66	4	810	8	24	44	64	TRUE	TRUE
10240	4320	10320	80	30	1356,357	4	540	8	24	88	64	TRUE	FALSE
10240	4320	10320	80	30	1356,357	2	810	8	22	86	58	TRUE	FALSE
10240	4320	10320	80	60	2751,105	4	810	8	24	44	32	TRUE	FALSE

						SSC	TRUE	0,994					
				(Hz)	(MHz)	FEC	TRUE	0,97			MST		
Hactive	Vactive	Htotal	Hblank	V Freq	Pixel Freq	lane	link_rate	symbol size	2ch, MST AudioSymbolCntReqPerHBlank	8ch, MST AudioSymbolCntReqPerHBlank	StrmSymbolCntAvailPerHBlank	2ch, isValid	8ch, isValid
3840	2160	3920	80	60	522,614	4	162	8	24	88	60	TRUE	FALSE
3840	2160	3920	80	60	522,614	2	540	8	24	88	62	TRUE	FALSE
3840	2160	3920	80	60	522,614	1	810	8	24	88	62	TRUE	FALSE
3840	2160	3920	80	120	1075,804	4	540	8	24	44	60	TRUE	TRUE
3840	2160	3920	80	120	1075,804	2	810	8	24	44	62	TRUE	TRUE
3840	2160	3920	80	120	1075,804	1	1000	32	8	12	8	FALSE	FALSE
3840	2160	3920	80	144	1306,206	4	540	8	24	44	60	TRUE	TRUE
3840	2160	3920	80	144	1306,206	2	810	8	24	44	62	TRUE	TRUE
3840	2160	3920	80	144	1306,206	1	1350	32	8	12	8	FALSE	FALSE
3840	2160	3920	80	240	2285,203	4	1000	32	8	12	8	FALSE	FALSE
3840	2160	3920	80	240	2285,203	2	1350	32	8	12	8	FALSE	FALSE
5120	2160	5200	80	30	341,796	4	162	8	48	128	60	TRUE	FALSE
5120	2160	5200	80	30	341,796	2	270	8	48	128	62	TRUE	FALSE
5120	2160	5200	80	30	341,796	1	540	8	48	128	62	TRUE	FALSE
5120	2160	5200	80	60	693,264	4	270	8	24	88	60	TRUE	FALSE
5120	2160	5200	80	60	693,264	2	540	8	24	88	62	TRUE	FALSE
5120	2160	5200	80	60	693,264	1	810	8	24	88	62	TRUE	FALSE
5120	2160	5200	80	120	1427,088	4	540	8	24	44	60	TRUE	TRUE
5120	2160	5200	80	120	1427,088	2	1000	32	8	12	8	FALSE	FALSE
5120	2160	5200	80	120	1427,088	1	1350	32	8	12	8	FALSE	FALSE
5120	2160	5200	80	144	1732,723	4	540	8	24	44	60	TRUE	TRUE
5120	2160	5200	80	144	1732,723	2	1000	32	8	12	8	FALSE	FALSE
5120	2160	5200	80	144	1732,723	1	2000	32	8	12	8	FALSE	FALSE
5120	2160	5200	80	240	3031,392	4	1000	32	8	12	8	FALSE	FALSE
5120	2160	5200	80	240	3031,392	2	1350	32	8	12	8	FALSE	FALSE
7680	4320	7760	80	30	1019,896	4	540	8	24	88	60	TRUE	FALSE
7680	4320	7760	80	30	1019,896	2	810	8	24	88	62	TRUE	FALSE
7680	4320	7760	80	30	1019,896	1	1000	32	8	24	8	FALSE	FALSE
7680	4320	7760	80	60	2068,66	4	810	8	24	44	60	TRUE	TRUE
7680	4320	7760	80	60	2068,66	2	1000	32	8	12	8	FALSE	FALSE

Audio tests (Challenge #2 – Test Time)

- Source DUT
  - No Sources supporting DP Test Automation for Audio.
  - Around 2h to execute Audio tests for Source devices at non-UHBR link rates. (test 4.4.4.5 requires around 30 minutes of test operator time).
- Sink DUT
  - Listening check is required when test Sink devices.
  - Around 2h to execute Audio tests for Sink devices at non-UHBR link rates.
- Extending test procedures to cover UHBR link rates and DSC configurations estimated to double test time.

Audio CTS (Challenge #3)

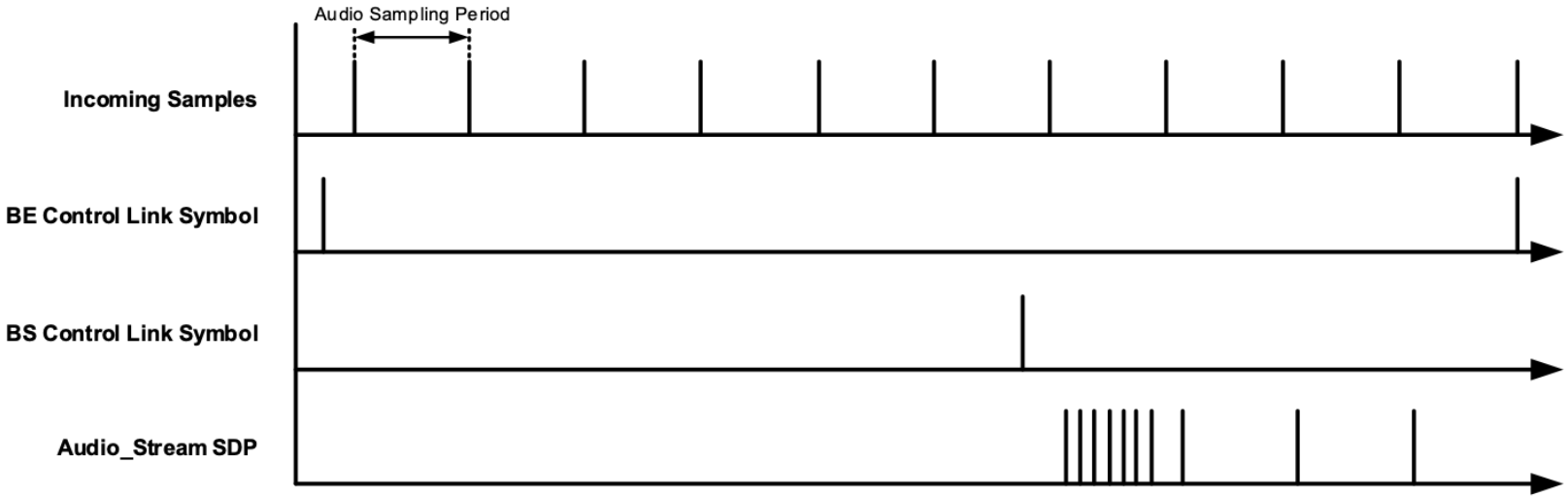


Figure A-2: Audio_Stream SDPs Transfer with Video during Video VActive Period

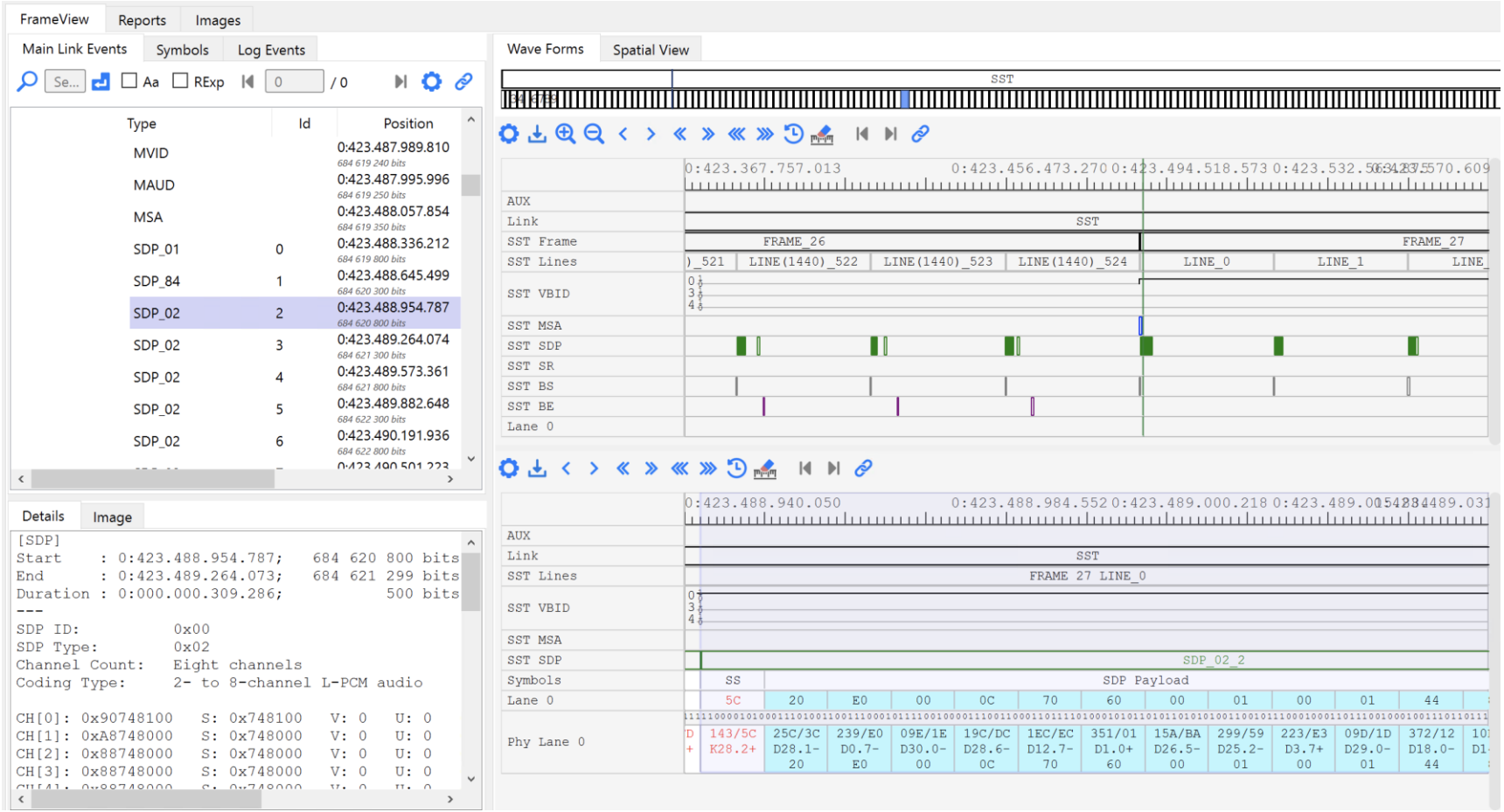
Audio CTS (Challenge #3) continued

$$floor(\frac{nF_s H_{total}}{F_p}) - 4 \le S_{tx} \le floor(\frac{nF_s H_{total}}{F_p}) + 4$$

where:

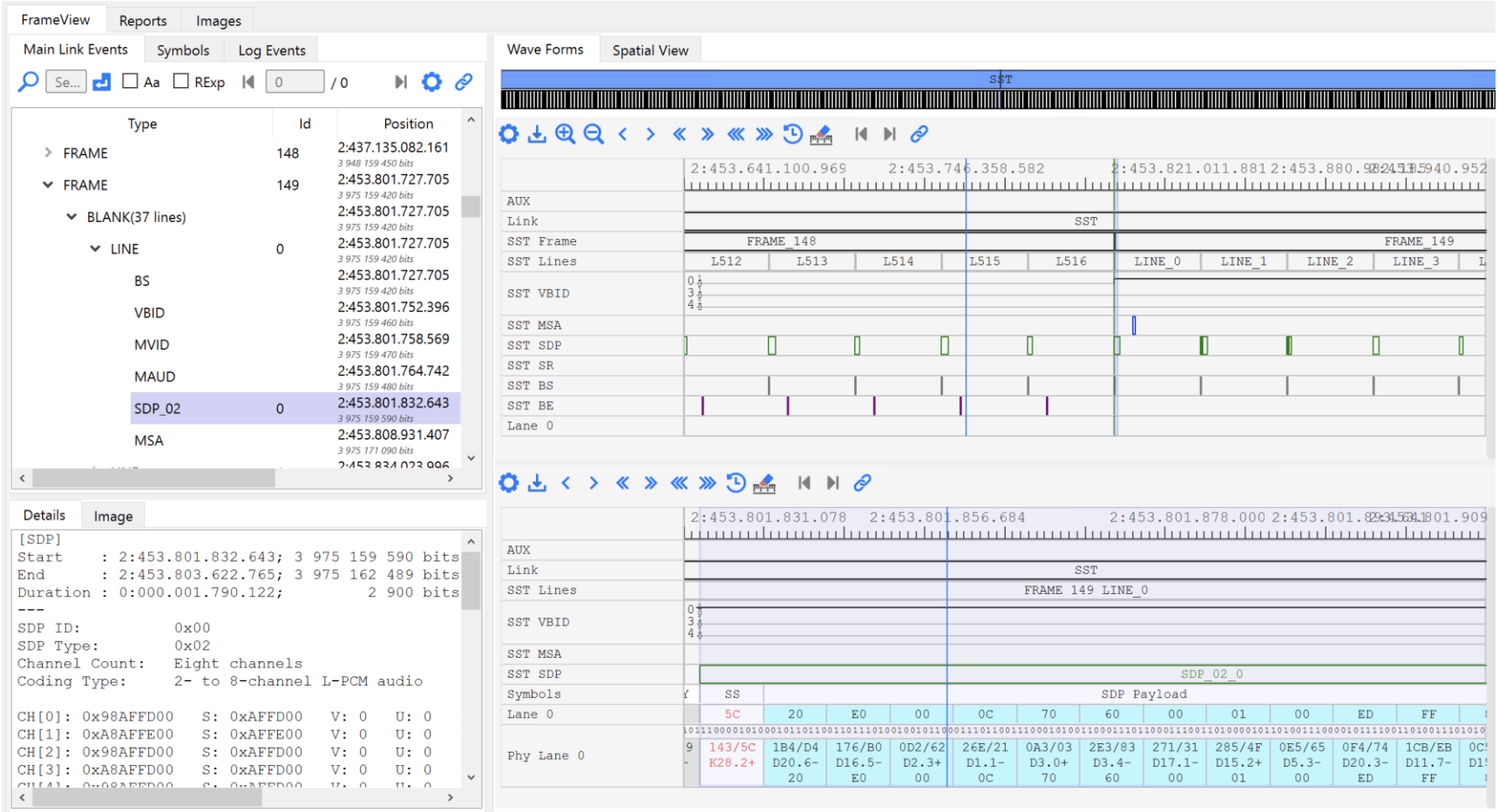
- S_{tx} is the number of audio samples received from the Source DUT over n consecutive lines
- F_s is the nominal audio sampling rate
- H_{total} is the horizontal total
- F_p is the pixel rate
- n is the number of lines

Source #1


FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Se...
Aa
RExp
0
/ 0
Type
Id
Position
MVID
0:423.487.989.810
684 619 240 bits
MAUD
0:423.487.995.996
684 619 250 bits
MSA
0:423.488.057.854
684 619 350 bits
SDP_01
0
0:423.488.336.212
684 619 800 bits
SDP_84
1
0:423.488.645.499
684 620 300 bits
SDP_02
2
0:423.488.954.787
684 620 800 bits
SDP_02
3
0:423.489.264.074
684 621 300 bits
SDP_02
4
0:423.489.573.361
684 621 800 bits
SDP_02
5
0:423.489.882.648
684 622 300 bits
SDP_02
6
0:423.490.191.936
684 622 800 bits
Details
Image
[SDP]
Start : 0:423.488.954.787; 684 620 800 bits
End : 0:423.489.264.073; 684 621 299 bits
Duration : 0:000.000.309.286; 500 bits

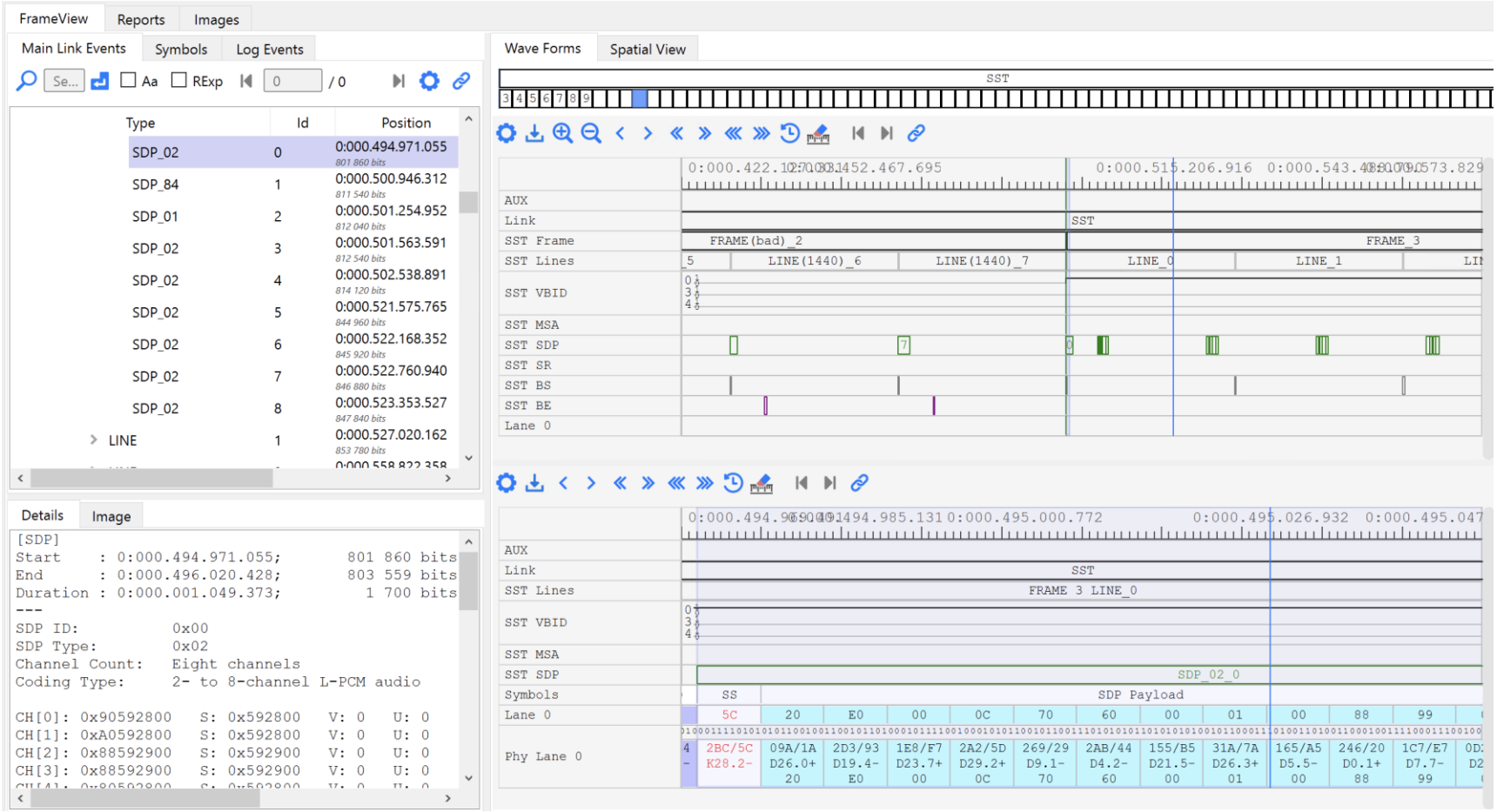
SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x90748100 S: 0x748100 V: 0 U: 0
CH[1]: 0xA8748000 S: 0x748000 V: 0 U: 0
CH[2]: 0x88748000 S: 0x748000 V: 0 U: 0
CH[3]: 0x88748000 S: 0x748000 V: 0 U: 0
Wave Forms
Spatial View
SST
0:423.367.757.013
0:423.456.473.270
0:423.494.518.573
0:423.532.563.875
AUX
Link
SST
SST Frame
FRAME_26
FRAME_27
SST Lines
)_521
LINE(1440)_522
LINE(1440)_523
LINE(1440)_524
LINE_0
LINE_1
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
0:423.488.940.050
0:423.488.984.552
0:423.489.000.218
0:423.489.031
FRAME 27 LINE_0
SDP_02_2
Symbols
SS
SDP Payload
5C
20
E0
00
0C
70
60
00
01
00
01
44
Phy Lane 0
143/5C
K28.2+
25C/3C
D28.1-
20
239/E0
D0.7-
E0
09E/1E
D30.0-
00
19C/DC
D28.6-
0C
1EC/EC
D12.7-
70
351/01
D1.0+
60
15A/BA
D26.5-
00
299/59
D25.2-
01
223/E3
D3.7+
00
09D/1D
D29.0-
01
372/12
D18.0-
44

Source #2


FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Se...
Aa
RExp
0
/ 0
Type
Id
Position
FRAME 148 2:437.135.082.161 3 948 159 450 bits
FRAME 149 2:453.801.727.705 3 975 159 420 bits
BLANK(37 lines) 2:453.801.727.705 3 975 159 420 bits
LINE 0 2:453.801.727.705 3 975 159 420 bits
BS 2:453.801.727.705 3 975 159 420 bits
VBID 2:453.801.752.396 3 975 159 460 bits
MVID 2:453.801.758.569 3 975 159 470 bits
MAUD 2:453.801.764.742 3 975 159 480 bits
SDP_02 0 2:453.801.832.643 3 975 159 590 bits
MSA 2:453.808.931.407 3 975 171 090 bits
Details
Image
[SDP]
Start : 2:453.801.832.643; 3 975 159 590 bits
End : 2:453.803.622.765; 3 975 162 489 bits
Duration : 0:000.001.790.122; 2 900 bits

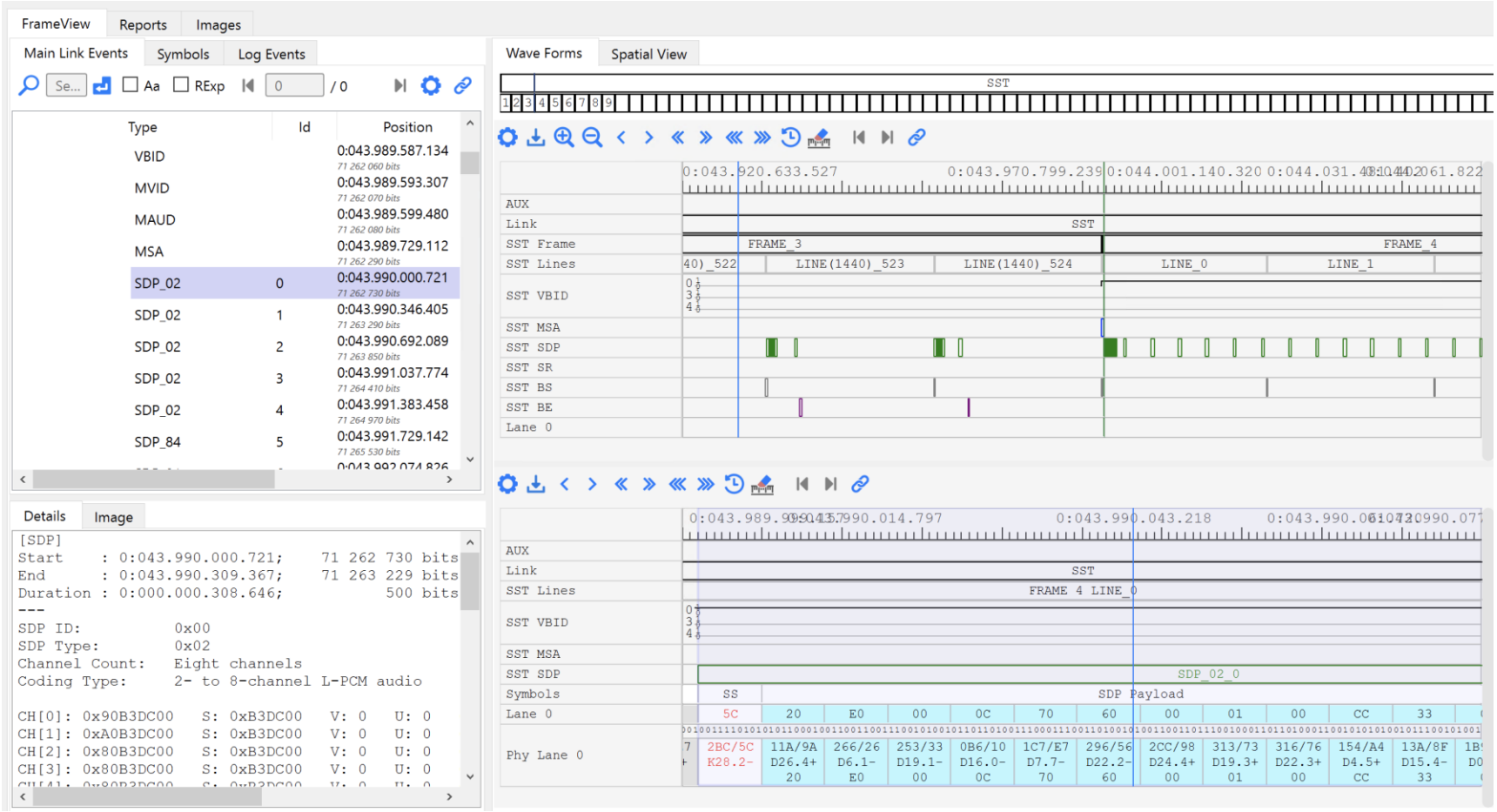
SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x98AFFD00 S: 0xAFFD00 V: 0 U: 0
CH[1]: 0xA8AFFE00 S: 0xAFFE00 V: 0 U: 0
CH[2]: 0x98AFFD00 S: 0xAFFD00 V: 0 U: 0
CH[3]: 0xA8AFFD00 S: 0xAFFD00 V: 0 U: 0
Wave Forms
Spatial View
SST
2:453.641.100.969
2:453.746.358.582
2:453.821.011.881
2:453.880.
2:453.940.952
AUX
Link
SST
SST Frame
FRAME 148
FRAME 149
SST Lines
L512
L513
L514
L515
L516
LINE_0
LINE_1
LINE_2
LINE_3
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
2:453.801.831.078
2:453.801.856.684
2:453.801.878.000
2:453.801.
SST
FRAME 149 LINE_0
SDP_02_0
Symbols
SS
SDP Payload
5C
20
E0
00
0C
70
60
00
01
00
ED
FF
Phy Lane 0
143/5C K28.2+
1B4/D4 D20.6- 20
176/B0 D16.5- E0
0D2/62 D2.3+ 00
26E/21 D1.1- 0C
0A3/03 D3.0+ 70
2E3/83 D3.4- 60
271/31 D17.1- 00
285/4F D15.2+ 01
0E5/65 D5.3- 00
0F4/74 D20.3- ED
1CB/EB D11.7- FF

Source #3


FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Aa
RExp
/ 0
Type
Id
Position
SDP_02 0 0:000.494.971.055 801 860 bits
SDP_84 1 0:000.500.946.312 811 540 bits
SDP_01 2 0:000.501.254.952 812 040 bits
SDP_02 3 0:000.501.563.591 812 540 bits
SDP_02 4 0:000.502.538.891 814 120 bits
SDP_02 5 0:000.521.575.765 844 960 bits
SDP_02 6 0:000.522.168.352 845 920 bits
SDP_02 7 0:000.522.760.940 846 880 bits
SDP_02 8 0:000.523.353.527 847 840 bits
LINE 1 0:000.527.020.162 853 780 bits
Details
Image
[SDP]
Start : 0:000.494.971.055; 801 860 bits
End : 0:000.496.020.428; 803 559 bits
Duration : 0:000.001.049.373; 1 700 bits

SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x90592800 S: 0x592800 V: 0 U: 0
CH[1]: 0xA0592800 S: 0x592800 V: 0 U: 0
CH[2]: 0x88592900 S: 0x592900 V: 0 U: 0
CH[3]: 0x88592900 S: 0x592900 V: 0 U: 0
Wave Forms
Spatial View
SST
AUX
Link
SST Frame
SST Lines
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
FRAME(bad)_2
FRAME_3
LINE(1440)_6
LINE(1440)_7
LINE_0
LINE_1
FRAME 3 LINE_0
SDP_02_0
Symbols
SS
SDP Payload
Phy Lane 0
5C
20
E0
00
0C
70
60
00
01
00
88
99
2BC/5C K28.2-
09A/1A D26.0+ 20
2D3/93 D19.4- E0
1E8/F7 D23.7+ 00
2A2/5D D29.2+ 0C
269/29 D9.1- 70
2AB/44 D4.2- 60
155/B5 D21.5- 00
31A/7A D26.3+ 01
165/A5 D5.5- 00
246/20 D0.1+ 88
1C7/E7 D7.7- 99

Source #4


FrameView
Reports
Images
Main Link Events
Symbols
Log Events
Se...
Aa
RExp
0
/ 0
Type
Id
Position
VBID
0:043.989.587.134
71 262 060 bits
MVID
0:043.989.593.307
71 262 070 bits
MAUD
0:043.989.599.480
71 262 080 bits
MSA
0:043.989.729.112
71 262 290 bits
SDP_02
0
0:043.990.000.721
71 262 730 bits
SDP_02
1
0:043.990.346.405
71 263 290 bits
SDP_02
2
0:043.990.692.089
71 263 850 bits
SDP_02
3
0:043.991.037.774
71 264 410 bits
SDP_02
4
0:043.991.383.458
71 264 970 bits
SDP_84
5
0:043.991.729.142
71 265 530 bits
Details
Image
[SDP]
Start : 0:043.990.000.721; 71 262 730 bits
End : 0:043.990.309.367; 71 263 229 bits
Duration : 0:000.000.308.646; 500 bits

SDP ID: 0x00
SDP Type: 0x02
Channel Count: Eight channels
Coding Type: 2- to 8-channel L-PCM audio
CH[0]: 0x90B3DC00 S: 0xB3DC00 V: 0 U: 0
CH[1]: 0xA0B3DC00 S: 0xB3DC00 V: 0 U: 0
CH[2]: 0x80B3DC00 S: 0xB3DC00 V: 0 U: 0
CH[3]: 0x80B3DC00 S: 0xB3DC00 V: 0 U: 0
Wave Forms
Spatial View
SST
0:043.920.633.527
0:043.970.799.239
0:044.001.140.320
AUX
Link
SST
SST Frame
FRAME_3
FRAME_4
SST Lines
LINE(1440)_523
LINE(1440)_524
LINE_0
LINE_1
SST VBID
SST MSA
SST SDP
SST SR
SST BS
SST BE
Lane 0
0:043.990.014.797
0:043.990.043.218
FRAME 4 LINE_0
SDP_02_0
Symbols
SS
SDP Payload
5C
20
E0
00
0C
70
60
00
01
00
CC
33
Phy Lane 0
2BC/5C K28.2-
11A/9A D26.4+ 20
266/26 D6.1- E0
253/33 D19.1- 00
0B6/10 D16.0- 0C
1C7/E7 D7.7- 70
296/56 D22.2- 60
2CC/98 D24.4+ 00
313/73 D19.3+ 01
316/76 D22.3+ 00
154/A4 D4.5+ CC
13A/8F D15.4- 33

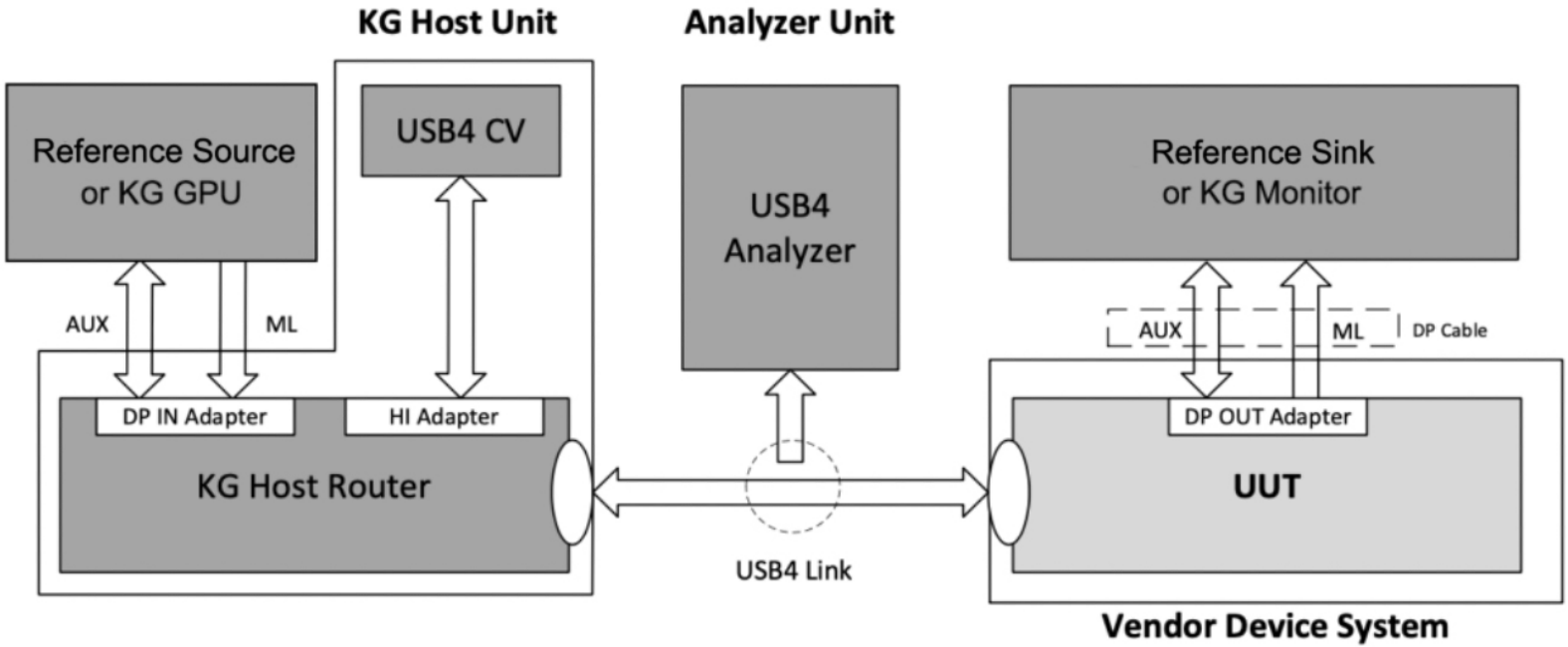
Audio CTS (Conclusions)

- No easy way to upgrade DP 1.4 8b/10b SST Audio CTS to cover DP 2.1 requirements
- Due to test time increase, it is suggested to test Audio at UHBR rates under separate tests. Under discussion now.
- It is suggested to test Audio at 8b/10b link rates also in MST mode. Not covered yet by SCR under review. To be discussed

USB4 DP Tunneling CTS

- Collaborating closely with USB-IF and ATCs
- Revision 2.2 released in August 2024
- Test procedures for Host, Device and Hub
- Test Setups with Known Good Devices and DisplayPort Test Equipment as Reference Sink/Source.
- For Test Setups with Reference Sink/Source lists DP 2.1 Link Layer tests to be performed
- Work in progress. Looking for a balance between test coverage and test time

USB4 DP Tunneling CTS (continued)



Various updates after revision 1.0 release

- DP 2.1 Link Layer CTS is evolving and improving
- VESA Members actively reviewing and commenting DP 2.1 Link Layer CTS
- Comments are used to draft new tests and update existing test procedures
- Draft 5 of the SCR consolidating such updates is under adoption vote

Source DUT updates

- 4.2.2.13 Native AUX defer retry validation for Source DUT before LT
- 4.2.2.14 Native AUX defer retry validation for Source DUT during LT just after TPS1
- 4.9.1.22 With 1 emulated LTTPR, Successful Link Training at any Lane Counts and Link Speeds
- 4.3.2.5 Lane Count Reduction (Deprecated)
- Allow Reference Sink to have DSC capability cleared for improving uncompressed Video tests automation at UHBR link rates

Sink DUT updates

- 5.6.3.7 DSC Validation for max supported pixel rate format at max UHBR Rate
- 5.4.3.3 Entering and Exiting Power Save Mode at UHBR rate
- 5.4.3.4 Resumption of Main-Link Activity after Extended Idle at UHBR rate
- 5.7.14.7 Hblank and Vblank Validation

LTTPR DUT updates

- 7.1.4.8 With 0 emulated LTTPR, Link Training with UFP fails when DFP not able to do EQ lock at max supported Lane Count and 128b/132b DP Link Speeds in Non-transparent mode
- 7.1.4.9 With 5 emulated LTTPR, Link Training with UFP fails when DFP not able to do EQ lock at max supported Lane Count and 128b/132b DP Link Speeds in Non-transparent mode
- 7.1.4.10 With 5 emulated LTTPR, Link Training with successful link training at max supported Lane Count and 128b/132b DP Link Speeds in Non-transparent mode

Minimal Vblank and Hblank requirements

- *"There are quite a few "high" refresh rate monitors (mainly for a gaming use case) that has a VBLANK period way shorter than 300 uSec, let alone 460 uSec listed as the minimum VBLANK period in VESA CVT Standard"*
- Sinks that do not honor specified minimum Vblank and Hblank periods can have interoperability issues with Source devices that expect these intervals to meet specification limits
- New EDID/DisplayID compliance test for Sink devices is drafted: 5.7.14.7 Hblank and Vblank Validation

Planned updates to DP 2.1 LL CTS

- Introduce MST tests
- Update Branch device tests to DP 2.1 requirements
- Introduce Panel Replay and ALPM tests
- Introduce HBR Audio tests

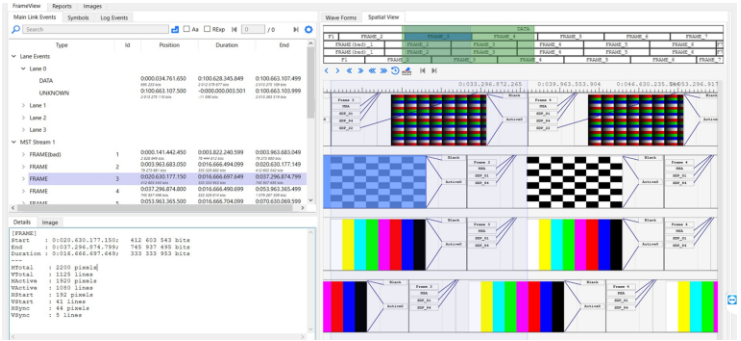
UCD-500 Gen2

16K DP 2.1 Generator & Analyzer

- DP 2.1 Sinks and Sources up to 8K@60Hz (16K@60Hz with DSC), 4 lanes, UHBR20
- DP and USB-C connections
- DSC, FEC, MST, LTTPR, PD etc….
- DP 2.1 Link Layer CTS Tool including
  - DSC, LTTPR, DisplayID/EDID, Adaptive-Sync compliance tests
- HDCP 2.3 CTS
- Now featuring Link Analyzer, Panel Replay and ALPM test functions

16K UHD

DP 2.1 LL CTS



Thank You

DP LRD Active Cable Testing Challenges and DP2.1 Connector Certification

Lexus Lee

Allion Labs,Inc

2024/10/21

Overview

- VESA LRD Active Cable Testing Challenges
- VESA Enhanced Connector Compliance Test Introduction

Overview

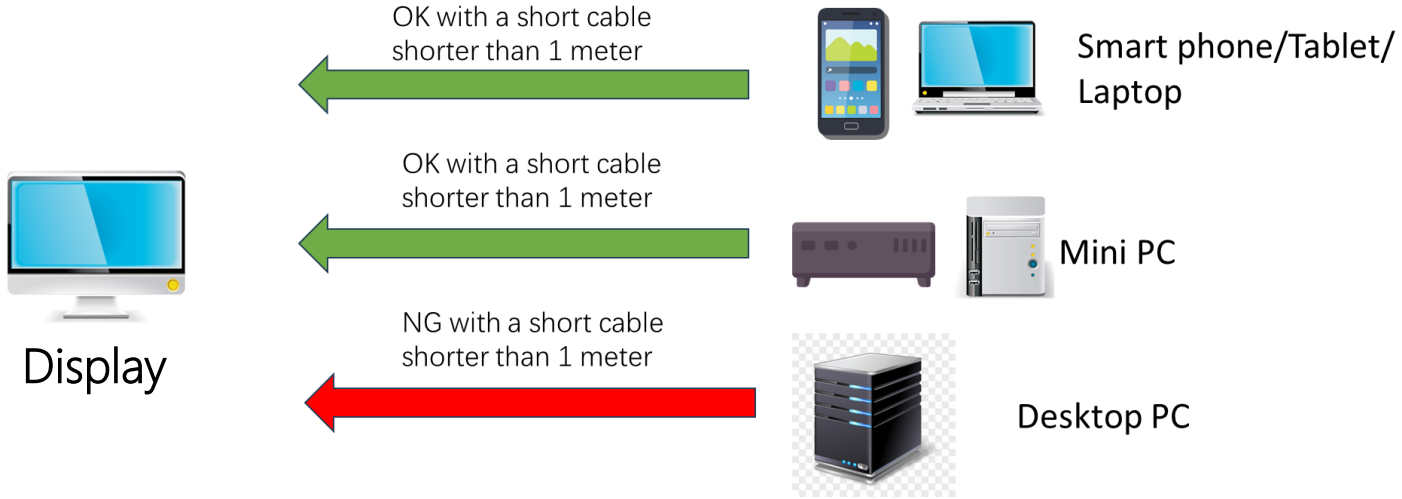
- VESA LRD Active Cable Testing Challenges
- VESA Enhanced Connector Compliance Test Introduction

The Current UHBR Passive Cable Status

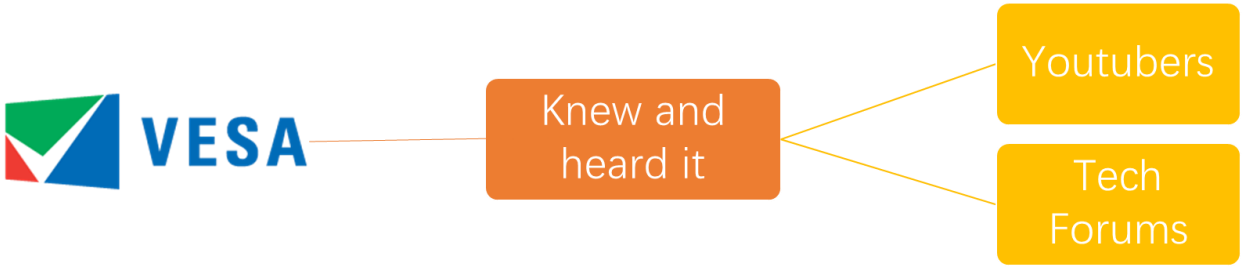
- DP to DP and USB-C to DP Passive cables for UHBR transmission
  - According to DP2.1a spec
    - UHBR 20-Capable Passive cable length: around 1 meter
    - UHBR 13.5-Capable Passive cable length: around 2 meters

- Criticism of UHBR20 ecosystem from youtubers and tech forums.

The Current UHBR Passive Cable Status Cont’



DisplayPort LRD Active Cable Solution

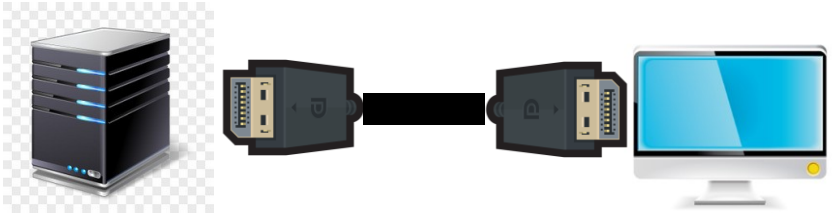


- VESA is going to bring us a solution to the criticism this year.
  - LRD Active Cable Solution
    - Get UHBR20 transmission to successfully work longer than 2 meter-long cable.
    - Creating a LRD Active Cable CTS

CTS Testing Challenges

- Knowledge to get DP LRD cable to work up
  - AUX and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Aux P: Pull down to GND
2. Aux N: Pull high to 2.89~3.6V.
3. DP_PWR:2.89~3.6V
4. Aux transaction if needed

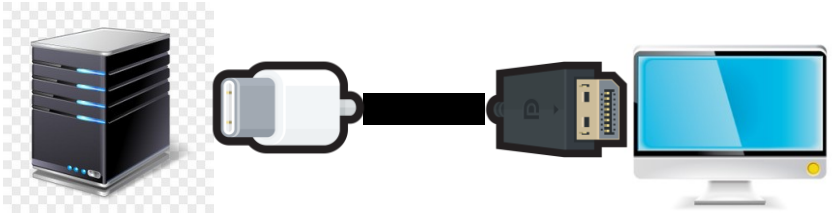


1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull high to 2.25~3.6V
5. Aux transaction if needed

CTS Testing Challenges Cont’

- Knowledge to get C to DP LRD cable to work up
  - Vconn, AUX, and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Vconn:3.0~5.5V
2. DP alt mode exerciser if needed.
3. Aux circuitry if needed.
4. Aux transaction if needed



1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull High to 2.25~3.6V
5. Aux transaction if needed

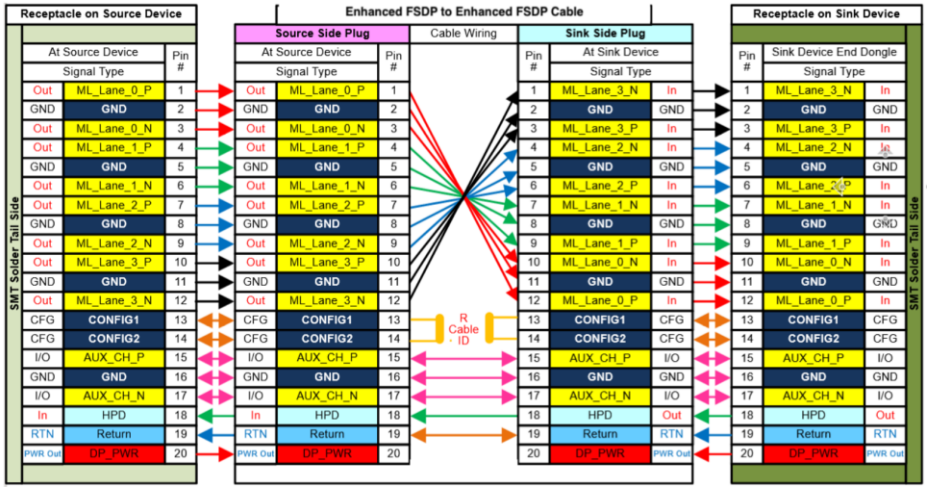
CTS Testing Challenges Cont’

- Power Consumption Check Before You Start Any Test
  - Do Link Training for
    - 1 Lane
    - 2 Lanes
    - 4 Lanes
  - Observe the current change of Vconn or DP PWR.
    - For example

	1 Lane	2 Lanes	4 Lanes
Current	80mA	170mA	380mA

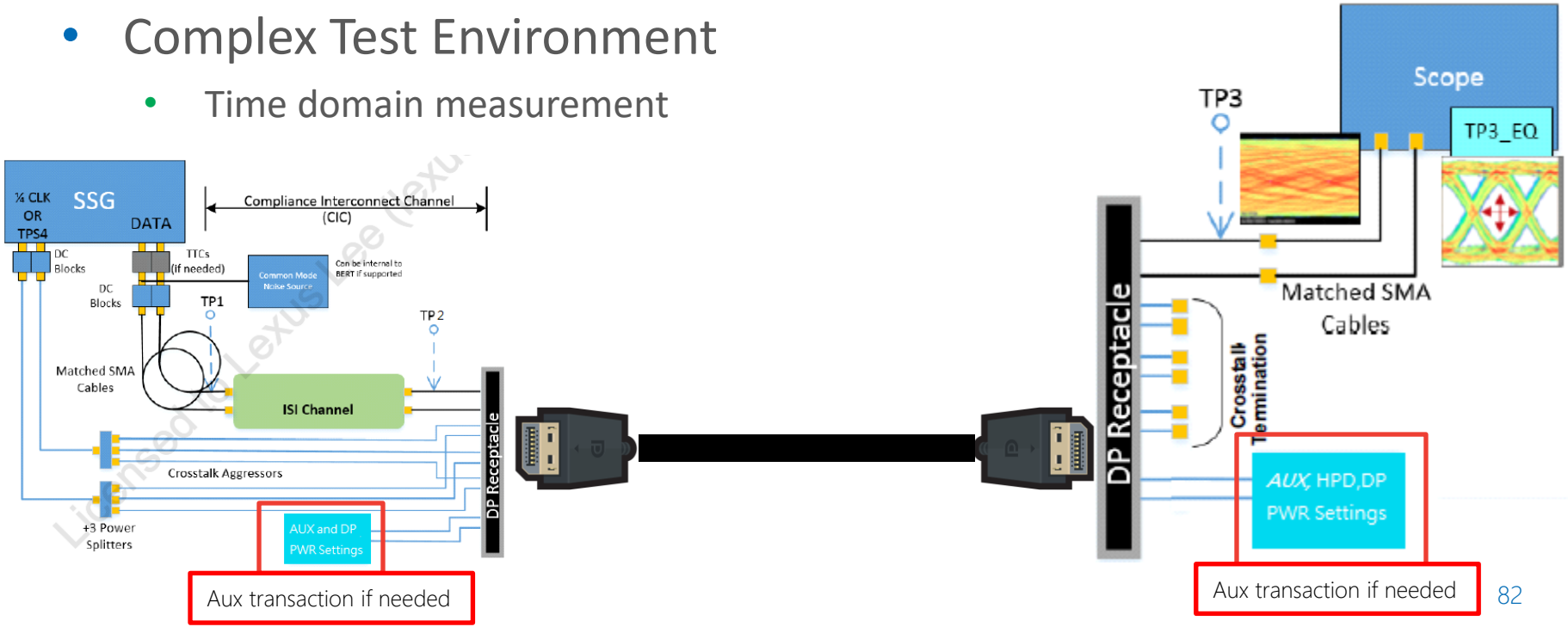
CTS Testing Challenges Cont’

- Know how the wires inside a DP cable are connected at both ends.
  - Look at high speed pairs, please



CTS Testing Challenges Cont’

- Complex Test Environment
  - Time domain measurement

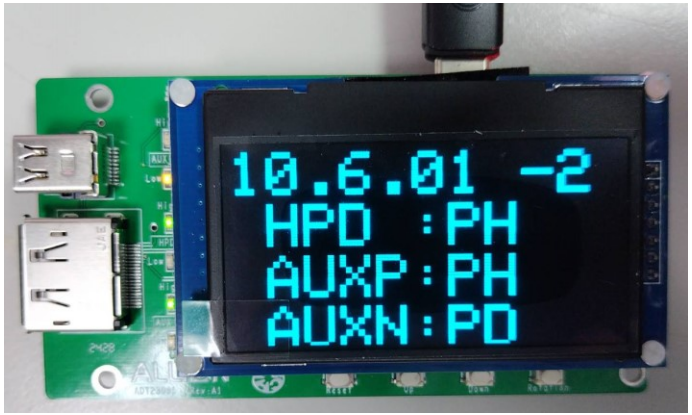


CTS Testing Challenges Cont’

- Complex Test Environment
  - Frequency domain measurement

CTS Testing Challenges Cont’

- Allion Test Fixture
  - Help to reduce the complex connection for your LRD cable testing.
    - Powered by USB-C port
    - Controllable HPD, AUX_P, and AUX_N

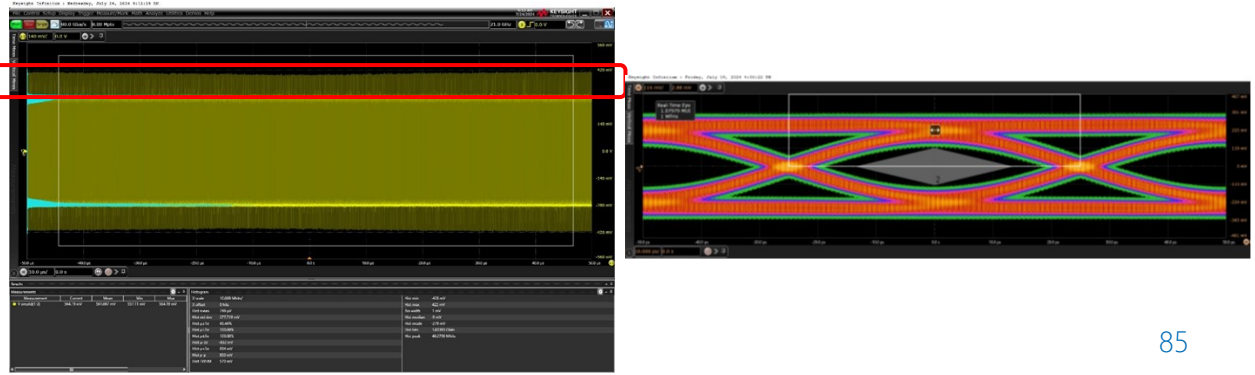


CTS Testing Challenges Cont’

- Stressed Signal Generator
  - Preset Calibration
    - Very important to stressed signal defined by DP spec.
    - Inaccurate preset number gets your stressed signal to highly not meet the expected ISI jitter, Eye Height, and Eye width.

Table 3-57: Preset FFE Coefficients[a b]

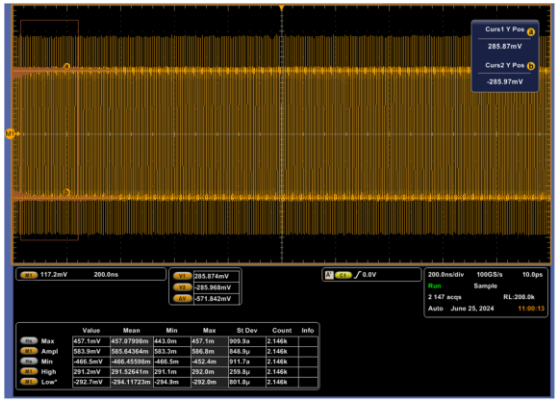
Preset Configuration #	Preshoot (dB)	De-emphasis (dB)	Informative Filter Coefficients		
			C_{-1}	C_0	C_{+1}
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0

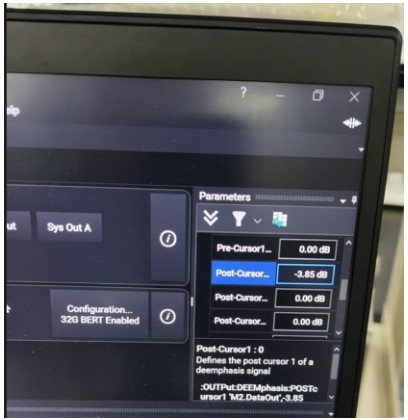


CTS Testing Challenges Cont’

- Stressed Signal Generator Cont’
  - Preset Calibration Cont’
    - Do not just enter the number that you want into your SSG FFE setting.

(SQ128) Rough De-emphasis: 20 log(585.6/923.4)=-3.95dB





Overview

- VESA LRD Active Cable Testing Challenges
- VESA Enhanced Connector Compliance Test Introduction

Latest DisplayPort Connector Spec Cont'

- Connector Types:

Type	Definition
Legacy	• Supports up to 8.1Gbps/lane(HBR) • Includes both an fsDP and an mDP version
Enhanced	• Enhanced fsDP Type 1 connector supports up to 13.5Gbps/lane(UHBR13.5) • Enhanced fsDP Type 2 connector supports up to 20Gbps/lane(UHBR20) • Enhanced mDP connector supports up to 20Gbps/lane(UHBR20)

Latest DisplayPort Connector Spec Cont'

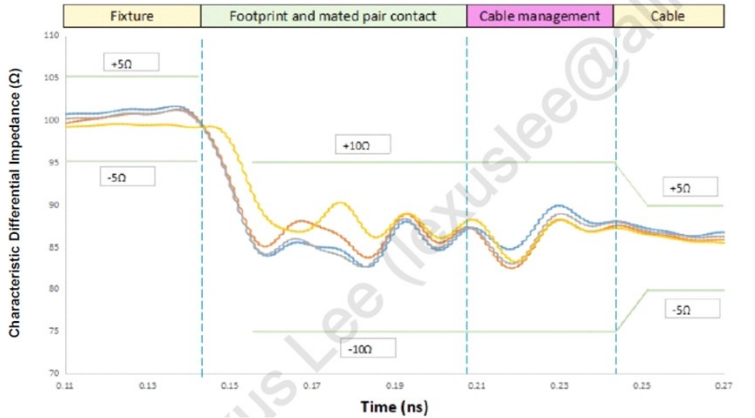
- Footprint Compatibility Matrix:

fsDP Conn/Footprint Type	Legacy PCB Footprint	Enhanced PCB Footprint Type 1	Enhanced PCB Footprint Type 2
Legacy	OK with HBR3	OK with HBR3	Ok with HBR3
Enhanced Type 1	N/A	OK with UHBR13.5	N/A
Enhanced Type 2	N/A	N/A	OK with UHBR20

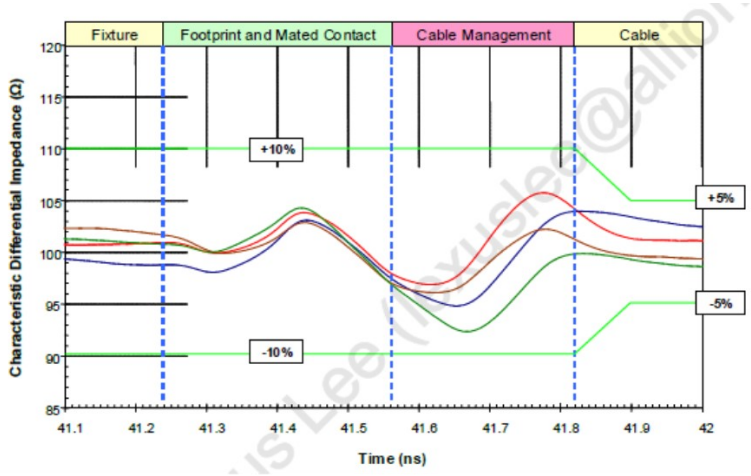
mDP Conn/Footprint Type	Legacy PCB Footprint	Enhanced PCB Footprint
Legacy	OK with HBR3	N/A
Enhanced	N/A	OK with UHBR20

Latest DisplayPort Connector Spec Cont'

- Discrepancy of Impedance:



Enhanced DP/mDP Connector

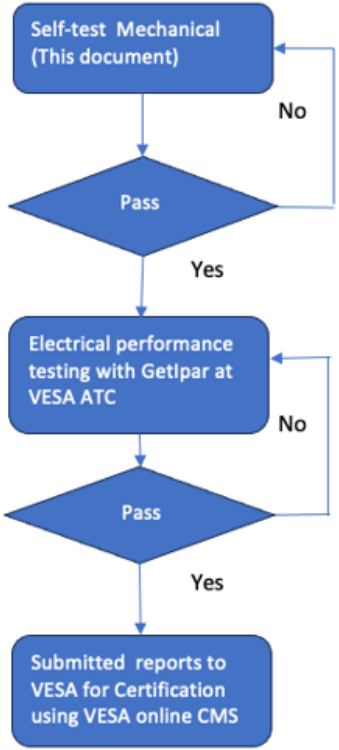


Legacy fsDP Connector

DP Enhanced Connector Compliance program

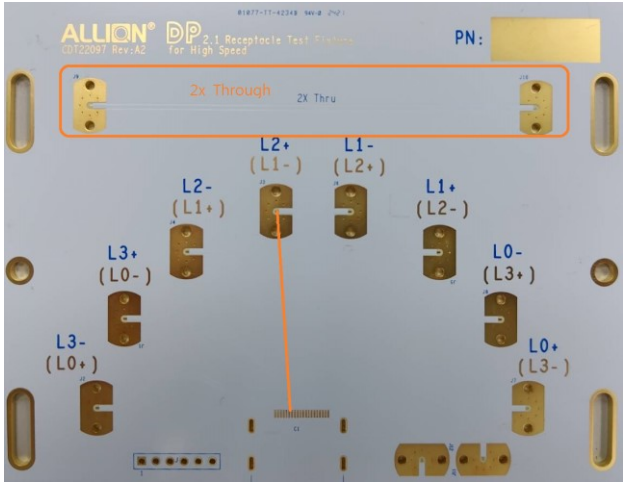
- Certification Flow:

VESA® DisplayPort™ Self-Test Report for Connectors v2.1



DP Enhanced Connector Compliance Program Cont'

- Test Fixture Check:
  - Intra-pair skew < or = 2ps
  - 1x&2x thru accuracy check
    - (2x through length)/2 < or = 1x through length
    - In order to avoid compensating too much.



DP Enhanced Connector Compliance Program Cont'

- Test Concept:
  - Test the Connector DUT with a certified cable
    - Pass/ Fail Criteria based on the "cable" requirement defined in the DP2.1a spec.
  - Test the certified cable with one of the Known Good Receptacle fixtures(KGF)
    - KGF1 and KGF2 are Bizlink and Wieson respectively
    - Test data submitted as a reference

Thank you

Compliance Testing

VESA PlugTest Events

- Provide significant value to member companies, particularly as new capabilities and products are deployed.
- Demonstrate and improve Traditional Interoperability
- Test Native DP and DP Alt Mode over USB Type-C™ products
  - UHBR rates, DSC, FEC, DisplayHDR and other new capabilities
  - Verify Test Equipment Correlation
- VESA hosted two successful PlugTests in 2023 (Taiwan and US)
- VESA hosts two PlugTests in 2024
  - Hawaii, USA: **Q1 2024 (completed)**
  - Taipei, Taiwan: **Q4 2024 (Oct 14-18th Taiwan)**

DP40, DP54 and DP80 Cable Specification and Certification program

- Enhanced DP cable and connector specifications and test requirements started in 2021
- DP54 and DP80 Certified cables – give users confidence UHBR10, UHBR13.5 and UHBR20 Gbps links work
- Over 150 Enhanced DP cables and connectors have been certified
- DP40 cable performance tier replaced with DP54 in 2024
- DP54 cables = UHBR10 and UHBR13.5 link rate performance

Product certifications* 2022/2023/2024

Products	2022	2023	2024
DP Sources	141	99	60
DP Sinks	339	277	320
DP Cables	42	59	56
DisplayHDR	388	397	369
ClearMR	14	45	30
AdaptiveSync	25	80	48

*Note: numbers are base model certs not including family models

VESA Technology Development Areas

VESA technology development

- VESA members are collaborating on several key technology areas
- Embedded DisplayPort - v2.0 (published Sept 2024)
- DP Tunneling over USB4 – compliance testing has begun
- AR/VR Task Group
  - Focused on creating solutions roadmap to meet performance, power and implementation requirements for future AR/VR needs. Specification is released. Work on CTS underway
- DP Automotive Extension Task Group
  - Working with automotive industry to address needs for high-resolution performance in this market segment
  - Working on DP AE CTS and testing
- Bulk Display Protocol
  - BDP specification and CTS nearing release
- Display Performance Metrics Task Group
  - DisplayHDR, ClearMR, AdaptiveSync

Summary

Summary

- Product shipments and certifications on based on VESA technologies continue to grow
- DP 2.1 UHBR capable product development and certifications have ramped up in 2024
- VESA Enhanced cable and connector certification programs have been very successful with significant numbers of DP40, DP54 and DP80 cables certified
- DisplayPort over USB-C is a game changer for small form factor and portable products and is now the defacto standard for laptops, tablets and handheld devices
- Display Performance Standards adoption and certification have been extremely successful the last several years
- Development and adoption of new technologies continues to drive increases in VESA membership growth

VESA

THANK YOU

DisplayPort.org
DisplayHDR.org
ClearMR.org
AdaptiveSync.org
VESA.org

Thank you for attending the VESA Workshop Tokyo, Japan 2024