Welcome
VESA Workshop
San Francisco, CA, USA
2025

VESA Workshop Agenda

Time	Topic	Speaker
10:00am	VESA Overview and Standards Updates, Including DisplayPort v 2.1b	Alan Kobayashi, VESA Board and DisplayPort Task Group Chair
10:30am	VESA Compliance Program	Jim Choate, VESA Compliance Manager
11:00am	DP2.1 Panel Replay and Advanced Link Power Management: Implementation and Testing Challenges	Marco Denicolai, Product Owner, IP Cores, Unigraf Oy
11:30am	DisplayPort Link Layer CTS v 2.1 MST Updates	Alok Soni, Software Lead, Teledyne LeCroy
12:00pm – 1:00pm	Lunch	
1:00pm	eDP and DP v 2.1 PHY CTS Overview and Updates	Abhijeet Shinde, Product Manager, Edge AI, Keysight Technologies
1:30pm	DP Alt Mode v 2.1a Overview and CTS Updates	Tim Wei, Senior Application Engineer, Ellisys
2:00pm	LRD/Active Cable Testing and DP 2.1 Enhanced Connector Certification	Lexus Lee, Technical Program Manager, Allion Labs
2:30pm – 2:45pm	Break	
2:45pm	VESA Display Panel Standards (ClearMR, DisplayHDR, AdaptiveSync)	Roland Wooster, Display Architect, Principal Engineer, Intel Corporation
3:15pm	Automotive Extension Services	Tung-Sheng Lin, Senior Technical Manager, MediaTek
3:35pm	Summary, Questions & Answers	Jim Choate, VESA Compliance Manager
3:50pm	Demo Stations Overview	

VESA's Mission and Latest/Upcoming DP Standards Family

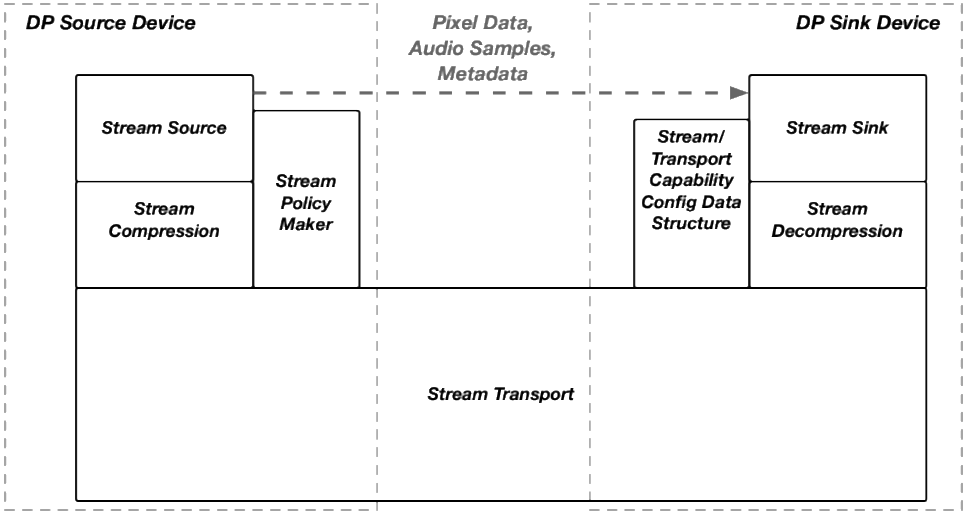
Alan Kobayashi

VESA Board Chair, VESA DisplayPort Task Group Chair

23-MAY-2025

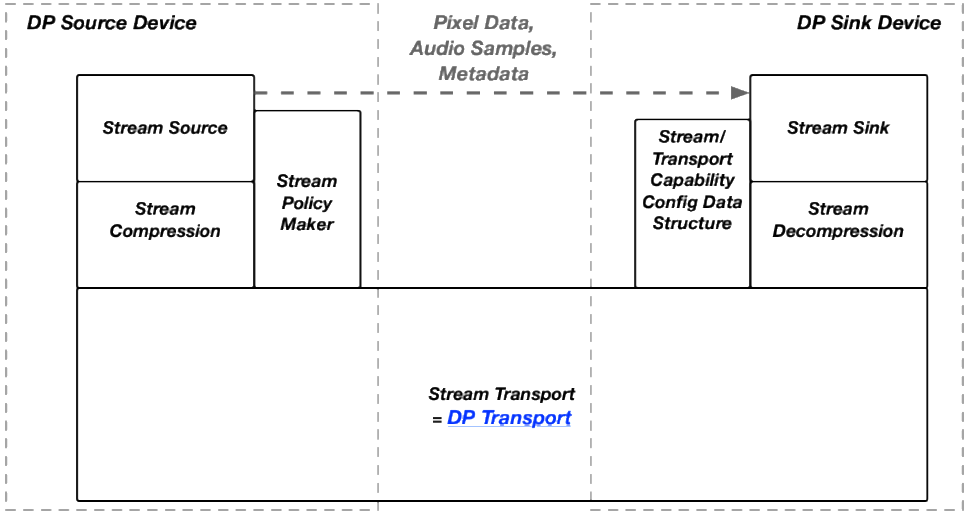
Interoperable End-to-End Visual Ecosystem

- Ensuring interoperability of display stream transport from Stream Source (e.g., GPU) to Stream Sink (e.g., Monitor)



Interoperable End-to-End Visual Ecosystem

- Ensuring interoperability of display stream transport from Stream Source (e.g., GPU) to Stream Sink (e.g., Monitor)
  - Stream Transport
    = DisplayPort (DP) via DP, USB-C, or USB-C-to-DP cable
  - DP transport consists of
    - Main Link:
      - Pixel Data, Audio Samples, and Metadata transport
    - AUX_CH and HPD:
      - Sideband communication for plug/unplug detection, capability discovery/configuration/status, status change notification



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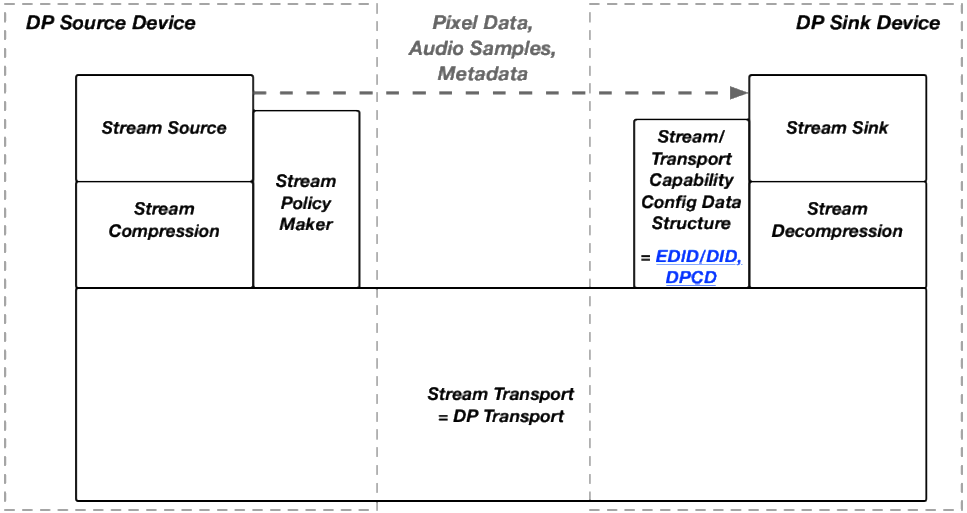
  - Capability/Config Data Structure
    - Stream Sink = EDID/DisplayID
    - DPRX = DPCD



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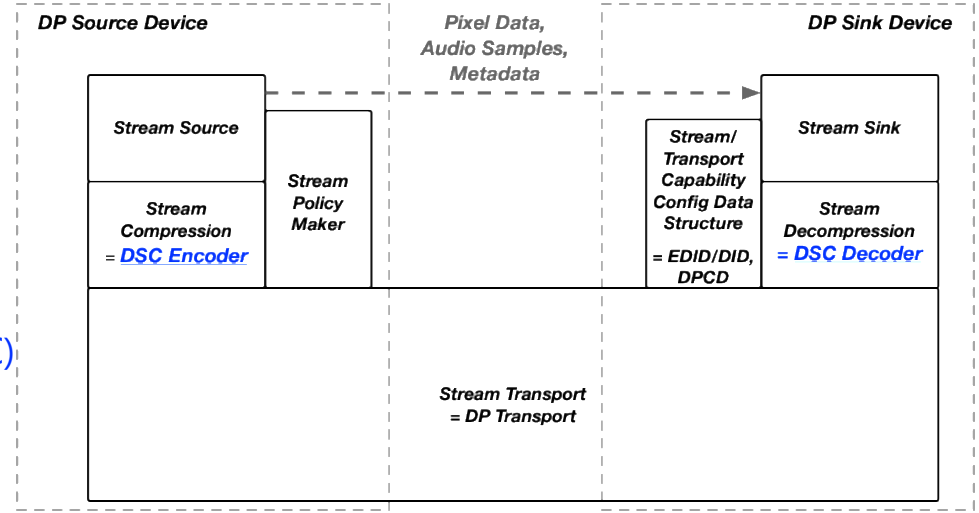
    = EDID/DisplayID for Stream and DPCD for Transport
  - Stream Compression
    = Display Stream Compression (DSC)



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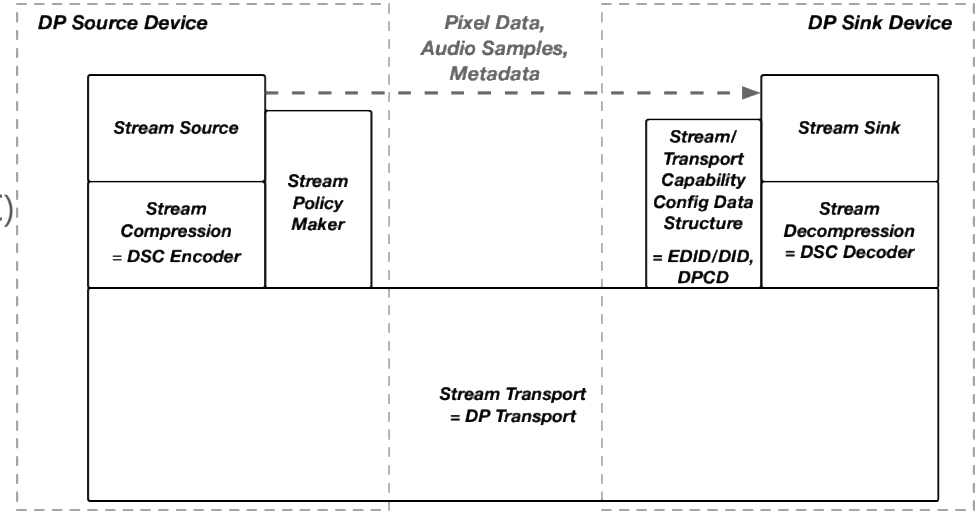
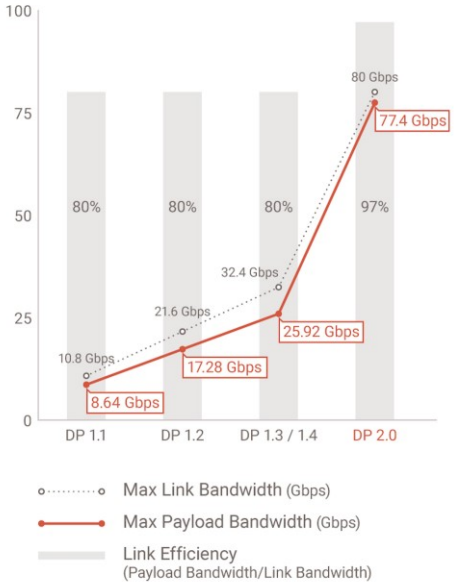
- Visual performance accountability
  - Display Performance Metrics (DPM)



Stream Transport Headroom Provided by DPv2.x

- UHBR20 added in DPv2.x provides for 3x payload (= usable) bandwidth of HBR3
  - Link rate increase + channel coding efficiency improvement (from 8b/10b to 128b/132b)
- "DSC mandate" added in DPv2.x significantly increases the transportable stream bandwidth
  - 4-lane HBR3 with DSC sufficient for 4K2K240
    - Also, good for 4x 4K2K60 monitors cascaded/via an MST dock
  - 4-lane UHBR20 with DSC sufficient for 12K2K240
    - Also, good for 3x 4K2K240 monitors cascaded/via an MST dock



DP Standard Version Number…

- It is a “never dying” habit to associate DP Standard version number to the maximum link rate supported…
  - DPv1.1 = HBR (2.7 Gbps/lane)
  - DPv1.2 = HBR2 (5.4 Gbps/lane)
  - DPv1.4 = HBR3 (8.1 Gbps/lane)
  - DPv2.x = UHBR rates (10/13.5/20 Gbps/lane)

DP Standard Version Number…

- However, only the latest version is active per VESA policy
  - The latest, and, thus, active, version is DPv2.1a released December 2023
  - A new standard version comes with:
    - New features not related to link rate (e.g., Panel Replay, Adaptive-Sync SDP payload extension in v2.x)
    - Interop improvement policy updates
- "My device supports up to 4-lane HBR2 with DSC and Panel Replay support"
  - HBR2 introduced in DPv1.2
  - DSC introduced in DPv1.4
  - Panel Replay introduced in DPv2.0

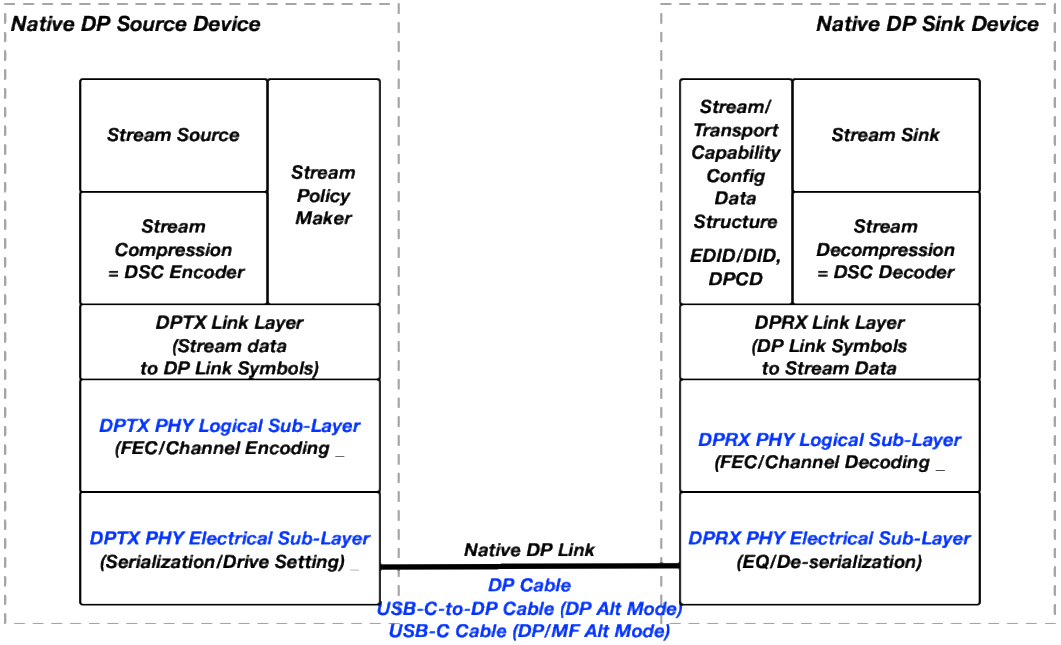
Two Types of DP Transport

- Native DP Transport
  - Uses DP PHY Layer to transport DP Link Symbols carrying stream data
  - Cable types
    - A DP cable
    - A USB-C cable or a USB-C-to-DP adapter cable: DP/Multi-Function (MF) Alt Mode
      - DP/MF Alt Modes are Native DP transport as they use DP PHY Layer to transport DP Link Symbols
- Tunneled DP Transport
  - Uses USB4 PHY Layer to transport Tunneled DP USB4 packets encapsulating DP Link Symbols carrying stream data
  - Cable type
    - A USB-C cable

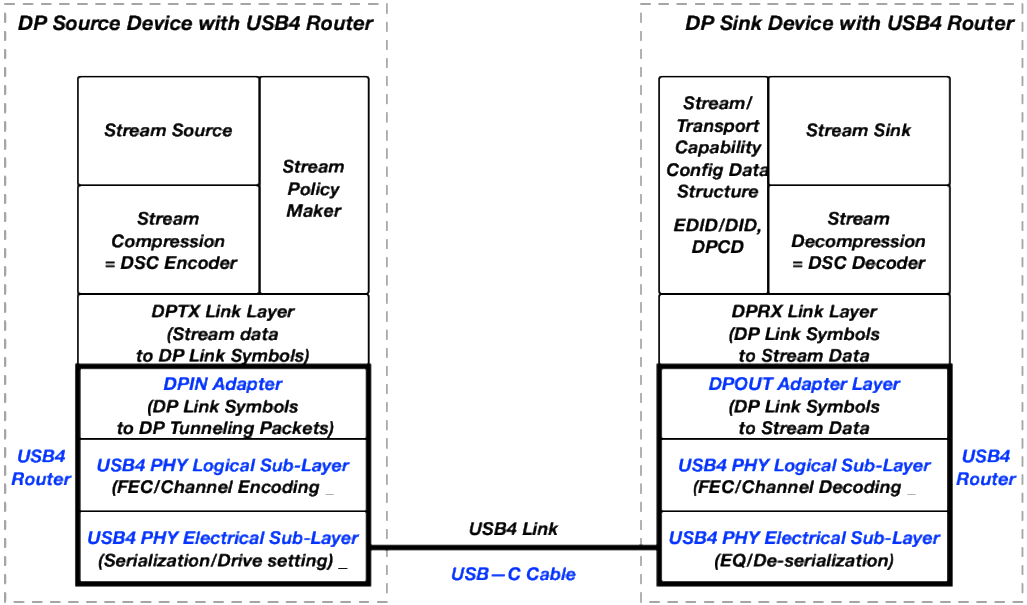
Native/Tunneled DP Mapping to Connector Pins

	Native DP		Tunneled DP
	DP Connector	**USB-C Connector**	**USB-C connector**
Main Link Data	ML0_P/_N ~ ML3_P/_N pins	TXp1/TXn1, TXp2/TXn2, RXp1/n2, and RXp2/n2 pins	Main Link Data, AUX transaction, and HPD event all encapsulated to Tunneled DP USB4 packets over USB4 Main Laines
AUX_CH	AUX_CH_P/_N pins	SBU1/SBU2 pins	
HPD	HPD pin	HPD event encapsulated in USB PD packet over CC pin	
Power	DP_PWR	V_CONN/VBUS	V_CONN/VBUS

Native DP Transport

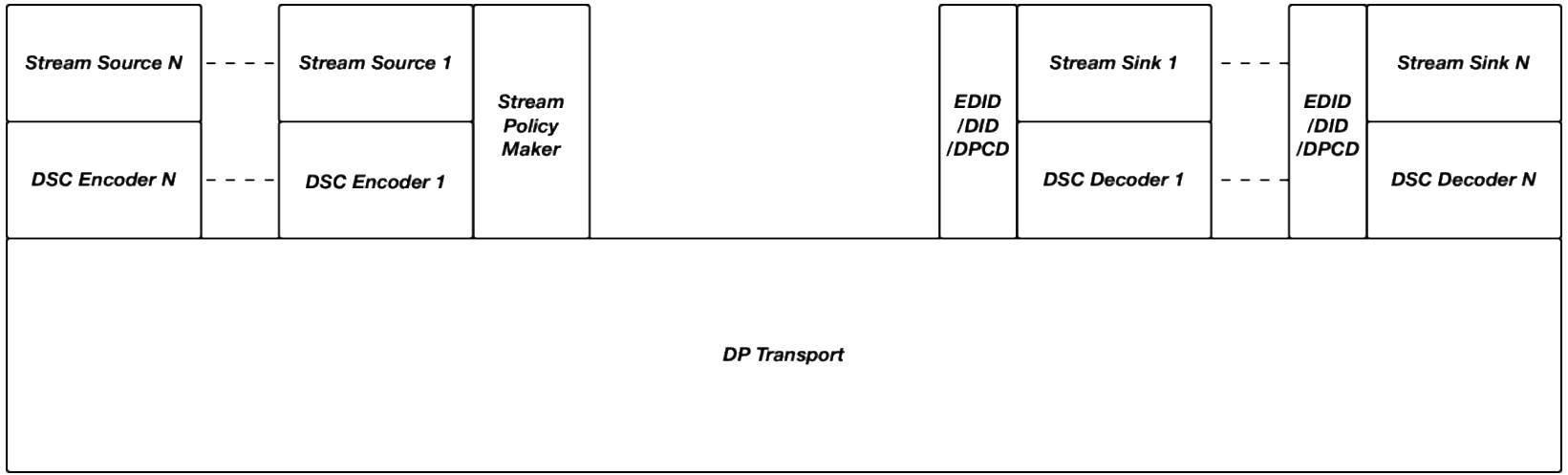


Tunneled DP Transport



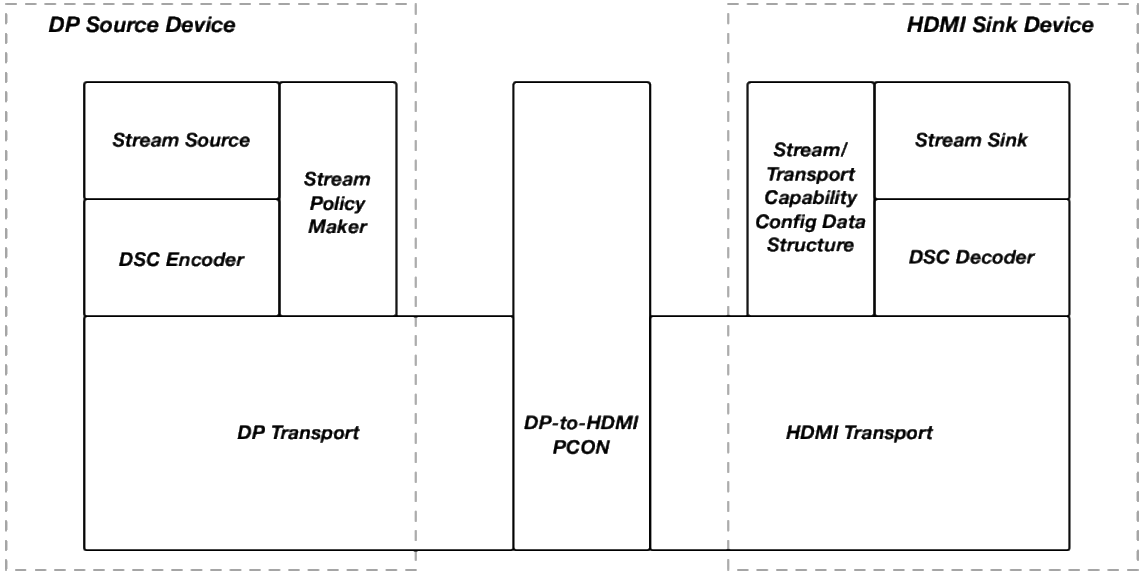
Supporting Transport of Multiple Streams

- Native DP Transport: DP MST (Multi-Stream Transport)
- Tunneled DP Transport: Tunneling of DP MST link or multiple DP SST (Single Stream Transport) links



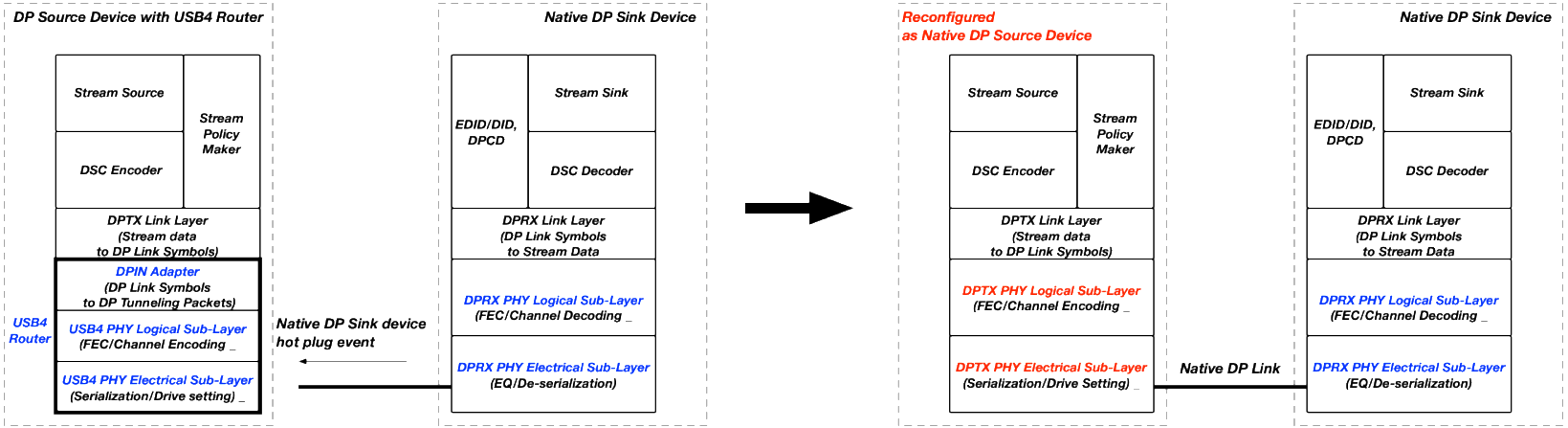
Supporting Non-DP Stream Transport

- Via PCON (Protocol Converter): E.g., DP-to-HDMI PCON
  - DP Standard defines PCON specification



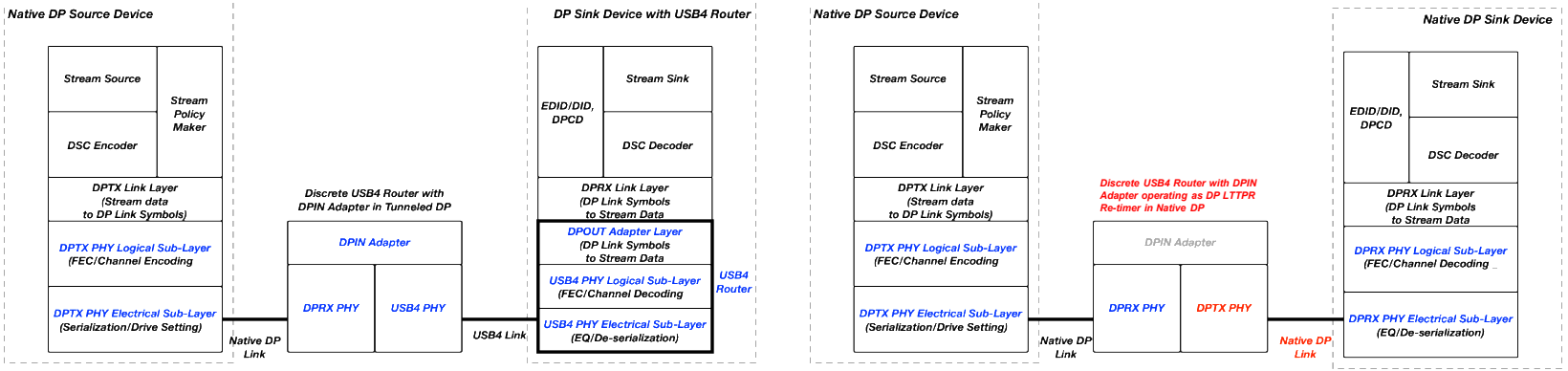
Native/Tunneled DP Dual Support Requirement

- A DP Source device with USB4 router is required to reconfigure itself as a Native DP Source device when connected to a Native DP-only Sink device
  - The same requirement exists for a DP Sink device with USB4 router



Native/Tunneled DP Dual Support Requirement

- A discrete USB4 router chip becomes an LTTPR re-timer in Native DP Transport



Native/Tunneled DP Dual Support Facilitation

- Goal
  - Facilitate an implementation that supports both Native DP Transport and Tunneled. DP Transport
- UHBR link rates added in DPv2.x Standard leverage USB4 PHY spec to the maximum extent feasible
  - 128b/132b channel coding
  - Link rates: UHBR10/UHBR20 = USB4Gen2/Gen3
    - UHBR13.5 unique to DP
  - TX FFE presets
  - Reference RX EQ
  - End-to-end channel loss budget assumptions

Helping USB4 Be More Efficient

- DP tunneling is typically the largest USB4 link bandwidth consumer, but USB4 carries non-DP tunneling traffic
  - E.g., PCIe tunneling, USB3 tunneling, Host Interface
- DSC mandate reduces the DP tunneling bandwidth consumption
  - E.g.: 67% reduction for 36 bpp uncompressed HDR to 12 bpp DSC compression
- Panel Replay also reduces DP tunneling bandwidth consumption when a static image is displayed on a monitor screen
  - 99%+ reduction when Panel Replay operation is activated
- DP BW Allocation Management avoids wasted BW allocation to DP tunneling
  - BW allocation based on the stream bandwidth (= pixel rate * pixel bit depth) instead of the maximum DP link payload bandwidth

DP Cable Logos

- Either a DP cable or a USB-C-to-DP cable (DP Alt Mode)
- DP8K
  - Up to 4-lane HBR3 without a DP cable identification mechanism
- DP54
  - Up to 4-lane UHBR13.5 with a DP cable identification mechanism
- DP80/DP80LL
  - Up to 4-lane UHBR20 with a DP cable identification mechanism

DP54 Cable

- Originally DP40 cable in DPv2.1 supporting up to 4-lane UHBR10
- Updated to DP54 supporting up to 4-lane UHBR13.5 in DPv2.1a
- Feasible of ~ 2-meter passive cable

DP80LL (Low Loss) Cable

- To be added in DPv2.1b targeted for the summer of 2025 release
- Lower loss than DP80 cable
  - DP80LL: -6.5 dB of loss at 10 GHz
  - DP80: -8.5 dB of loss at 10 GHz
- Feasible of ~ 3-meter LRD active cable
  - Leverages USB4 LRD active cable spec and compliance test methodology
- DP80 cable not deprecated, but LRD active cable required to meet DP80LL budget
  - DP80 passive cable length is limited to ~ 1 meter

	DP1.4x		DP2.x			
	DP1.4 (FEB 2016)	**DP1.4a (APR 2018)**	**DP2.0 (JUN 2019)**	**DP2.1 (OCT 2022)**	**DP2.1a (DEC 2023)**	**DP2.1b (Target: Summer 2025)**
Link Rates	HBR3, HBR2, HBR, and RBR (8.1/5.4/2.7/1.62 Gbps/lane, respectively). *HBR3 and HBR2 DPTX Voltage Swing and Pre-emphasis Monotonicity spec updated in DP1.4a*		**Addition UHBR rates** (UHBR20, UHBR13.5, UHBR10, having 3x/2x/1.5x of HBR3 link usable bandwidth). The maximum commonality with USB4 Gen2/Gen3 PHY: 128b/132b channel coding, RS(198,194) 8-bit symbol FEC, 16x TX FFE presets, RX reference CTLE/DFE			
Channel Coding and Pixel Data Mapping	8b/10b DP SST (Single Stream Transport) /MST (Multi-Stream Transport)		**Addition of 128b1/32b DP.** The common pixel data mapping to Link Layer symbols for both single- and multi-stream transport			
LTTPR	Added LTTPR (Link Training Tunable PHY Repeater) spec		Mandated LTTPR Non-Transparent Mode for UHBR rates	LTTPR Spec Clarification: (1) AUX transaction handling (2) 8b/10b DP LT in Non-LTTPR Mode and LLTPR Transparent Mode		
Link Training Fallback	Link rate reduction before lane count reduction (e.g., 4L HBR3 —> 2L HBR3 —> 4L HBR2)		For 128b/132b DP, fallback is to the next highest BW (e.g., 4L UHBR20 —> 4L UHBR13.5, instead of 2-lane UHBR20). **The next highest BW policy also allowed for 8b/10b DP.** **The repetition of DP Link Training with the same Link Config in case of a Link Training failure allowed up to twice starting from DP2.1a**			
Cables	Defined DP8K cable spec for HBR3 link rate		Detachable cables for UHBR rate limited to USB4 Gen2/Gen3 C-C cables	Addition of **DP40** and **DP80** DP/C-to-DP cables	DP40 cable replaced with **DP54** cable	Addition of **DP80LL** cable. Active DP cables required to meet DP80LL loss budget
FEC	Added RS(254, 250) 10-bit symbol FEC: Mandated for DSC bitstream, Optional for uncompressed		No change to 8b/10b DP FEC. **RS(198, 194), 8-bit symbol FEC always enabled for UlHBR rates**			
Power Management	AUX write of 02h to DPCD 00600h to prompt DPRX into DP Link Sleep State			Addition of **AUX-less ALPM**		
Video Fallback	640x480p60 (VGA Safe Mode)		1080p60 Video Fallback (enumerated at DPCD 00020h)			
DSC Transport	Added as optional		**Made DSC transport support mandatory for DP devices with UHBR-rate support.** Added **DSC pass-through for DP Branch device** (e.g., DP-to-HDMI PCON) added			
Panel Replay	N/A		**Added as optional for reductions of (1) active power and (2) DP tunneling BW**	**Added "Main Link Off" Panel Replay** for further power reduction leveraging AUX_less ALPM Specified Panel Replay concurrent with Adaptive-Sync operation		
Audio Support	(1) Added Audio Stream SDP as mandatory for DPRX both in single- and multi-stream transport and (2) extended supported audio stream formats to cover up to 32-ch 3D LPCM audio starting from DP1.4					
SDP	Added VSC_EXT chain-able SDP	Added Adaptive-Sync SDP		Expanded Adaptive-Sync SDP payload for an improved Adaptive-Sync (known as VRR in HDMI terminology) operation		
Protocol Converter (PCON) Support	HDMI TMDS Mode support only. Autonomous Mode only; no Source-controlled Mode)		**Added support for HDMI FRL Mode (from DP2.0) and VRR Mode (from DP2.1a). Added Source-controlled Mode**		**Refined Autonomous Mode**	**Updated Autonomous Mode as Regulated Autonomous Mode**
DPRX HBLANK Expansion/Reduction	Added DPRX HBLANK Expansion mainly to support 8K60 HDMI2.1 TV support (8K4K60 (VIC197) with 12bpp DSC requires reduced HBLANK to fit in 4-lane HBR3)			Added DPRX HBLANK Reduction mainly to increase Audio Stream SDP transport BW in UHBR rates in conjunction with DSC bitstream transport		
DP Tunneling	DP Tunneling DPCD registers for proprietary tunneling of DP Link Symbols (e.g., Thunderbolt3)			DP Tunneling DPCD registers for DP tunneling over USB4. **Added (1) DP tunneling BW allocation management and (2) Panel Replay optimization**		

Standard Spec and CTS (Compliance Test Spec)

- A standard specification encourages compliance through a logo certification program
  - A logo certification requires for a product to pass compliance and interop tests
  - Compliance test procedures described in CTS (Compliance Test Spec)
- However, the reality is…
  - A CTS release ends up lagging a standard spec release
  - A CTS keeps evolving to correct shortcomings and improve coverage
    - VESA uses SCR (Spec Change Request)/Errata process to add interim spec updates
    - Interop tests augment compliance test coverage
    - Neither compliance nor interop test reliably catches intermittent failures, but they increase the likelihood of interop of the certified products in the field

DP Standard and DP CTS

- DP2.1x CTS adds test coverages for UHBR-rate, Panel Replay, LTTPR, DP tunneling, etc.
- However, even those DP products that do not support any new feature in DP2.x need to be compliance tested with DP2.1x CTS with the latest Errata
  - It has added testing of policy updates for interop improvement
- Those compliance test failures caused by inadequacy of compliance test spec and/or implementation of a test equipment may/will be waived

Post DP2.1b: Next DP Link Rate Increase?

- USB4v2 added USB4 Gen4 link rate of 40 Gbps/lane
  - Doubled USB4 Gen3 link rate of 20 Gbps/lane
- Currently, no DP link rate increase beyond UHBR20 considered
  - No clear use case merit beyond 80 Gbps of 4-lane UHBR20 identified

DP-Derivative Standards: eDP Standard

- eDP2.0 released in September 2024
- More convergence with DP Standard
  - Making a reference to DP Standard
    - 128b/132b DP (new in eDP2.0)
    - Panel Replay
    - AUX-less ALPM (Advanced Link Power Management)

DP-Derivative Standards: DP Alt Mode Standard

- DP Alt Mode v2.1a released in August 2024, with v2.1b for additional clarification on the way
- Main update = Cable identification flow clarification for interop improvement

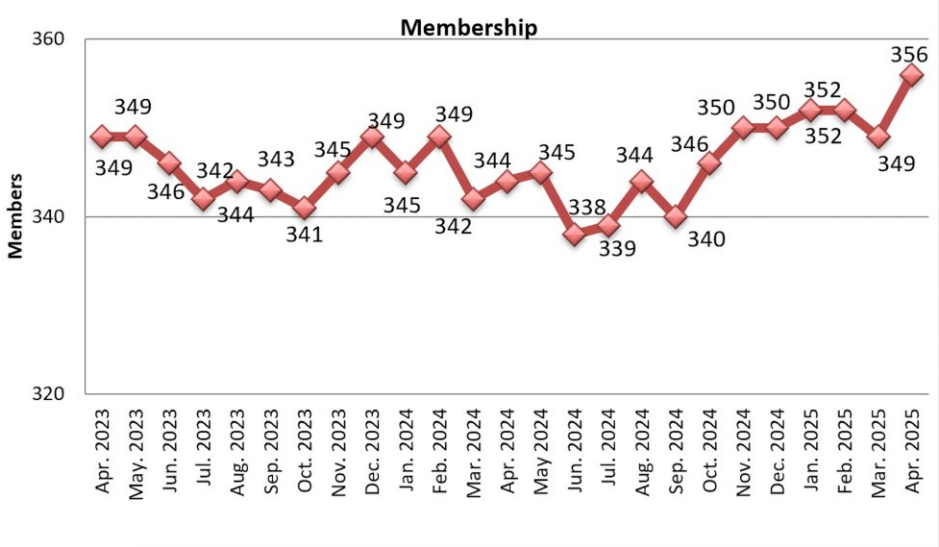
DP-Derivative Standards:
DP Automotive Extension Services

- DP Automotive Extension Services v1.0 released in December 2023
- Safety and security extension for DP use case for automotive
- Current focus is on the compliance test enablement

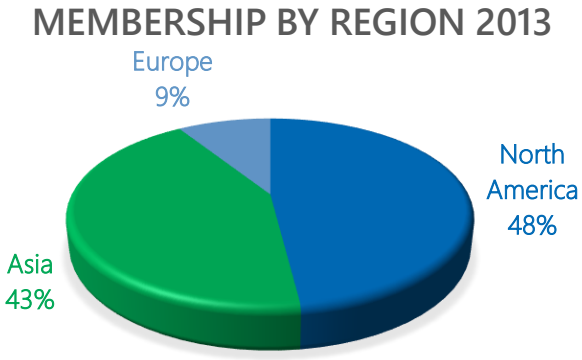
VESA Compliance Program

About VESA

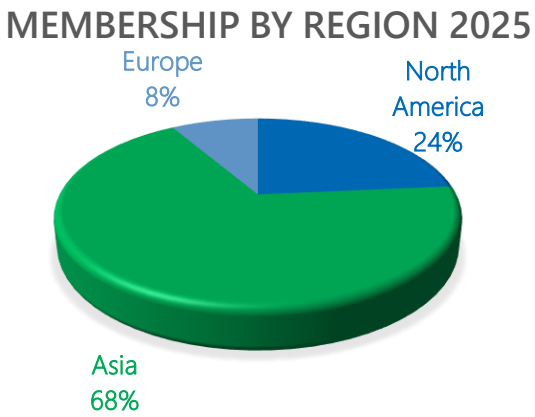
- A growing global industry alliance with over 350 members in 2025. Strong growth in membership over 10 years.
- Mission to develop, promote and support ecosystem of vendors and certified interoperable products for the electronics industry.
- *Develops OPEN standards, contribution is open to all companies at all stages of development*



VESA Membership Growth



Changes from 2013:
Asia + 25%



Many Aspects of DisplayPort Technology

Display Interfaces

- DisplayPort
- Embedded DisplayPort
- DisplayPort Alt Mode (Native DisplayPort over USB-C connector)
- DisplayPort Tunneling (USB4 and Thunderbolt)
- Automotive Extensions Services (DP AE specification) – New Release

Display Data Compression

- Display Stream Compression (DSC)
- VESA Display Codec for Mobile (VDC-M)

Display Metrology

- Standardized Display Performance Measurement
- DisplayHDR Certification (High Dynamic Range)
- ClearMR Certification
- AdaptiveSync Display Certification

Display Capability Parameters

- DisplayID
- Extended Display Identification Data (EDID)
- Multi-Display Interface (MST)

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VESA Local Asian Support Capability

- VESA continues to provide local support to Asia to address growing regional membership needs
- China (Mainland) and Taiwan are the fastest growing areas for VESA's membership.
- **Kellen** is VESA's Representative in Asia
- This partnership provide members with a communication option in their native language. Kellen handles membership related activities including, new membership requests, renewals, event support and translation of VESA member messaging, etc.
- AsiaVESA@kellencompany.com or at +86 10 6580 0670

DisplayPort Market Penetration

- DisplayPort adoption continues to grow in 2025
- DisplayPort and DisplayPort Alternate Mode over USB-C
  - The common monitor interface for personal computers
  - Supported on the USB-C interfaces
  - Mandated for USB4 and Thunderbolt
  - Automotive integration with DP AE specification
  - Mobile phones with USB-C
- Embedded DisplayPort (eDP)
  - ~95% penetration in notebook PCs, used in many high-end tablets and now automotive

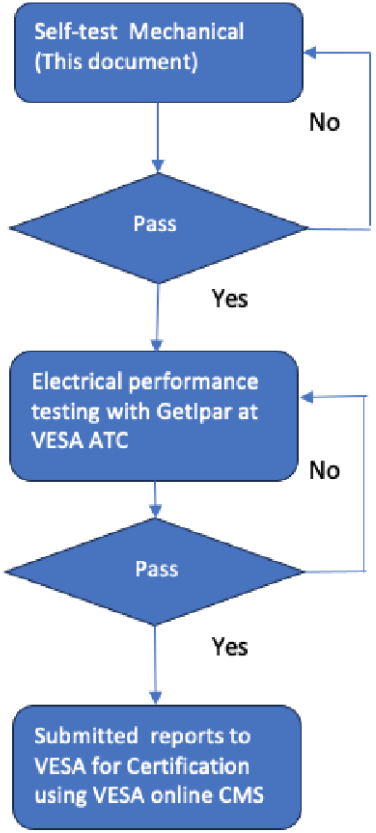
Compliance Test Specification Updates

VESA has updated base specification and all CTS documents in past two years

- DP 2.1a Spec update – released 12/2023
- DP 2.1 PHY CTS v1.0 – released 6/23
- DP 2.1 Link CTS v1.0 – released 11/2023
- Enhanced DP Connector Self-Test v2.1 – 8/2024
- DP Alt Mode CTS v2.1 – 8/2024
- Embedded DP (eDP) – 9/2024

Enhanced Connectors

- UHBR rates = the need for high performance DP connectors
- VESA created specification and test requirements for Enhanced DP connectors (fsDP and mDP)
- This includes both right angle and vertical mount connectors



DP54 and DP80 Cable Specification and Certification program

- Work on Enhanced DP cable and connector specifications and test requirements started in 2021 to ensure high performance connectors and cables would be available for products supporting UHBR rates
- DP54 and DP80 Certified cables provide added assurance of proper operation at the highest link rates (UHBR10, UHBR13.5 and UHBR20 Gbps)
- Over 150 Enhanced DP cables and connectors have been certified since launch of the Enhanced DP cable and connector certification programs
- DP40 cable performance tier replaced with DP54 in 2024
- DP54 cables are required to support UHBR10 and UHBR13.5 link rates, enabling longer cables for sources and sinks that implement 13.5Gbps as highest link rate

Product certifications* 2022/2023/2024

Products	2022	2023	2024
DP Sources	141	99	60
DP Sinks	339	277	320
DP Cables	42	59	56
DisplayHDR	388	397	369
ClearMR	14	45	30
AdaptiveSync	25	80	48

*Note: numbers are base model certs not including family models

VESA PlugTest Events

- Provide significant value to member companies, particularly as new capabilities and products are deployed.
- Demonstrate and improve Traditional Interoperability
- Test Native DP and DP Alt Mode over USB Type-C™ products
  - UHBR rates, DSC, FEC, DisplayHDR and other new capabilities
  - Verify Test Equipment Correlation
- VESA hosted two successful PlugTests in 2024 (Taiwan and US)
- VESA will host two PlugTests in 2025

Dates/Locations:

Done: October 14-18, 2024 (Taipei, Taiwan) – Illume Hotel Taipei

Done: May 19- 22, 2025 (South San Francisco, USA) – Embassy Suites

Planning: October 13-17, (Taipei, Taiwan)

DP2.1 PR and ALPM Implementation and Testing Challenges

Marco Denicolai
Unigraf Oy
May 23, 2025

Disclaimer

All opinions, judgments, recommendations, etc. here presented are the opinions of the presenter and do not necessarily reflect the opinions of VESA

Agenda

- Saving power with Panel Replay (PR)
- Saving power with Advanced Link Power Management (ALPM)
- Interaction with FEC, MST and HDCP

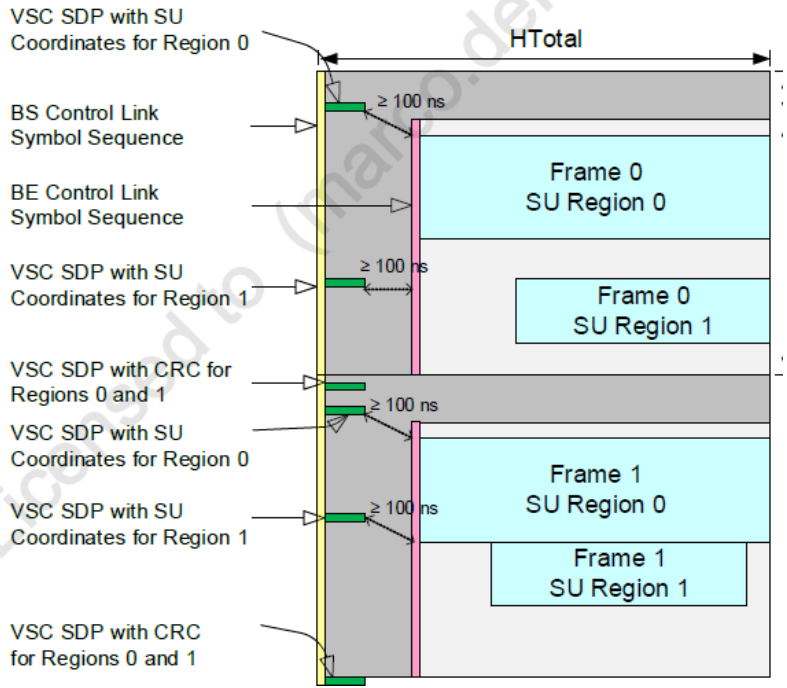
The Devil is in the details…

DisplayPort system-level power conservation

- Optional Panel Replay (PR) can be enabled to turn the Main Link off when no data is being transferred and save power.
- When PR is in Active state, the Sink will use the image captured in its Remote Frame Buffer (RFB) to refresh the display.
- During PR Active state, the Source can either continue to transmit a frame-rate-governed video timing (discarded by the Sink) or, optionally, turn the Main Link off.
- Optional Main Link power on/off management uses Advanced Link Power Management (ALPM) in AUX-less mode.

Panel Replay overview

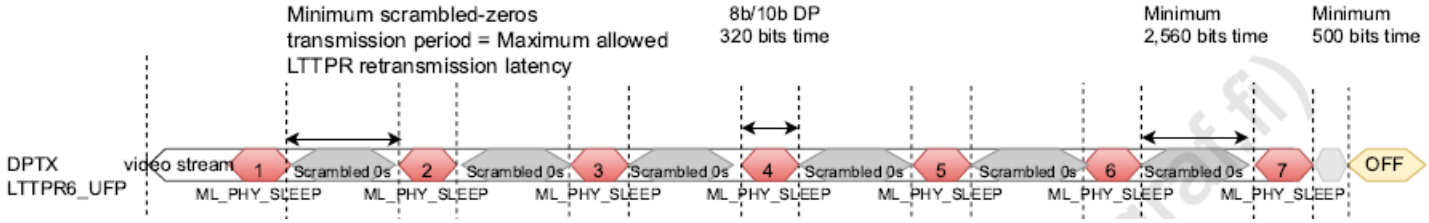
- Transitions between Live Frame mode and PR Active state happen using VSC SDPs.
- The Source can transmit a Full Frame update, or one or more smaller Selective Update (SU) Regions, each starting at their respective video scan line position.
- SU Region coordinates and dimensions are defined using a VSC SDP transmitted at least 100ns before the start of the SU region.
- After a SU Region, the Source may optionally transmit a VSC SDP containing the CRC accumulated for all of the SU Regions of the frame.
- Optional SU Region Early Transport support: the first SU Region is transmitted starting from the first active video scan line instead of its real position. The following regions are transmitted preserving the relative distance between them.



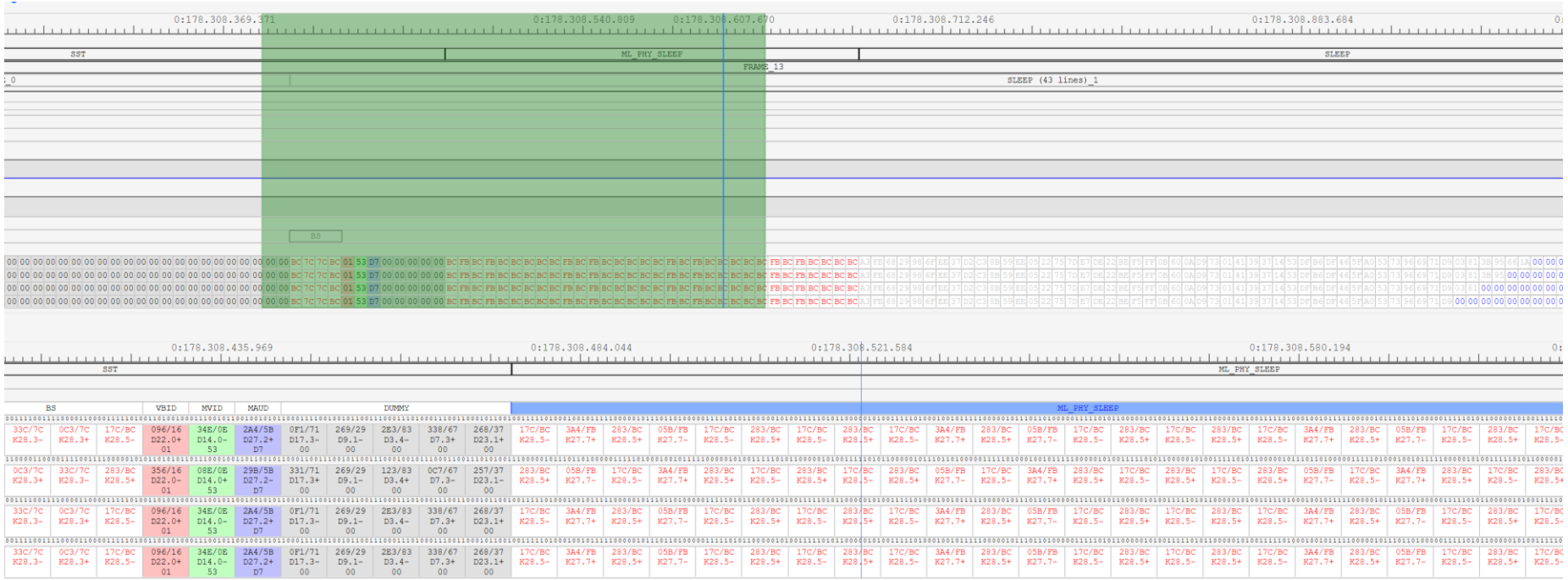
ALPM: Main Link Power-off

- The Source uses the ML_PHY_SLEEP sequence followed by scrambled zeroes to signal LTTPRs and Sink that the Main Link will be powered-off.
- The ML_PHY_SLEEP sequence consists of:
  - 8b/10b: a sequence of [K28.5, K27.7, K28.5, K27.7, K28.5, K28.5, K28.5, K28.5], with correct disparity
  - 128b-132b: a special 129-bit supersymbol [CDI=1 + 89898989h, 89898989h, 89898989h, 89898989h]. CDI is XORed according to standard rules, then precoded
- The Source transmits four consecutive ML_PHY_SLEEP sequences followed by scrambled 0s:
  - Once for each connected LTTPR
  - Once for the Sink

- The ML_PHY_SLEEP sequence must not overwrite BS+VBID, MSA, SDP data or FEC control link symbols.
- The Sink must look for two consecutive ML_PHY_SLEEP sequences and allow for max 4 symbol errors within them.
- Mandatory minimum ALW_SLEEP time after power-off sequence: 15us



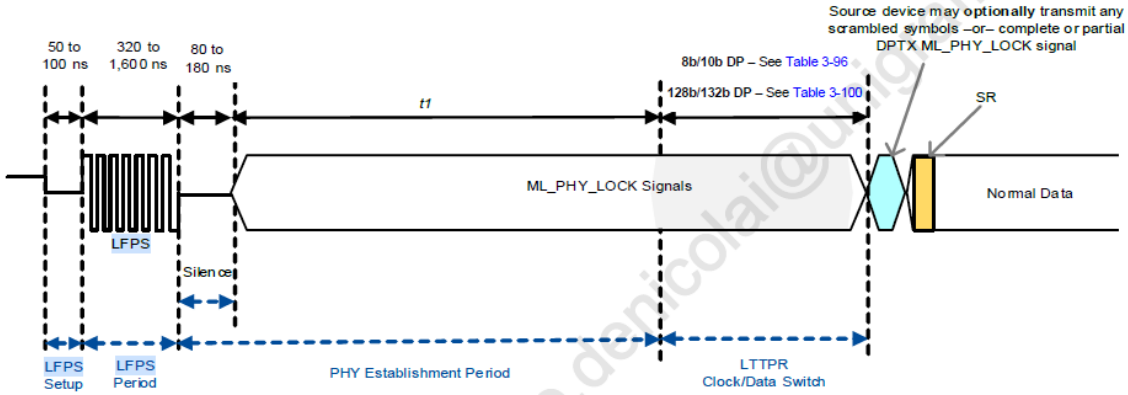
ALPM: Main Link Power-off (cont.)



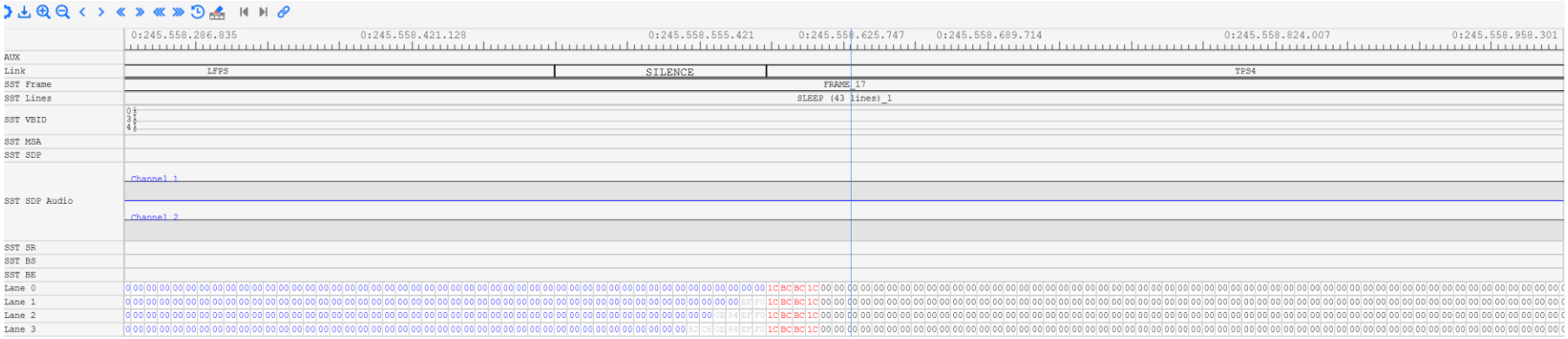
ALPM: Main Link Power-on (aka “wake”)

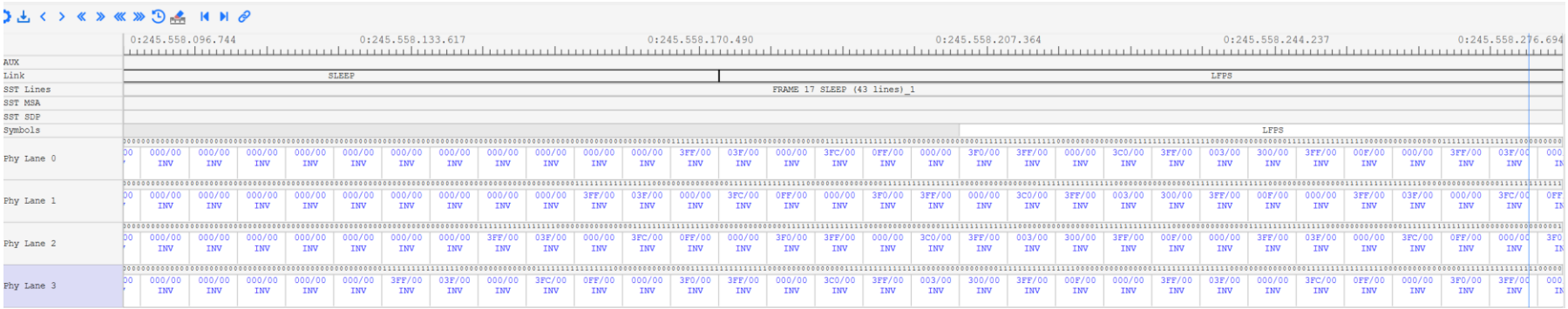
- The Source uses the ML_PHY_WAKE sequence to signal LTTPRs and Sink that the Main Link has been powered back on.
- The ML_PHY_WAKE sequence is composed by LFPS period (square wave at 12.5…50 MHz, at least 16 pulses, no more than 1.6us long) followed by a silence period and ML_PHY_LOCK pattern.
- ML_PHY_LOCK pattern:
  - 8b/10b – same as TPS4
  - 128b/132b – same as 128b_132b_TPS2 but with reduced intervals between LT_SCRAMBLER_RESET symbols (4 logical frames instead of 16)

- LFPS can have different common mode voltage amplitude than the ML data. Switch to ML common mode voltage is performed during the silence period
- The shortest duration of ML_PHY_LOCK is 50us. The Sink must complete EQ adaptation within this time. This is significantly shorter than usual link training



ALPM: Main Link Power-on (cont.)

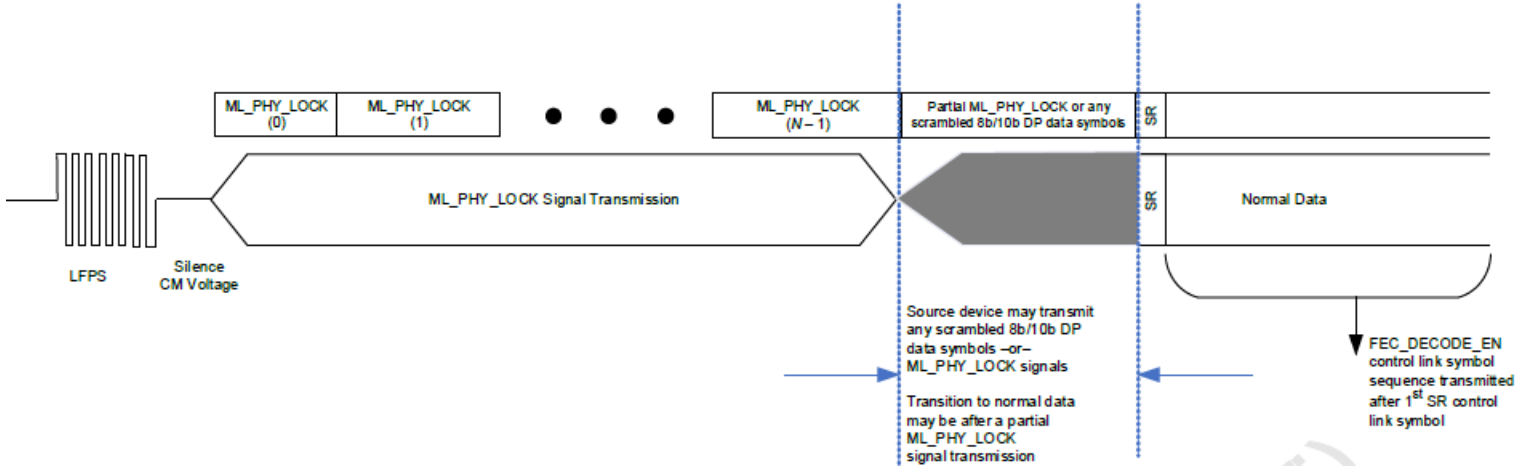




8b/10b FEC support

- In 8b/10b mode, FEC is not mandatory for ALPM. However, it is mandatory for Panel Replay.
- FEC block structure is maintained during the power-off sequence
- On the Sink side, FEC is considered disabled after power-off. Source must re-enable it by transmitting the FEC_DECODE_EN sequence after ML_PHY_LOCK pattern.

- The FEC block containing the final part of power-off sequence's scrambled 0s may be left incomplete. Sink must handle this situation correctly.
- The Sink cannot disable its FEC Decoder right when ML_PHY_SLEEP is detected but needs to wait for the last FEC block data to be decoded, since it could contain e.g. the tale of the last video frame transmitted.

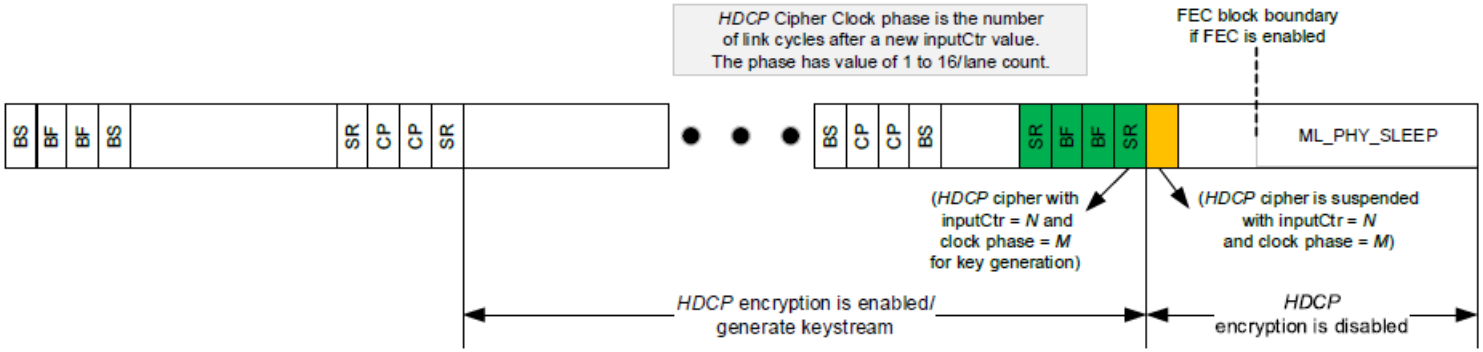


MST support

- During power-off sequence, ML_PHY_SLEEP is transmitted using all time slots.
- Source must be careful not to overwrite important data such as BS and VBID with ML_PHY_SLEEP in allocated slots.
- After power-on sequence, MST framing is started after the ML_PHY_LOCK pattern with an MST SR symbol.

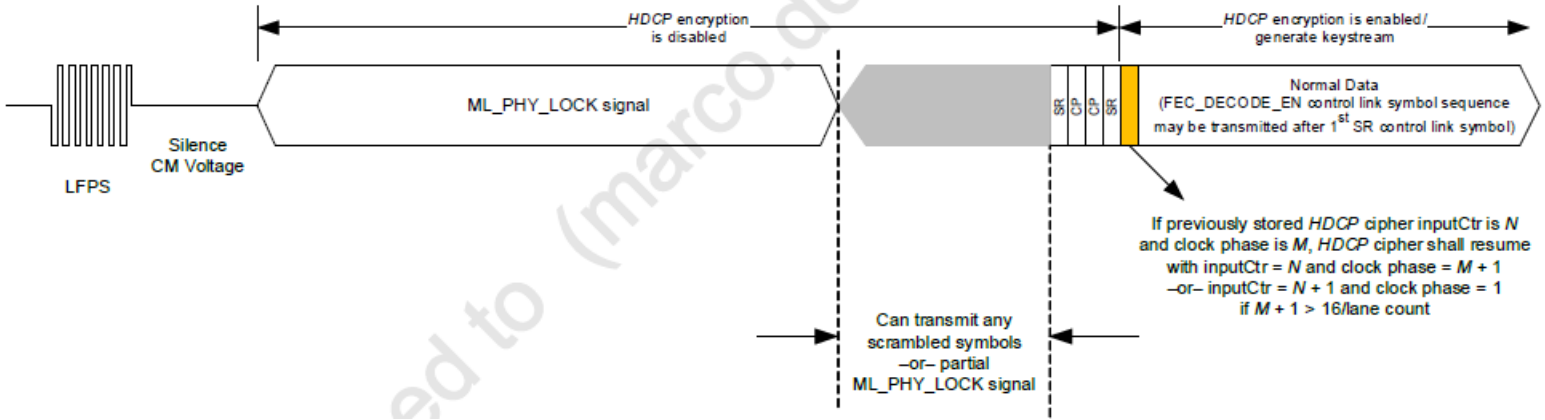
HDCP support

- Only HDCP r2.3 (or higher) is supported with AUX-less ALPM.
- HDCP is suspended before ML_PHY_SLEEP, HDCP cypher is frozen.



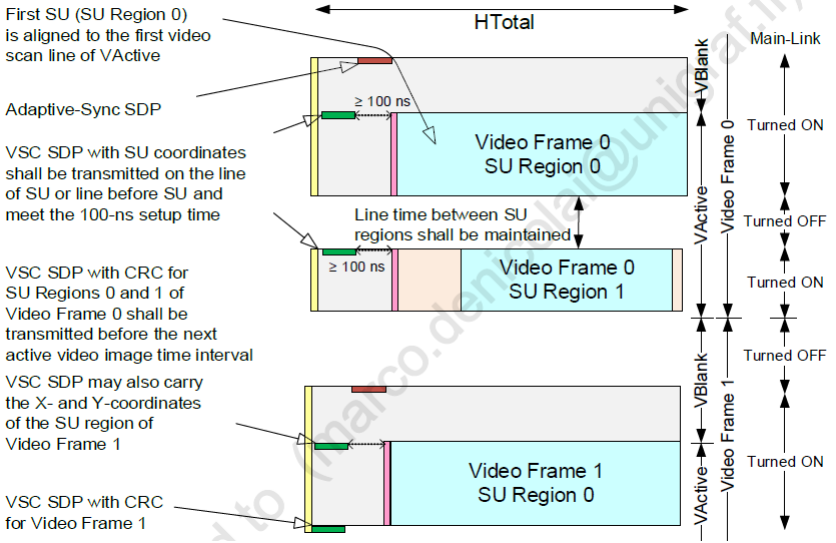
HDCP support (cont.)

- After power-on, HDCP is resumed and decryption continues from the previously frozen state, without the need for re-authentication.
- For 8b/10b SST and 128b/132b, encryption suspend and resume procedure is straightforward. For 8b/10b MST it is more complicated.



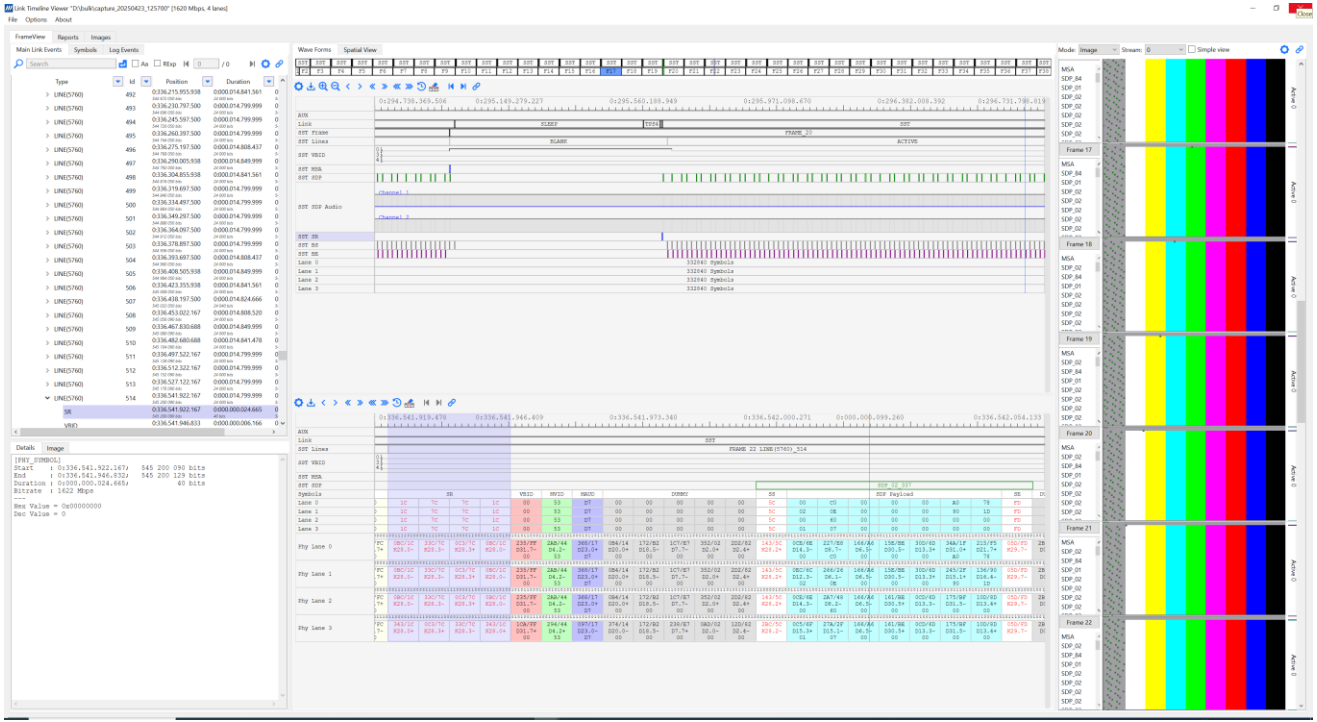
Panel Replay with ALPM

- When PR is in Active state, the Main Link can stay powered (option 1-A) or can be powered-off (option 1-C) using ALPM
- When ALPM is used, Sink and Source video timing synchronization is maintained using Adaptive-Sync SDPs, for each frame and at the same position.
- When ALPM is used, Early Transport is mandatory.
- Power-off is possible between SU regions, but the line interval still must be maintained.



DP Link Analyzer

A Unigraf tool for capturing Main-link Data Events and AUX Transactions. Within each frame, users can have a deep view of the events and metadata that occurs in each line. Measure distances in nanoseconds and symbol size to identify the length of problems in between events. Observe descrambled and scrambled symbols in hexadecimal format in each of the active lanes.



DP2.1 Compliance Tests Update Phase 6

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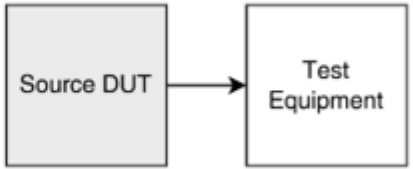
Company : Teledyne LeCroy

Date: 05/23/2025 (23-May-2025)

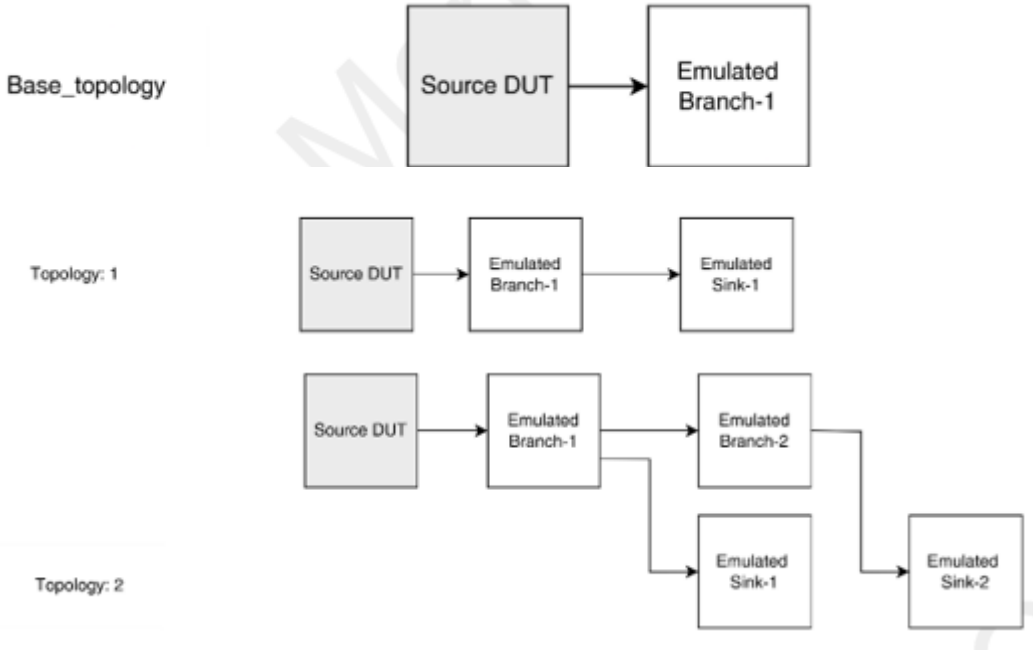
VESA Approved DP2.1 Compliance Tests Coverage:

- MST Source device tests
  - Topology test setup
  - New CDF for MST
  - Approved Tests (6.1.1.1 to 6.1.1.22)

Source Setup -1

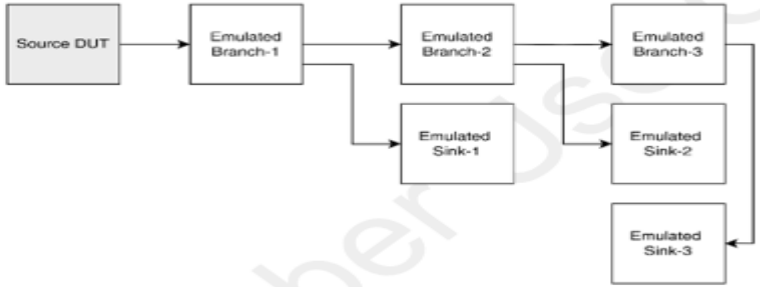


MST Source CTS topology (test setup for emulated Composite Sink)

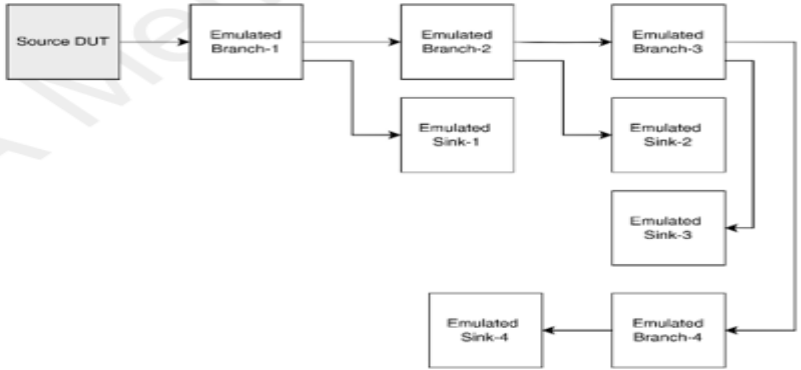


MST Source CTS topology (test setup for emulated Composite Sink)

Topology: 3

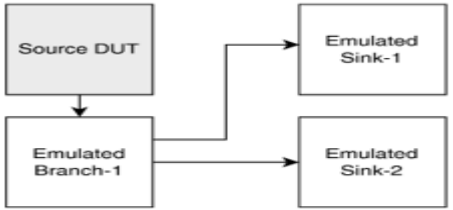


Topology: 4

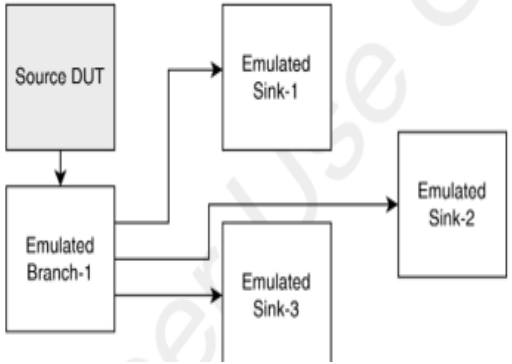


MST Source CTS topology (test setup for emulated MST Hub and sinks)

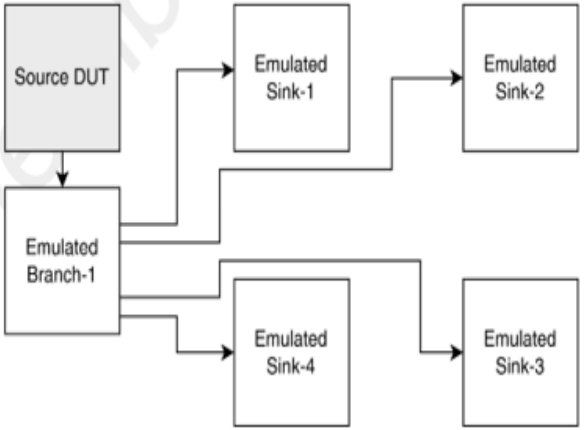
Topology: 5



Topology: 6



Topology: 7



MST Source CTS new CDF entries

S.No	CDF Entry	Default Value
1	MST_TRANSMISSION	Yes
2	MST_MAX_STREAM_COUNT	4
3	MST_UP_REQUEST_SUPPORTED	Yes
4	MST_RSN_REQUEST_SUPPORTED	No
5	MST_MAX_DAISY_CHAIN_SINK_SUPPORTED	4
6	MST_POWER_UP_DOWN_PHY_SUPPORTED	Yes

MST Source CTS

Tests	Objective	Main Points
6.1.1.1	Source DUT reads the MST Capability and Sets the MSTM of MST Branch	Verify that DUT programs DPCD 00111h MSTM_CTRL 3-bits correctly (MST_EN, UP_REQ_EN and UPSTREAM_IS_SRC)
6.1.1.2	Source DUT sends Link Address Request after detecting an MST branch	Verify that DUT requests LINK_ADDRESS for topology discovery [Repeat for Topology setup 1,2,3,4]
6.1.1.3	Source DUT sends Enum Path resources for each of the detected Sink	Verify that DUT requests ENUM_PATH_RESOURCES for each sink in topology [Repeat for Topology setup 1,2,3,4,5,6,7]. Validate resource allocation for each sink and video present.
6.1.1.4	Source DUT Initiates and completes Allocate Payload sequence for each of the detected Sink	Verify that DUT programs DPCD 001c0h to 001c2h and verifies with DPCD 002c0h. [Repeat for Topology setup 1,2,3,4,5,6,7]. The Allocate payload also take into account for FEC overhead.
6.1.1.5	Source DUT Generates multiple video streams at once, matching with the payload allocation set by it	Verify that DUT sends Video for multiple Monitors at the same time within 10 sec. [Repeat for Topology setup 1,2,3,4,5,6,7].
6.1.1.6	Source DUT Reacts appropriately to CSN request upon device removal : Remove sink from daisy chain	Verify that DUT does handle CSN update and clear payload table for removed sink. [with sink removals Topology setup switches from 4 to 3 to 2 finally 1]
6.1.1.7	*Source DUT Reacts appropriately to CSN request upon device removal : Remove branch from daisy chain*	Verify that DUT does handle CSN update and clear payload table for removed branch [with sink removals Topology setup switches from 4 to 3 to 2 finally 1]
6.1.1.8	*Source DUT Reacts appropriately to CSN request upon device removal : Remove sink connected to single branch*	Verify that DUT does handle CSN update and clear payload table for removed sink [with sink removals Topology setup switches from 7 to 6 to 5 to 1 and finally Base topology]
6.1.1.9	*Source DUT Reacts appropriately to CSN request upon device connection : Sink connected to a single branch*	Verify that DUT does handle CSN update and add payload table for added sink [with sink addition Topology setup switches from Base topology to 1 to 5 to 6 and finally 7]
6.1.1.10	*Source DUT Reacts appropriately to CSN request upon device connection : Composite Sink (Daisy Chain Capable Sink) Setup*	Verify that DUT does handle CSN update and add payload table for added Composite-sink [with addition Topology setup switches from Base topology to 1 to 2 to 3 and finally 4]
6.1.1.11	*Source DUT Reacts appropriately to RSN request*	Verify that DUT handle RSN up request and update Allocate Payload [Repeat for Topology setup 5,6,7]. RSN update for BW change in emulated topology, validates, clear payload, followed by config of PBN or just update payload table.

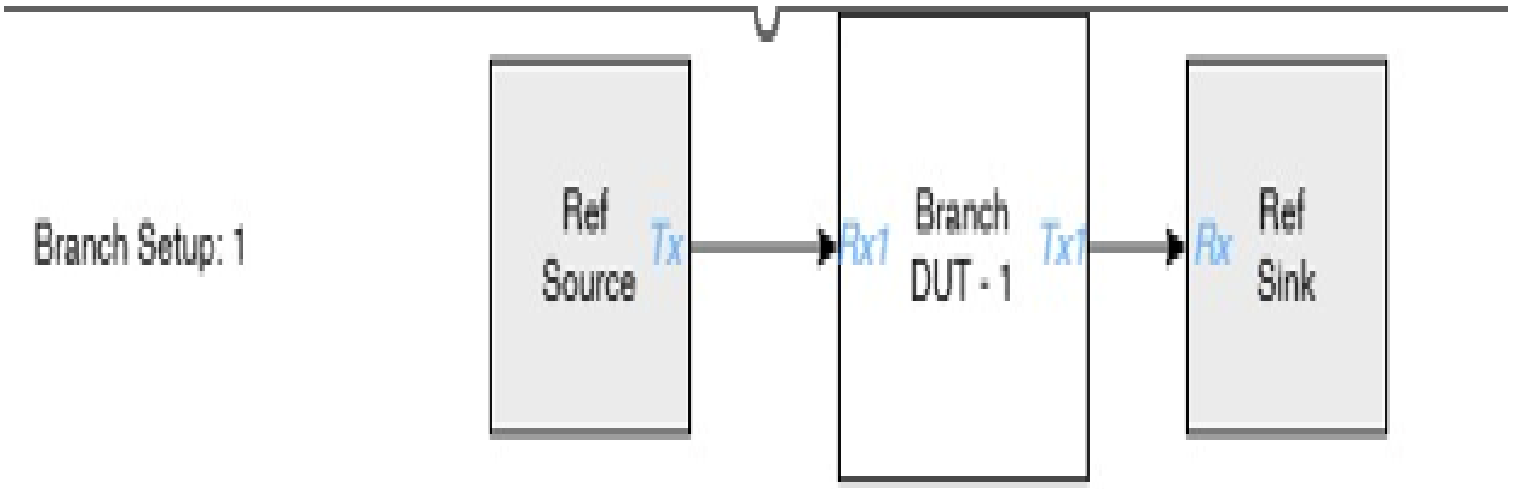
MST Source CTS

Tests	Objective	Main Points
6.1.1.12	Source DUT *Ability to generate multiple video streams: Combination of DSC and Non-DSC images*	Verify that DUT can generate a combination of DSC and non-DSC image at the same time. [Repeat for Topology setup 2,3,4]
6.1.1.13	Source DUT *reads the EDID, Native DispID and DPCD of each of the detected sinks*	Verify that DUT can read connected sink DPCD, EDID and Native DisplayId using sideband msg [Repeat for Topology setup 5,6,7]
6.1.1.14	Source DUT *reads appropriate DSC and FEC capabilities*	Verify that DUT read FEC and DSC capabilities of all connected sink for Topology 1.
6.1.1.15	Source DUT handles unknown up requests	Verify that DUT gracefully handles unknown request types and returns a NACK reply while remaining stable.
6.1.1.16	Source DUT handles NACK down reply	Verify that DUT gracefully handles NACK down reply for various down requests sink for Topology 1.
6.1.1.17	Source DUT handles incorrect down replies	Verify that DUT can handle incorrect, inaccurate or incomplete down reply sideband messages gracefully for Topology 1.
6.1.1.18	*Source DUT* handles branch device down reply timeout	Verify that DUT ability to wait for 4 seconds for a down reply before timing out and retrying for Topology 1.
6.1.1.19	*Source DUT* MST to SST transition	Verify that DUT ability to transition from an MST stream to an SST only stream for Topology 1.
6.1.1.20	*Source DUT* SST to MST transition	Verify that DUT ability to transition from an SST only stream to an MST stream upon detecting an MST branch device for Topology 1
6.1.1.21	*Source* DUT's ability to set devices in low power mode and back in normal mode	Verify that DUT ability to drive all the connected devices into a Power saving (low power) mode and bring them all back to a normal mode for Topology 1
6.1.1.22	*Source* DUT's ability to read the GUID and set if 0	Verify that DUT ability to read the GUID of each of the connected devices and set a unique value if it is reported as 0 [Repeat for Topology setup 1,2,3,4,5,6,7].

MST Device CTS new CDF entries

S.No	CDF Entry	Default Value
1	BRANCH_DUT_NO_OF_DFP_DPPORT	Range 1-4
2	BRANCH_DUT_UFP_PORT_NUM_CONNECTED_TO_TE	Range 1-16
3	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_TE	Range 1-16
4	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK1	Range 1-16
5	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK2	Range 1-16
6	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK3	Range 1-16
7	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK4	Range 1-16
8	BRANCH_DUT_CSN_DFP_BROADCAST	False

MST Branch Setup1

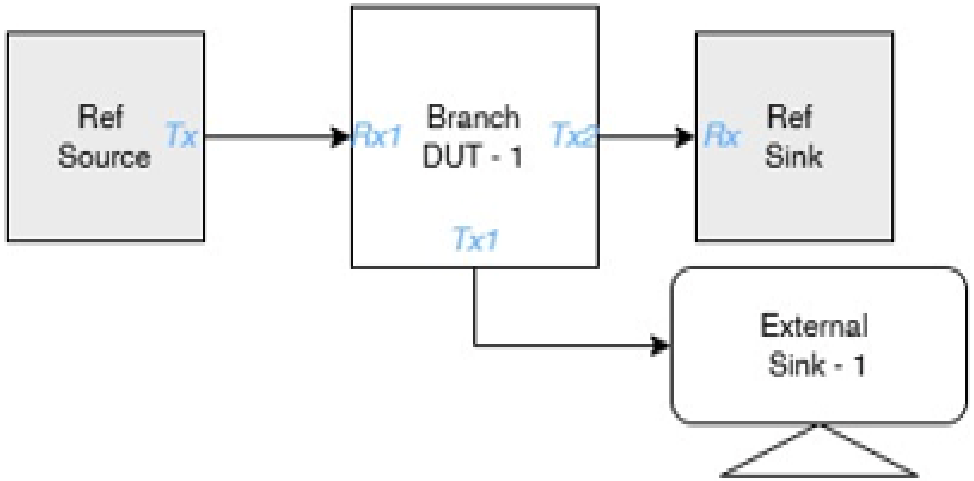


MST Branch Setup1 Tests

Tests	Objective	Main Points
6.2.1.1	Branch DUT has appropriate MST capabilities set	Verify that the Branch DUT sets the correct MST capabilities (and DFP Port) in its DPCD registers
6.2.1.2	Branch DUT responds correctly to the Link Address Request	Verify that the Branch DUT replies with an ACK to LINK_ADDRESS down request with the values as per the CDF, that is, the number of ports, port connected and as per the test setup on Rx by the Test equipment. Reference sink will honor CDF max limit on emulating various topologies.
6.2.1.3	Branch DUT forwards down requests accurately, and forwards down replies accurately	Verify that Branch DUT is able to forward the down requests after modifying the sideband headers. And able to forward the down replies after modifying the sideband headers. Focus on LCT,LCR, clear payload table, correctness of sideband msg update.
6.2.1.4	Branch DUT forwards up requests accurately, and forwards up replies accurately	Verify that the Branch DUT is able to forward the up requests after modifying the sideband headers. Similarly, also verify that the Branch DUT is able to forward the up replies after modifying the sideband headers. Focus on LCT,LCR, correctness of sideband msg update.
6.2.1.5	Branch DUT responds correctly to Enum Path resources	Verify that the Branch DUT replies with an ACK to ENUM_PATH_RESOURSES down request with the correct PBN value as per the lane count and link rate of the corresponding DP link. This validation make sure PBN update take account of FEC overhead addition and removal done correctly, between HBR and UHBR, FEC enable, FEC disable.
6.2.1.6	Branch DUT responds correctly to Query Payload	After allocation of resources, verify that the Branch DUT responds to QUERY_PAYLOAD down request with the correct values and ACK to Allocate Payload msg.
6.2.1.7	Branch DUT reads and responds to Remote_DPCD_read accurately	Verify that the branch DUT reads the DPCD registers on a DFP via native AUX transactions upon REMOTE_DPCD_READ down request and replies with an ACK with the correct values
6.2.1.8	Branch DUT writes and responds to Remote_DPCD_write accurately	Verify that the branch DUT writes to the DPCD registers on a DFP via native AUX transactions upon REMOTE_DPCD_WRITE down request and replies with an ACK
6.2.1.9	Branch DUT ability to forward correct video stream in DSC and Non-DSC cases	Verify branch DUT forwards DSC and Non-DSC images at the same time.
6.2.1.10	Branch DUT Correctly calculates and allocates timeslots	Verify the Branch DUT's ability to correctly allocate timeslots for all the VCs on each of the DFPs
6.2.1.11	Branch DUT's ability to respond to REMOTE_DPCD_READ and REMOTE_DPCD_WRITE	After sending a down request of REMOTE_DPCD_READ and REMOTE_DPCD_WRITE verify the Branch DUT's ability to do a native AUX read and write respectively
6.2.1.12	Branch DUT's ability to respond to REMOTE_I2C_READ	After sending a down request of REMOTE_I2C_READ and verify the Branch DUT's ability to do a I2C over AUX

MST Branch Setup2

Branch Setup: 2

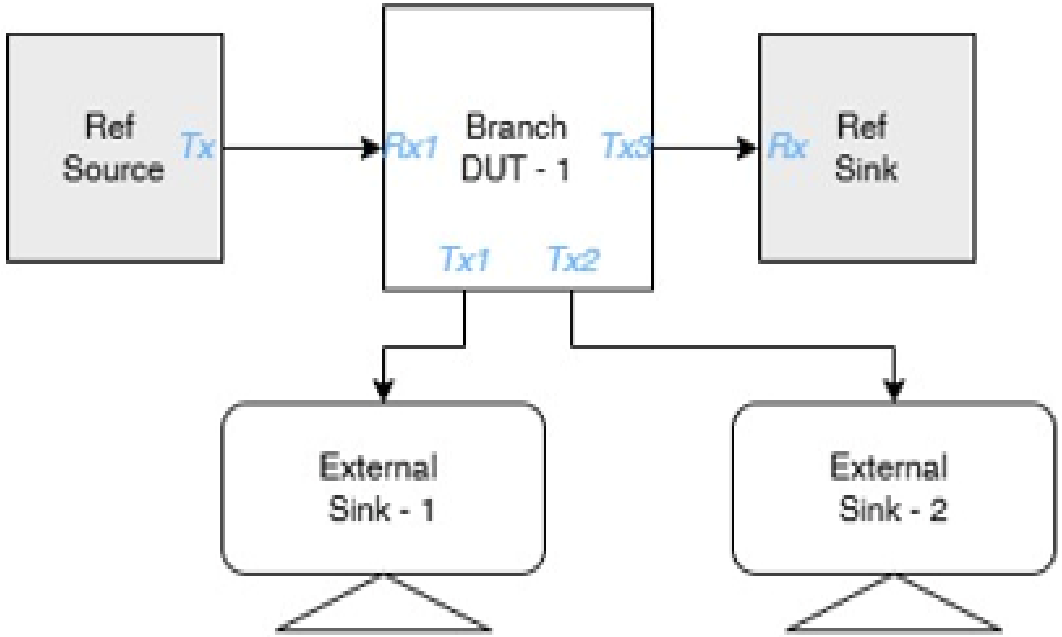


MST Branch Setup2 Tests

Tests	Objective	Main Points
6.2.2.1	Branch DUT responds correctly to the Link Address Request	Verify that the Branch DUT replies with an ACK to LINK_ADDRESS down request with the values as per the CDF, that is, the number of ports, port connected and as per the test setup on Rx by the Test equipment. Reference sink will honor CDF max limit on emulating various topologies.
6.2.2.2	Branch DUT responds Correctly calculates and allocates timeslots	Verify the Branch DUT's ability to correctly allocate timeslots for all the VCs on each of the DFPs
6.2.2.3	Branch DUT's Ability to send through the video stream accurately to an emulated Branch device on its DFP	Verify the Branch DUT's ability to forward video streams when multiple VCs are allocated to a single downstream port
6.2.2.4	Branch DUT's Ability to set up Low power mode on reference Sink appropriately	Verify the Branch DUT's ability to set a DFP device in low power on POWER_DOWN_PHY down request
6.2.2.5	Branch DUT's Ability to come out of low power mode.	Verify the Branch DUT's ability to come out of low power mode upon POWER_UP_PHY down request
6.2.2.6	Branch DUT Generates CSN up request upon sink device disconnection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a sink device on one of the DFPs
6.2.2.7	Generates CSN up request upon sink device connection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon connection of a sink device on one of the DFPs
6.2.2.8	Generates CSN up request upon branch device disconnection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a branch device on one of the DFPs
6.2.2.9	Generates CSN up request upon branch device connection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon connection of a branch device on one of the DFPs
6.2.2.10	Generates CSN down request upon Upstream device disconnection	When an upstream device is disconnected, verify that Branch DUT issues a CONNECTION_STATUS_NOTIFY down request broadcast

MST Branch Setup3

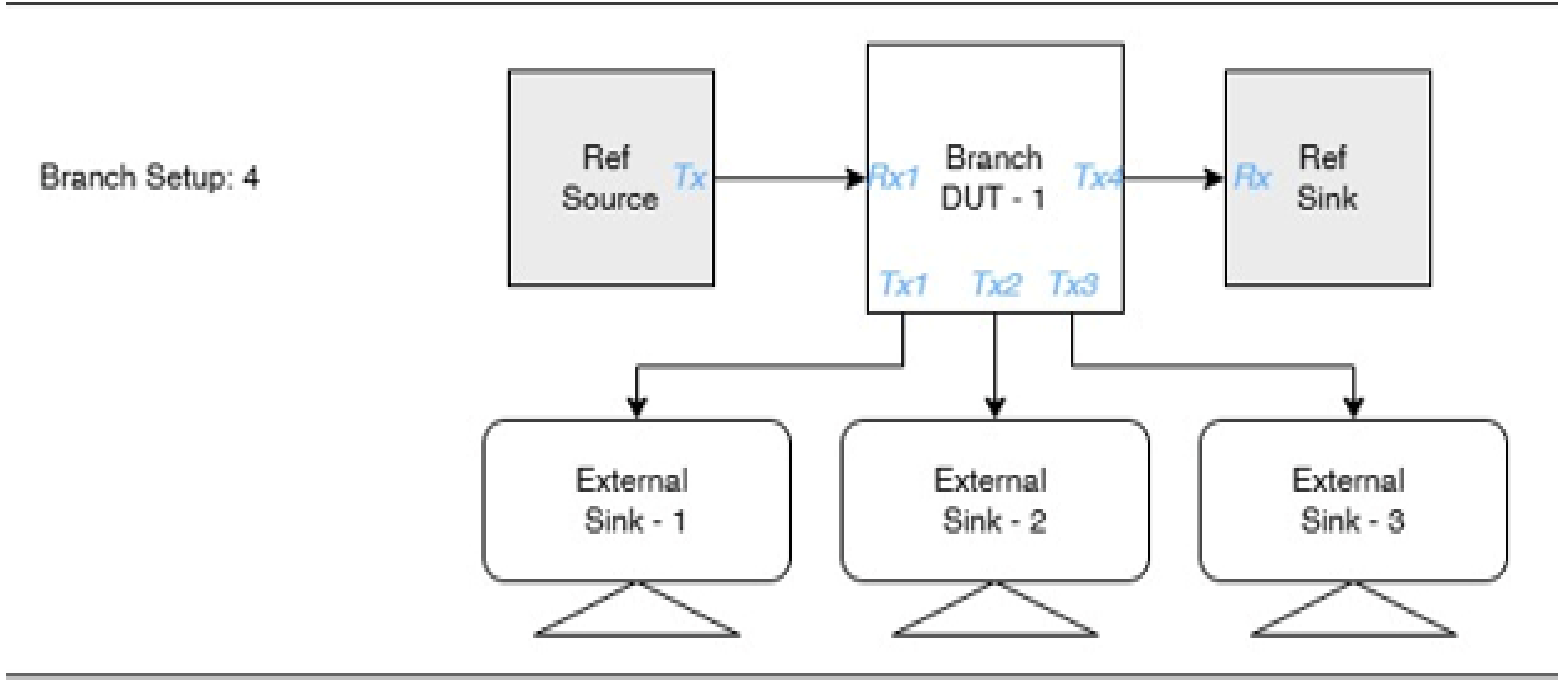
Branch Setup: 3



MST Branch Setup3 Tests

Tests	Objective	Main Points
6.2.3.1	Branch DUT responds correctly to the Link Address Request	Verify that the Branch DUT replies with an ACK to LINK_ADDRESS down request with the values as per the CDF, that is, the number of ports, port connected and as per the test setup on Rx by the Test equipment
6.2.3.2	Branch DUT Correctly calculates and allocates timeslots	Verify the Branch DUT's ability to correctly allocate timeslots for all the VCs on each of the DFPs
6.2.3.3	Branch DUT's Ability to send through the video stream accurately to an emulated Branch device on its DFP	Verify the Branch DUT's ability to forward video streams when multiple VCs are allocated to a single downstream port
6.2.3.4	Branch DUT's Ability to set up Low power mode on reference sink appropriately	Verify the Branch DUT's ability to set a DFP device in low power on POWER_DOWN_PHY down request
6.2.3.5	Branch DUT's Ability to come out of low power mode.	Verify the Branch DUT's ability to come out of low power mode upon POWER_UP_PHY down request
6.2.3.6	Branch DUT Generates CSN up request upon sink device disconnection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a sink device on one of the DFPs
6.2.3.7	Generates CSN up request upon sink device connection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon connection of a sink device on one of the DFPs
6.2.3.8	Generates CSN up request upon branch device disconnection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a branch device on one of the DFPs
6.2.3.9	Generates CSN up request upon branch device connection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon connection of a branch device on one of the DFPs
6.2.3.10	VC timeslots increase	Verify that the Branch DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are increased
6.2.3.11	VC timeslots decrease	Verify that the Branch DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are decreased
6.2.3.12	VC timeslots delete	Verify that the Branch DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are deleted
6.2.3.13	VC timeslots addition	Verify that the Branch DUT updates its VC table correctly when a new Virtual channel is added.
6.2.3.14	Generates CSN down request upon Upstream device disconnection	When an upstream device is disconnected, verify that Branch DUT issues a CONNECTION_STATUS_NOTIFY down request broadcast

MST Branch Setup4

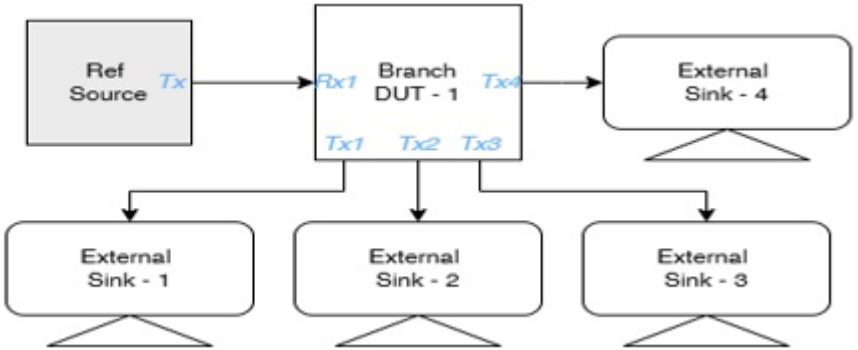


MST Branch Setup4 Tests

Tests	Objective	Main Points
6.2.4.1	Branch DUT responds correctly to the Link Address Request.	Verify that the Branch DUT replies with an ACK to LINK_ADDRESS down request with the values as per the CDF, that is, the number of ports, port connected and as per the test setup on Rx by the Test equipment
6.2.4.2	Branch DUT Correctly calculates and allocates timeslots	Verify the Branch DUT's ability to correctly allocate timeslots for all the VCs on each of the DFPs
6.2.4.3	Branch DUT's Ability to send through the video stream accurately to an emulated Branch device on its DFP	Verify the Branch DUT's ability to forward video streams when multiple VCs are allocated to a single downstream port
6.2.4.4	Branch DUT's Ability to set up Low power mode on reference sink appropriately	Verify the Branch DUT's ability to set a DFP device in low power on POWER_DOWN_PHY down request
6.2.4.5	Branch DUT's Ability to come out of low power mode	Verify the Branch DUT's ability to come out of low power mode upon POWER_UP_PHY down request
6.2.4.6	Branch DUT Generates CSN up request upon sink device disconnection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a sink device on one of the DFPs
6.2.4.7	Generates CSN up request upon sink device connection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon connection of a sink device on one of the DFPs
6.2.4.8	Generates CSN up request upon branch device disconnection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a branch device on one of the DFPs
6.2.4.9	Generates CSN up request upon branch device connection	Verify that the Branch DUT generates a CONNECTION_STATUS_NOTIFY up request upon connection of a branch device on one of the DFPs
6.2.4.10	VC timeslots increase	Verify that the Branch DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are increased
6.2.4.11	VC timeslots decrease	Verify that the Branch DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are decreased
6.2.4.12	VC timeslots delete	Verify that the Branch DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are deleted
6.2.4.13	VC timeslots addition	Verify that the Branch DUT updates its VC table correctly when a new Virtual channel is added.
6.2.4.14	Generates CSN down request upon Upstream device disconnection	When an upstream device is disconnected, verify that Branch DUT issues a CONNECTION_STATUS_NOTIFY down request broadcast

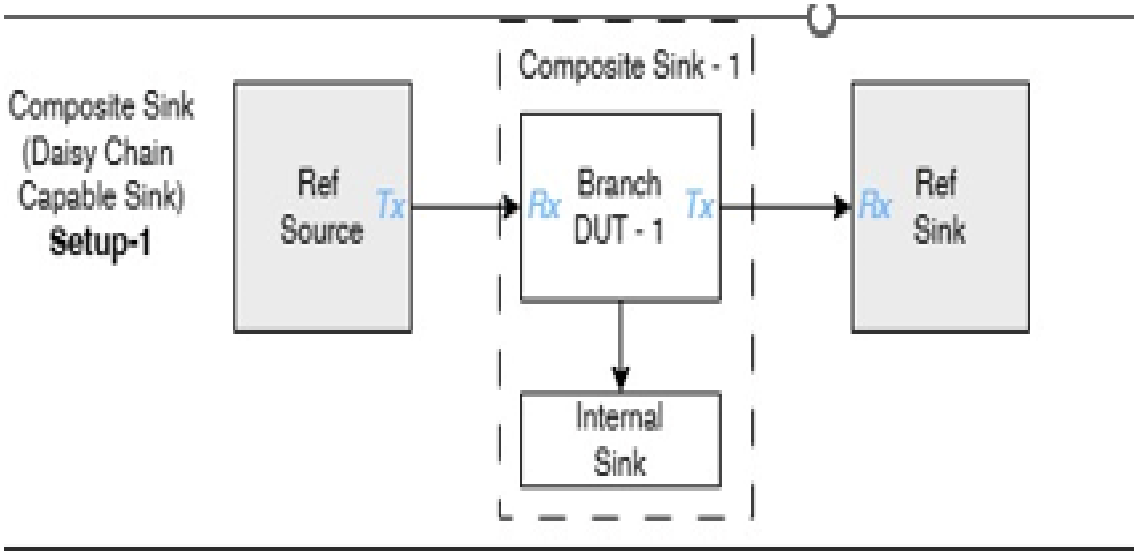
MST Branch Setup5 Tests

Branch Setup: 5



Tests	Objective	Main Points
6.2.5.1	Branch DUT responds correctly to the Link Address Request	Verify that the Branch DUT replies with an ACK to LINK_ADDRESS down request with the values as per the CDF, that is, the number of ports, port connected and as per the test setup on Rx by the Test equipment
6.2.5.2	*Branch DUT's Ability to send through the video stream accurately*	Verify the Branch DUT's ability to forward video streams when multiple VCs are allocated
6.2.5.3	Branch DUT's Ability to set up Low power mode on reference sink appropriately	Verify the Branch DUT's ability to set a DFP device in low power on POWER_DOWN_PHY down request
6.2.5.4	Branch DUT's Ability to come out of low power mode	Verify the Branch DUT's ability to come out of low power mode upon POWER_UP_PHY down request

Composite Sink Setup1



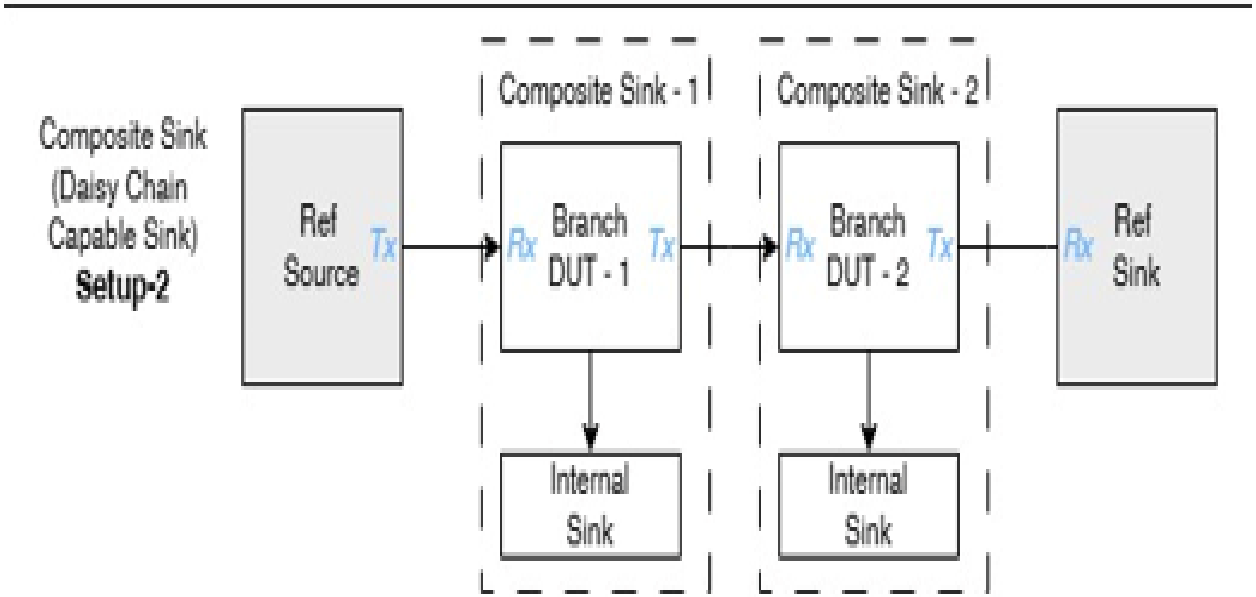
Composite Sink Setup1 Tests

Tests	Objective	Main Points
6.2.6.1	Composite Sink DUT has appropriate MST capabilities set	Verify that the Composite Sink DUT sets the correct MST capabilities in its DPCD registers
6.2.6.2	Composite Sink DUT responds correctly to the Link Address Request	Verify that the Composite Sink DUT replies with an ACK to LINK_ADDRESS down request with the values as per the CDF, that is, the number of ports, port connected and as per the test setup on Rx by the Test equipment
6.2.6.3	Composite Sink DUT forwards down requests accurately, and forwards down replies accurately	Verify that the Composite Sink DUT is able to forward the down requests after modifying the sideband headers. Similarly, also verify that the Composite Sink DUT is able to forward the down replies after modifying the sideband headers
6.2.6.4	Composite Sink DUT forwards up requests accurately, and forwards up replies accurately	Verify that the Composite Sink DUT is able to forward the up requests after modifying the sideband headers. Similarly, also verify that the Composite Sink DUT is able to forward the up replies after modifying the sideband headers
6.2.6.5	Composite Sink DUT responds correctly to Enum Path resources	Verify that the Composite Sink DUT replies with an ACK to ENUM_PATH_RESOURSES down request with the correct PBN value as per the lane count and link rate of the corresponding DP link
6.2.6.6	Composite Sink DUT responds correctly to Query Payload	After allocation of resources, verify that the Composite Sink DUT responds to QUERY_PAYLOAD down request with the correct values
6.2.6.7	Composite Sink DUT reads and responds to Remote_DPCD_read accurately	Verify that the Composite Sink DUT reads the DPCD registers on a DFP via native AUX transactions upon REMOTE_DPCD_READ down request and replies with an ACK with the correct values
6.2.6.8	Composite Sink DUT writes and responds to Remote_DPCD_write accurately	Verify that the Composite Sink DUT writes to the DPCD registers on a DFP via native AUX transactions upon REMOTE_DPCD_WRITE down request and replies with an ACK
6.2.6.9	Composite Sink DUT ability to forward correct video stream in DSC and Non-DSC cases	Verify that the Composite Sink DUT splits up and forwards video streams for a combination of DSC and Non-DSC cases
6.2.6.10	Composite Sink DUT Correctly calculates and allocates timeslots	Verify the Composite Sink DUT's ability to correctly allocate timeslots for all the VCs on each of the DFPs
6.2.6.11	Composite Sink DUT's Ability to send through the video stream accurately to an emulated Branch device on its DFP	Verify the Composite Sink DUT's ability to forward video streams when multiple VCs are allocated to a single downstream port

Composite Sink Setup1 Tests

Tests	Objective	Main Points
6.2.6.12	Composite Sink DUT's Ability to set up Low power mode on reference sink appropriately	Verify the Composite Sink DUT's ability to set a DFP device in low power on POWER_DOWN_PHY down request
6.2.6.13	Composite Sink DUT's Ability to come out of low power mode.	Verify the Composite Sink DUT's ability to come out of low power mode upon POWER_UP_PHY down request
6.2.6.14	Composite Sink DUT Generates CSN up request upon sink device disconnection	Verify that the Composite Sink DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a sink device on one of the DFPs
6.2.6.15	Generates CSN up request upon branch device disconnection	Verify that the Composite Sink DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a branch device on one of the DFPs
6.2.6.16	VC timeslots increase	Verify that the Composite Sink DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are increased
6.2.6.17	VC timeslots decrease	Verify that the Composite Sink DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are decreased
6.2.6.18	*VC timeslots delete*	Verify that the Composite Sink DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are deleted
6.2.6.19	VC timeslots addition	Verify that the Composite Sink DUT updates its VC table correctly when a new Virtual channel is added
6.2.6.20	*Generates CSN down request upon Upstream device disconnection*	When an upstream device is disconnected, verify that Composite Sink DUT issues a CONNECTION_STATUS_NOTIFY down request broadcast
6.2.6.21	Composite Sink DUT's ability to respond to REMOTE_DPCD_READ and REMOTE_DPCD_WRITE	When Reference source sends a down request of REMOTE_DPCD_READ and REMOTE_DPCD_WRITE verify the Composite Sink DUT's ability to do a native AUX read and write respectively
6.2.6.22	Composite Sink DUT's ability to respond to REMOTE_I2C_READ	When Reference source sends a down request of REMOTE_I2C_READ and verify the Composite Sink DUT's ability to do a I2C over AUX

Composite Sink Setup2



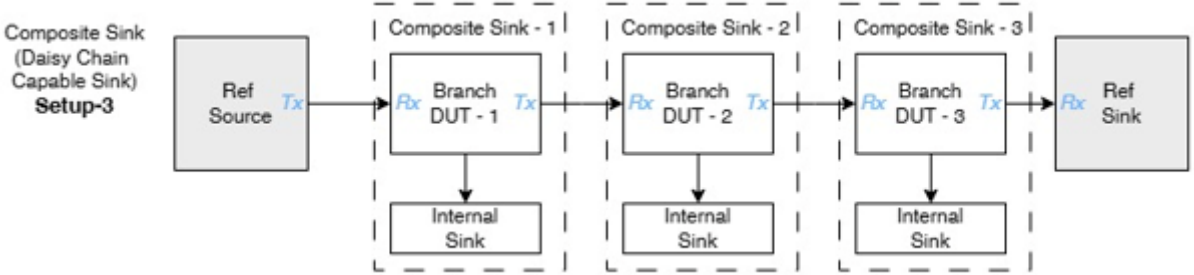
Composite Sink Setup2 Tests

Tests	Objective	Main Points
6.2.7.1	Composite Sink DUT responds correctly to the Link Address Request	Verify that the Composite Sink DUT replies with an ACK to LINK_ADDRESS down request with the values as per the CDF, that is, the number of ports, port connected and as per the test setup on Rx by the Test equipment
6.2.7.2	*Composite Sink DUT forwards down requests accurately, and forwards down replies accurately*	Verify that the Composite Sink DUT is able to forward the down requests after modifying the sideband headers. Similarly, also verify that the Composite Sink DUT is able to forward the down replies after modifying the sideband headers
6.2.7.3	*Composite Sink DUT forwards up requests accurately, and forwards up replies accurately*	Verify that the Composite Sink DUT is able to forward the up requests after modifying the sideband headers. Similarly, also verify that the Composite Sink DUT is able to forward the up replies after modifying the sideband headers
6.2.7.4	Composite Sink DUT responds correctly to Enum Path resources	Verify that the Composite Sink DUT replies with an ACK to ENUM_PATH_RESOURSES down request with the correct PBN value as per the lane count and link rate of the corresponding DP link
6.2.7.5	Composite Sink DUT responds correctly to Query Payload	After allocation of resources, verify that the Composite Sink DUT responds to QUERY_PAYLOAD down request with the correct values
6.2.7.6	Composite Sink DUT reads and responds to Remote_DPCD_read accurately	Verify that the Composite Sink DUT reads the DPCD registers on a DFP via native AUX transactions upon REMOTE_DPCD_READ down request and replies with an ACK with the correct values
6.2.7.7	Composite Sink DUT writes and responds to Remote_DPCD_write accurately	Verify that the Composite Sink DUT writes to the DPCD registers on a DFP via native AUX transactions upon REMOTE_DPCD_WRITE down request and replies with an ACK
6.2.7.8	Composite Sink DUT ability to forward correct video stream in DSC and Non-DSC cases	Verify that the Composite Sink DUT splits up and forwards video streams for a combination of DSC and Non-DSC cases
6.2.7.9	Composite Sink DUT Correctly calculates and allocates timeslots	Verify the Composite Sink DUT's ability to correctly allocate timeslots for all the VCs on each of the DFPs
6.2.7.10	Composite Sink DUT's Ability to send through the video stream accurately to an emulated Branch device on its DFP	Verify the Composite Sink DUT's ability to forward video streams when multiple VCs are allocated to a single downstream port
6.2.7.11	Composite Sink DUT's Ability to set up Low power mode on reference sink appropriately	Verify the Composite Sink DUT's ability to set a DFP device in low power on POWER_DOWN_PHY down request

Composite Sink Setup2 Tests

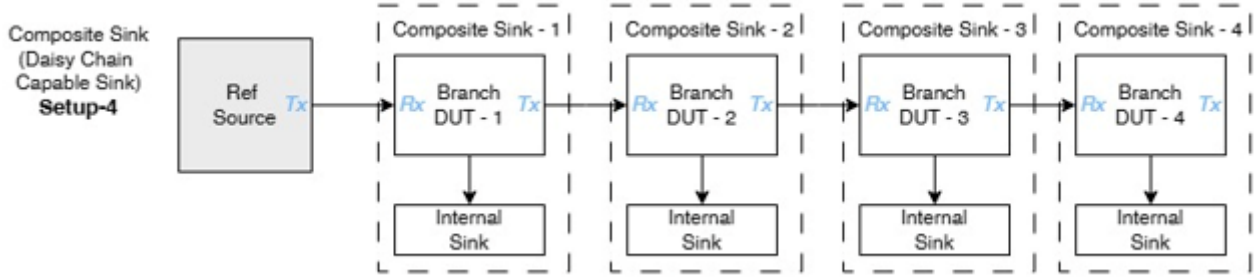
Tests	Objective	Main Points
6.2.7.12	Composite Sink DUT's Ability to come out of low power mode	Verify the Composite Sink DUT's ability to come out of low power mode upon POWER_UP_PHY down request
6.2.7.13	Composite Sink DUT Generates CSN up request upon sink device disconnection	Verify that the Composite Sink DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a sink device on one of the DFPs
6.2.7.14	Generates CSN up request upon sink device connection	Verify that the Composite Sink DUT generates a CONNECTION_STATUS_NOTIFY up request upon connection of a sink device on one of the DFPs
6.2.7.15	Generates CSN up request upon branch device disconnection	Verify that the Composite Sink DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a branch device on one of the DFPs
6.2.7.16	Generates CSN up request upon branch device connection	Verify that the Composite Sink DUT generates a CONNECTION_STATUS_NOTIFY up request upon connection of a branch device on one of the DFPs
6.2.7.17	VC timeslots increase	Verify that the Composite Sink DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are increased
6.2.7.18	VC timeslots decrease	Verify that the Composite Sink DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are decreased
6.2.7.19	VC timeslots delete	Verify that the Composite Sink DUT updates its VC table correctly when timeslots for a Virtual channel in the middle of the table are deleted
6.2.7.20	VC timeslots addition	Verify that the Composite Sink DUT updates its VC table correctly when a new Virtual channel is added.
6.2.7.21	Generates CSN down request upon Upstream device disconnection	When an upstream device is disconnected, verify that Composite Sink DUT issues a CONNECTION_STATUS_NOTIFY down request broadcast

Composite Sink Setup3 Tests



Tests	Objective	Main Points
6.2.8.1	Composite Sink DUT responds correctly to the Link Address Request	Verify that the Composite Sink DUT replies with an ACK to LINK_ADDRESS down request with the values as per the CDF, that is, the number of ports, port connected and as per the test setup on Rx by the Test equipment
6.2.8.2	Composite Sink DUT's Ability to set up Low power mode on reference sink appropriately	Verify the Composite Sink DUT's ability to set a DFP device in low power on POWER_DOWN_PHY down request
6.2.8.3	Composite Sink DUT's Ability to come out of low power mode.	Verify the Composite Sink DUT's ability to come out of low power mode upon POWER_UP_PHY down request
6.2.8.4	*Composite Sink DUT Generates CSN up request upon sink device disconnection*	Verify that the Composite Sink DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a sink device on one of the DFPs
6.2.8.5	Generates CSN up request upon sink device connection	Verify that the Composite Sink DUT generates a CONNECTION_STATUS_NOTIFY up request upon connection of a sink device on one of the DFPs

Composite Sink Setup4 Tests



Tests	Objective	Main Points
6.2.9.1	Composite Sink DUT responds correctly to the Link Address Request	Verify that the Composite Sink DUT replies with an ACK to LINK_ADDRESS down request with the values as per the CDF, that is, the number of ports, port connected and as per the test setup on Rx by the Test equipment
6.2.9.2	*Composite Sink DUT Generates CSN up request upon sink device disconnection*	Verify that the Composite Sink DUT generates a CONNECTION_STATUS_NOTIFY up request upon disconnection of a sink device on one of the DFPs
6.2.9.3	Generates CSN up request upon sink device connection	Verify that the Composite Sink DUT generates a CONNECTION_STATUS_NOTIFY up request upon connection of a sink device on one of the DFPs

- Q/A

Lunch – Demo Tables

DisplayPort Electrical Testing Overview

Abhijeet Shinde
Keysight Technologies
05/23/2025

Agenda

- DP2.1 Electrical Compliance Test Requirements
- DP2.1 PHY Updates
- DP2.1 Transmitter Test
- DP2.1 Receiver Test
- eDP PHY Electrical Conformance Testing

DP2.1a Electrical Compliance Test Requirement

DisplayPort Interface

Main Link

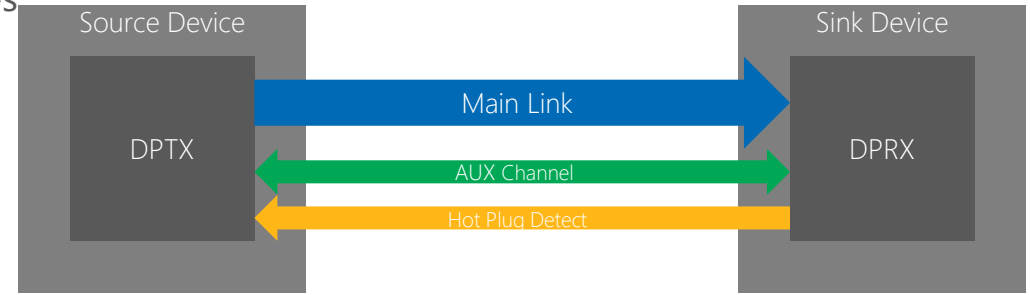
- Display data transfer
- 4 unidirectional high-speed lanes
- Multiple bitrates supported

AUX Channel

- Link management
- Test mode control
- 1 bidirectional low-speed lane

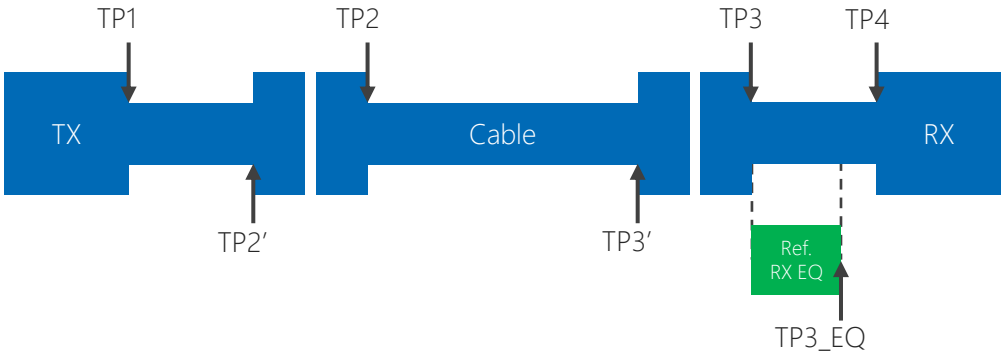
Hot Plug Detect

- Source detects presence of sink
- Sink notifies of status changes via IRQ



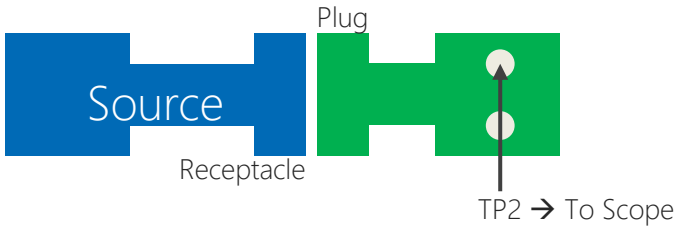
Test Points

Test Point	Definition
TP1	Source transmitter pins.
TP2	Test interface of a TPA, next to mated connection to a DP source.
TP2’	RX JTOL signal injection point for DUTs with plug.
TP2_CTLE	RX JTOL calibration and test point for DUTs with plug.
TP3	Test interface of a TPA, next to mated connection to a DP sink.
TP3’	Signal injection point to a DP sink.
TP3_EQ	TP3 using a defined cable model with equalization applied.’
TP3_CTLE	TP3 using a defined HBR3 cable model with CTLE applied.
TP3_DFE	TP3 using a defined HBR3 cable model with CTLE and DFE applied.
TP4	Sink receiver pins.

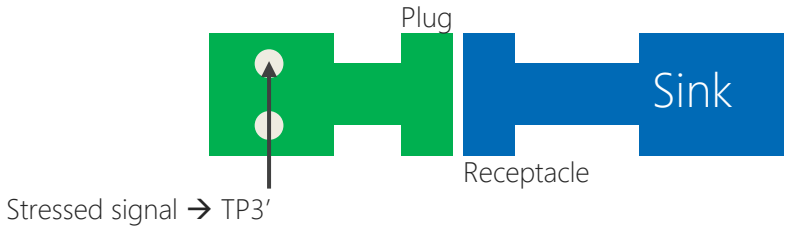


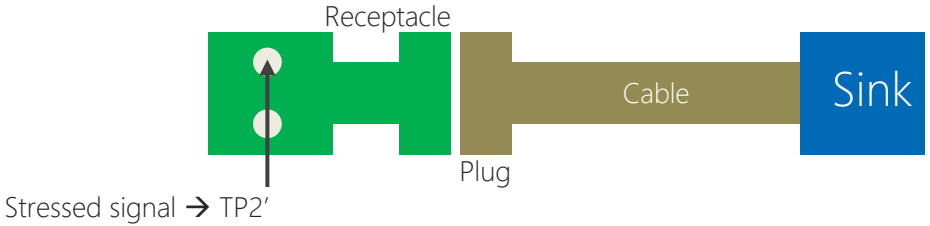
Test Point Access Examples

DPTX Testing



DPRX Testing





How to test the PHY layer?

Source

- Configure the source to output test patterns with certain drive settings → **AUX controller**
- Embed worst-case channels, apply equalization on the oscilloscope
- Run measurements

Sink

- Generate the stress signal with a pattern generator
- Guide the sink through Link Training → **AUX controller**
- Read built-in error counter → **AUX controller**

DP2.1 PHY Updates

Electrical Updates from DP2.1 to DP2.1a to DP2.1b

- There are minimal changes in 8b/10b electrical compliance testing.
- A new DP54 cable has been introduced in DP2.1a for UHBR13.5.
- The UHBR13.5 Source Enhanced FSDP testing will utilize the new DP54 cable model.
- A new DP80LL cable has been introduced in DP2.1b for UHBR20.
- The UHBR20 Source will utilize the DP80LL cable with a 9dB loss budget.
- Changes in test limits primarily affect Source Testing.

- UHBR10
  - DPTX TP2
    - Total Jitter =380 mUI
    - Data-Dependent Jitter =160 mUI
    - Eye Width = 600 mUI
    - Eye Height = 242 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 185 mV
  - DPTX TP3_EQ
    - Total Jitter =450 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 115 mV
  - DPRX TP3_EQ
    - Total Jitter =485 mUI
    - Data-Dependent Jitter =240 mUI
    - Eye Width = 540 mUI
    - Eye Height = 112 mV
- UHBR20
  - DPTX TP2
    - Total Jitter =435 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 240 mV
  - DPTX TP3_EQ
    - Total Jitter =455 mUI
    - Data-Dependent Jitter =210 mUI
    - Eye Width = 560 mUI
    - Eye Height = 100 mV
  - DPRX TP3_EQ
    - Data-Dependent Jitter =255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV

- UHBR10
  - DPTX TP2
    - Total Jitter =440 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 550 mUI
    - Eye Height = 162 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 200 mV
  - DPTX TP3_EQ
    - Total Jitter =515 mUI
    - Data-Dependent Jitter =245 mUI
    - Eye Width = 520 mUI
    - Eye Height = 80 mV
  - DPRX TP3_EQ
    - Total Jitter =530 mUI
    - Data-Dependent Jitter =260 mUI
    - Eye Width = 520 mUI
    - Eye Height = 73 mV
- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI

- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI

- UHBR20
  - DPTX TP2 EnhDP DP80
    - Total Jitter = 480 mUI
    - Data-Dependent Jitter = 200 mUI
    - Eye Width =540 mUI
    - Eye Height = 240 mV
  - DPTX TP2 EnhDP DP80LL
    - Total Jitter = 495 mUI
    - Data-Dependent Jitter = 220 mUI
    - Eye Width =530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ for all connector Type
    - Total Jitter = 500 mUI
    - Data-Dependent Jitter = 210 mUI
    - Eye Width =560 mUI
    - Eye Height = 100 mV
  - DPRX TP3EQ for all connector type
    - Data-Dependent Jitter = 255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV

DP2.1 CTS Errata

- Clarification on 8b/10b SSC Modulation Deviation Limit
- Test fixture insertion loss update
- FFE Preset 15 measurement update
- LTTPR Frequency Variation test update
- Eye Height and Mask requirement update for UHBR Rates
- BERT Preset Calibration

DP2.1 Transmitter Test

Electrical Transmitter Tests

Item	Name	Normative/ Informative
3.1	Eye Diagram Test	Normative
3.2	HBR/RBR Non-PE Level Verification Test	Normative
3.3	HBR/RBR PE Level Verification and Maximum Differential Peak-to-Peak Voltage Test	Normative
3.4	HBR3/HBR2 PE Level and Equalization Verification Test	Normative
3.5	HBR3/HBR2 $V_{TX\_DIFFp\text{-}p\_MAX}$ Test	Normative
3.6	Inter-pair Skew Test	Informative
3.7	Intra-pair Skew Test	Informative
3.8	AC Common Mode Noise Test	Informative
3.9	Non-ISI Jitter Measurement Test	Normative
3.10	HBR3 TX Differential RL Test	Informative
3.11	TJ/RJ/DJ Measurement Tests	Normative
3.12	Main-Link Frequency Compliance Test	Normative
3.13	Spread-spectrum Modulation Frequency Test	Normative
3.14	Spread-spectrum Modulation Deviation Test	Normative
3.15	dF/dT Spread-spectrum Deviation High-frequency Variation Test	Informative
xx	Embedded Re-timer Frequency Variation Test	Normative

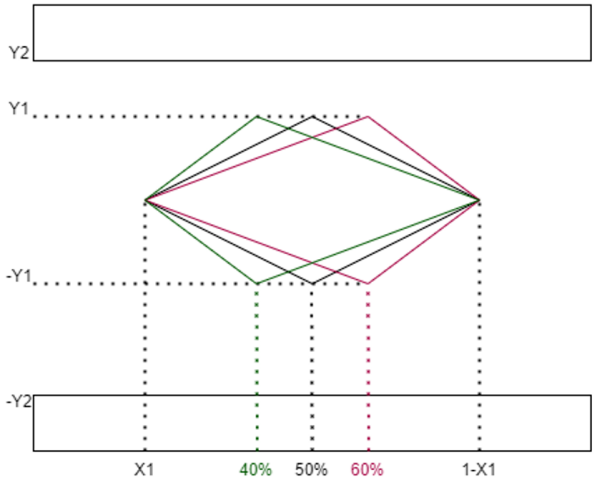
8b/10b

Item	Name	Normative/ Informative
4.2	Preset and CTLE-DFE Declaration	Normative
4.3	UHBR Source Transmitter Equalization	Normative
4.4	UHBR Bit Rate	Normative
4.4	UHBR Unit Interval	Informative
4.5	UHBR SSC Down Spread Range, Rate, Phase Deviation, and Slew Rate	Normative
4.6	UHBR Embedded Re-timer Frequency Variation	Informative
4.7	UHBR TP2 Eye at 1E-6 BER	Normative
4.8	UHBR TP2 Jitter at 1E-9 BER	Normative
4.9	UHBR AC Common Mode Nosie Test	Informative
4.10	UHBR TP3_EQ Eye at 1E-6	Normative
4.11	UHBR TP3_CTLE Jitter at 1E-9	Informative
4.12	UHBR Transmitter Return Loss	Informative

128b/132b

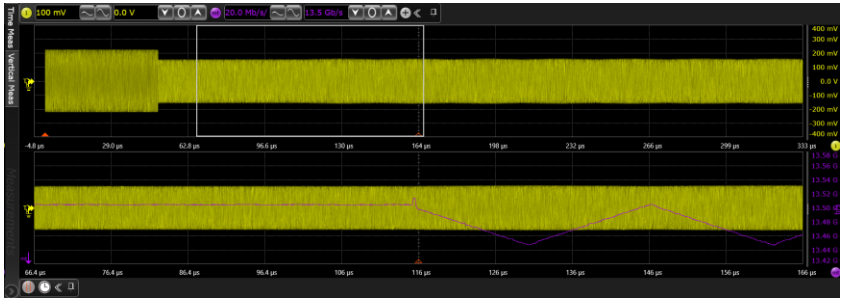
UHBR Eye Mask Update

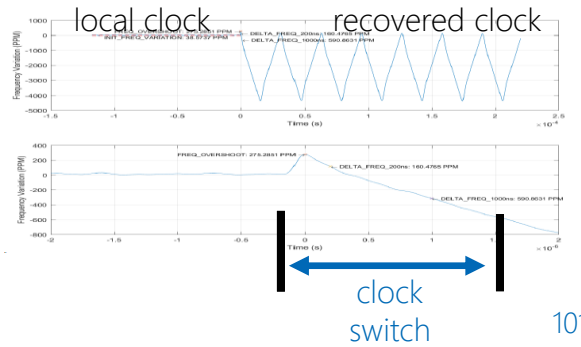
- If original eye mask fails, then modified mask will be used to re-test.
- Modify mask must comply the Y1 and X1 as per the DP 2.1 PHY CTS



LTTPR Frequency Variation Test

- LTTPRs are needed as total channel loss increases with the PHY rate
  - Longer channel
  - More complex link training
- LTTPR Re-timer Clock Switch Test Mode
  - DPCD 0x0010B – 0x0010Eh [7] =1
- Initial Test Challenges
  - Entering Clock Switch test mode
  - Triggering on LTTPR local clock event





DP TX testing challenges

- The test time for DP TX is significant
- DP Source not supporting PHY Test Automation
  - DP Source does not transmit the compliance pattern

DP2.1 Receiver Test

Electrical Receiver Tests

Item	Name	Normative/ Informative
5.1	8b/10b DP Sink JTOL Test	Normative

Item	Name	Normative/ Informative
6.1	128b/132b DP UHBR Sink JTOL Test	Normative

Item	Calibration Point	Name
5.1.3.1.1	TP1-TP3	HBR3 Jitter Calibration
5.1.3.1.2	TP1-TP3	HBR2 Jitter Calibration
5.1.3.1.3	TP1-TP3	HBR Jitter Calibration
5.1.3.1.4	TP2/TP3	HBR3 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR2 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR Eye Height and Total Jitter Calibration
5.1.3.1.5	TP1/TP3	HBR3/HBR2/HBR Crosstalk Calibration
5.1.3.2	TP2/TP3	RBR Jitter Calibration
5.1.3.2	TP3	RBR Eye Height Calibration
5.1.3.2.1	TP3	RBR Crosstalk Calibration

Item	Calibration Point	Name
6.1.3.1.4.1	TP1	AC Common-Mode Interference Calibration
6.1.3.1.4.2	TP1	Random Jitter Calibration
6.1.3.1.4.3	TP1	Periodic Jitter Calibration
6.1.3.1.4.4	TP1	Total Jitter Calibration
6.1.3.1.4.5	TP1	Eye Height Calibration
6.1.3.1.5	TP3	Insertion Loss Calibration
6.1.3.1.6	TP3	Eye Diagram Calibration

BERT Preset Calibration

- To verify the BERT FFE as outlined in the DP 2.1 PHY CTS specification
- The Preset calibration check can assist in identifying setup problems.

Set Preset []	Expected Preshoot [dB]	Measured Preshoot [dB]	Expected Deemphasis [dB]	Measured Deemphasis [dB]	Coeff_1 []	Coeff0 []	Coeff1 []	Pass/Fail
1	0.00	0.10	-1.90	-1.75	0.030	0.870	-0.100	Pass
2	-3.10	-3.16	-3.60	-3.57	0.130	0.690	-0.180	Pass
3	0.00	0.03	-5.00	-4.81	0.030	0.750	-0.220	Pass
4	0.00	-0.20	-8.40	-8.25	0.030	0.655	-0.315	Pass
5	0.90	1.13	0.00	0.20	-0.035	0.965	0.000	Pass
6	1.10	1.18	-1.90	-1.86	-0.020	0.880	-0.100	Pass
7	1.40	1.35	-3.80	-3.60	-0.020	0.810	-0.170	Pass
8	1.70	1.65	-5.80	-5.61	-0.020	0.750	-0.230	Pass
9	2.10	2.03	-8.00	-7.89	-0.020	0.690	-0.290	Pass
10	1.70	1.82	0.00	0.13	-0.080	0.920	0.000	Pass
11	2.20	2.49	-2.20	-2.24	-0.080	0.820	-0.100	Pass
12	2.50	2.31	-3.60	-3.47	-0.060	0.790	-0.150	Pass
13	3.40	3.57	-6.70	-6.64	-0.070	0.700	-0.230	Pass
14	3.60	3.67	0.00	0.01	-0.170	0.830	0.000	Pass

DP RX testing challenges

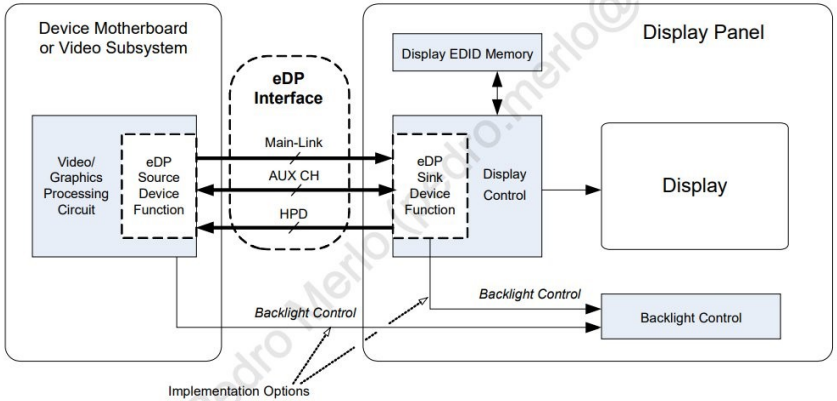
- DP Sink does not enable error count registers
- Calibrations take a significant amount of time
  - Different setup needs for 8b/10b and 128b/132b

VESA

Embedded DisplayPort

eDP

- Standardized features and interoperability guidelines
  - Feature set determined by the system integrator
- Current specification is eDP2.0
  - Based on DP2.1
- No compliance program = Conformance Test!!



eDP2.0 Update

- eDP2.0 v1.0 published in September 2024
- Supports 128b/132b encoding
- Supports UHBR data rates
  - UHBR10, UHBR13.5 and UHBR20
- Leverages worst-case end-to-end link budget from DP2.1

Key Differences eDP2.0 vs DP2.1

Required

- DPCD registers for eDP
- Reduced AUX timing
- Enhanced framing
- Fast link training (sink)
- eDP-specific sink noise/jitter budget, reference EQ

Optional

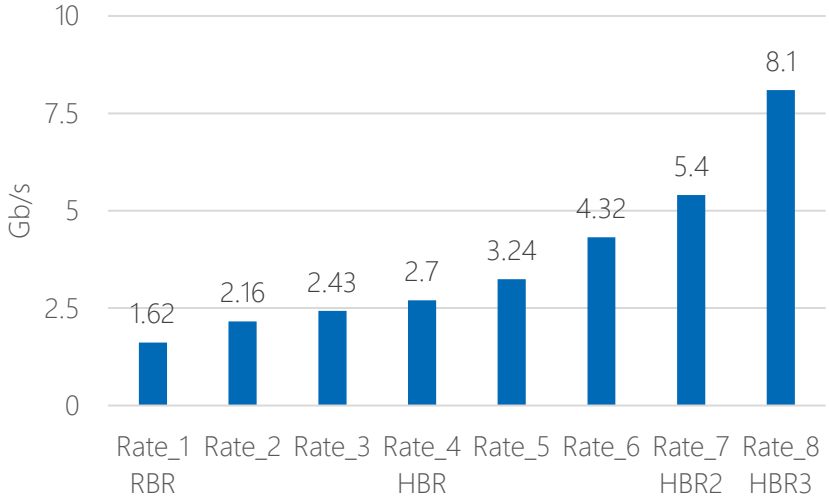
- Low AUX voltage swing
- Source detection by way of AUX CH
- STREAM_STATUS_CHANGED bits support
- GUID registers support
- Fast link training (host)
- Reduced main-link voltage swing level
- EDID
- HPD pin on sink device

Recommended

- Fewest number of lanes possible

Main Link Differences

- Eight 8b/10b rates, and Three UHBR rates
- Custom rates supported



- TP3_EQ total jitter budget
- BER = 10^{-9}

Test Point	Description	I/N	DJ_{MAX}	TJ_{MAX}
TP1	eDPTX package pin	Informative	0.17 UI	0.27 UI
TP2	Source device eDP cable connector	Informative	N/A	N/A
TP3	Sink device (panel) eDP cable connector	-	-	-
TP3_EQ	**After reference RX equalizer**	**Normative**	**0.41 UI**	**0.50 UI**
TP4	eDPRX package pins	Informative	0.46 UI	0.55 UI

AUX Channel Differences

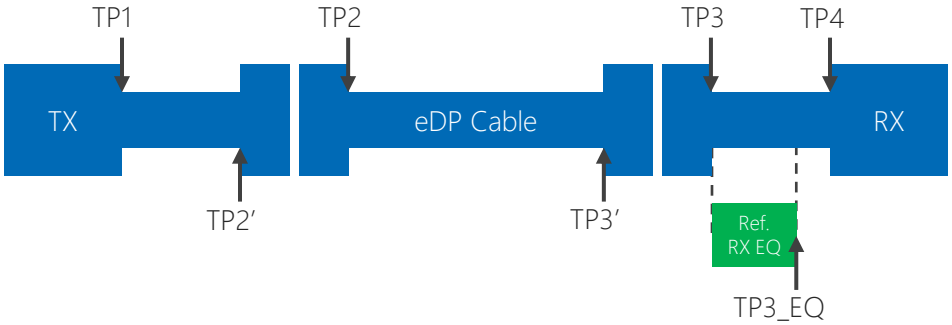
- No AC-coupling capacitors on Sink device side
- No pull-up/-down resistors
- Why?
  - The Sink device does not monitor the common mode voltage on AUX_CH_P and AUX_CH_N for Source device Hot Plug/Unplug and powered/unpowered detection

eDP Electrical Specification

- Low voltage swing levels
- Framework to apply optional customized voltage swings
- Reduced RX differential voltage sensitivity
- New transfer rates
- Framework to apply jitter specifications to optional customized frequencies
- Same Link Training procedures and voltage swing tables like DP, but with lower signal voltages

eDP Transmitter Test

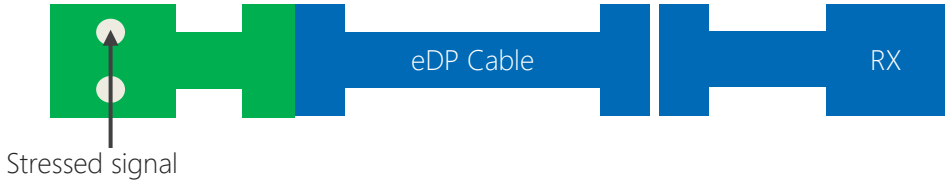
- Test Point/Fixture

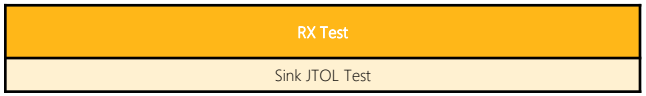


Recommended Source Main-Link TX Electrical Specification
Link Rate
Unit Interval
Total Jitter
Residual ISI
Non-ISI
Eye Diagram

eDP Receiver Test

- Test Point/Fixture





Calibration Point	RX Calibration
TP1	Sinusoidal Jitter Calibration
TP1	Random Jitter Calibration
TP3	Residual ISI
TP3	Eye Diagram
TP3	Crosstalk

VESA

Thank You!

DP Alt Mode v 2.1a Overview and Updates

Tim Wei– Senior Application Engineer

Ellisys

May 23, 2025

Ellisys USB Test and Analysis Solutions

USB Explorer™ 350

Multi-function USB Type-C®, USB 3.2, and Power Delivery Protocol Test Platform

VESA-Approved Tester for DisplayPort ALT Mode

Type-C Tracker™

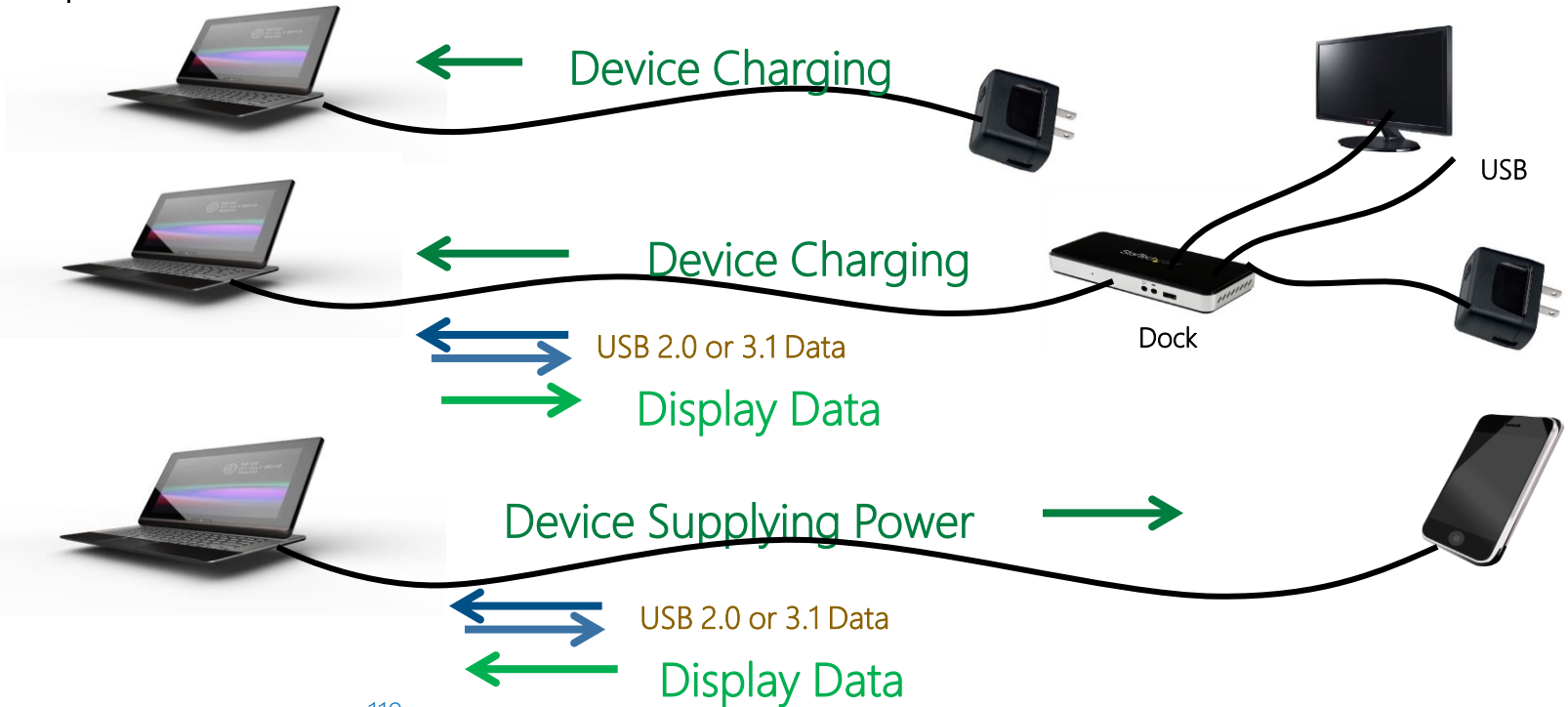
Protocol and Electrical Analysis Tool for USB Type-C® Standards

Includes DP AUX and DP ALT Support

ellisys
Better Analysis

Example USB Type-C Configurations

Either end can serve as USB Host, USB-PD Power Consumer, and DisplayPort Video Source (these services are independent of each other



DP Alt Mode over USB-C Ecosystem is Mainstream


USB-C Tablets


USB-C Laptops


USB-C Displays


Multi Function Adapters

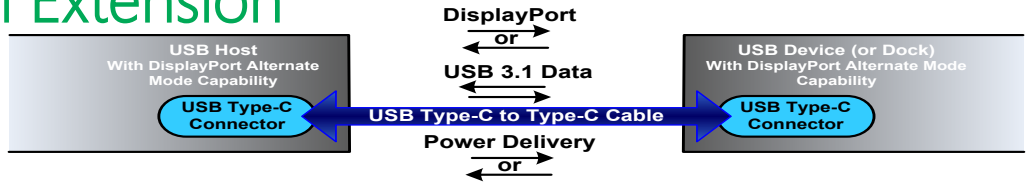
All types of certified adapters available

- C to DP adapters, Multifunction docks
- Type C protocol converters (HDMI, VGA, DVI) using DP Alt Mode

More are certified every week

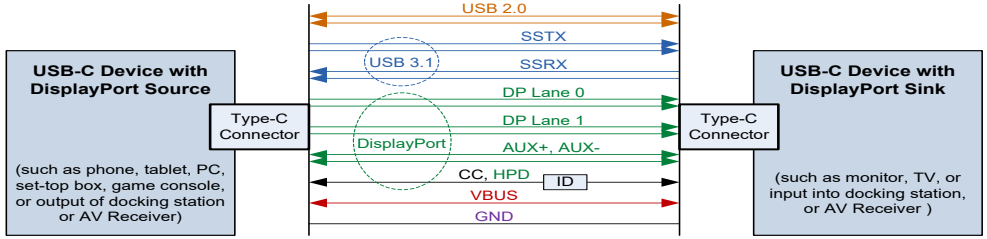
- Major PC OEMs continue to launch new products with DP Alt Mode over USB-C
- Major Display OEMs continue to add USB-C inputs to their products

USB-C Connector Functional Extension DP Alt Mode



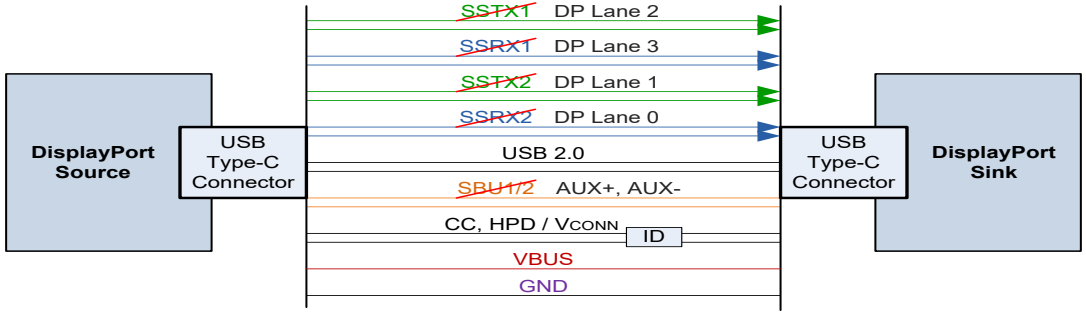
- A passive Full Feature USB Type-C to Type-C cable can carry up to four DisplayPort lanes
  - Same performance and features as a standard DisplayPort connection
  - Allows DisplayPort data rates to increase in the future, since the USB Type-C connector has very high data rate capability
- DisplayPort can be combined with USB 3.2 operation over the same USB Type-C cable
- USB 2.0 and USB Power Delivery is available in all configurations

2xDisplayPort and USB 3.2 over a Standard USB-C Cable



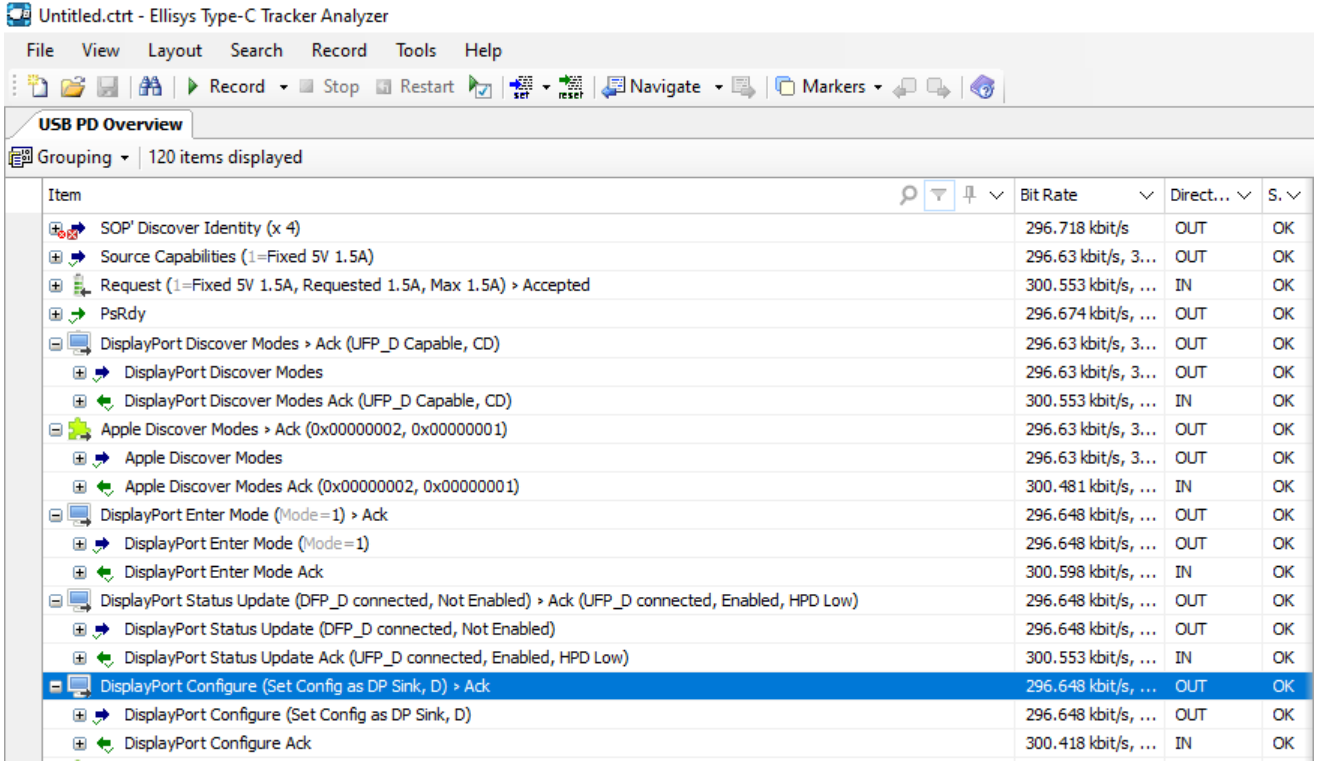
- Uses a standard “Full Feature” USB-C to USB-C cable which is designed to include DisplayPort
- The above configuration uses two high-speed lanes each for DisplayPort and USB 3.2
  - Ideal for docking stations, or for displays or TVs that include USB 3.2 functions
- DisplayPort performance provided by two lanes
  - HBR3: 4K(3840x2160)@60fps 24bpp
  - UHBR20: 8K (7680x4320)@30fps 30bpp

4xDP Over a USB Type-C to USB Type-C Full Feature Passive Cable



- Utilizes optional DP Alt Mode capability of USB Type-C connector
- DisplayPort can use all four high speed lanes to deliver full DisplayPort performance
- The DisplayPort AUX Channel uses the SBU pins
- The DisplayPort HPD / IRQ is transmitted over the CC pin using the USB-PD protocol
- USB 2.0 and USB Power Delivery always available
- DisplayPort performance provided by four lanes
  - HBR3: 5K (5120x2800)@60fps 24bpp
  - UHBR20: 10K (10240x4320)@60fps 24bpp

Typical DisplayPort Alternate Mode Flow



DisplayPort Alternate Mode 2.1 Update

- SVDM Header Update (by USB PD Spec)
- Cable DP Capabilities VDO update to support UHBR20 and UHBR13.5
  - Both passive and active cables
- SOP' Active Cable DisplayPort Configurations VDO update
- DP Capabilities VDO Update (DPAM Version field)
- SOP DisplayPort Configurations VDO Update
  - Cable information
  - DPAM Version
- DisplayPort Status Update VDO Update

SVDM Header Update

12:11	**Structured VDM Version (Minor)[a]**	Version number (Minor) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier 01b = Version 2.1 All other values are RESERVED.
14:13	**Structured VDM Version (Major)[a]**	Version number (Major) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier. 01b = Version 2.x. (x indicates SVDM minor version) All other values are RESERVED.

12:11 was reserved

Cable DP Capabilities VDO update

Table 4-5: SOP' Cable DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)[a]

Bit(s)	Description	Values
1:0	**RESERVED**	RESERVED (always 00b).
5:2	**Signaling for Transport of DisplayPort Protocol[b]**	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[c]
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**DP Source Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported. 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
23:16	**DP Sink Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
25:24	**RESERVED**	RESERVED (always 00b).
26[d]	**UHBR13.5**	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[c]
27	**RESERVED**	RESERVED (always 0).
29:28[d]	**Active Component**	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30	**DPAM Version**	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 4-2: Active Cable DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)

Bit(s)	Description	Values
1:0	RESERVED	RESERVED (always 00b).
5:2	Signaling for Transport of DisplayPort Protocol[a]	XXX1b = Supports *DP* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	DP Source Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported. All other values are RESERVED.
23:16	DP Sink Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). All other values are RESERVED.
31:24	RESERVED	RESERVED (always 00h).

a. "X" value indicates "Don't Care."

Active Cable DisplayPort Configurations VDO update

Table 4-7: SOP' Active Cable DisplayPort Configurations

Bit(s)	Description	Values
1:0	**Select Configuration**	00b = Set configuration for *USB*.[a] 01b = Set configuration for active cable as a *DP* Source device (UFP_U is a *DP* Source device).[b] 10b = Set configuration for active cable as a *DP* Sink device (UFP_U is a *DP* Sink device).[b] 11b = RESERVED.
5:2	**Signaling for Transport of DisplayPort Protocol**	0h = Bit rate is unspecified (used only when the Select Configuration field is programmed for USB Configuration). 1h = Select *DP* bit rates and electrical settings. All other values are RESERVED.
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**Configure Active Cable Pin Assignment**	00h = Deselect pin assignment. 04h = Select Pin Assignment C.[c] 08h = Select Pin Assignment D.[d] 10h = Select Pin Assignment E.[e] All other values are RESERVED.
31:16	**RESERVED**	RESERVED (always 0000h).

Table 4-4: Active Cable DisplayPort Configurations

Bit(s)	Description	Values
1:0	Select Configuration	00b = Set configuration for *USB*.[a] 01b = Set configuration for active cable as a *DP* Source device (UFP_U is a *DP* Source device).[b] 10b = Set configuration for active cable as a *DP* Sink device (UFP_U is a *DP* Sink device).[b] 11b = RESERVED.
5:2	Signaling for Transport of DisplayPort Protocol	0h = Bit rate is unspecified (used only when the Select Configuration field is programmed for USB Configuration). 1h = Select *DP* bit rates and electrical settings. All other values are RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	Configure Active Cable Pin Assignment	00h = De-select pin assignment. 04h = Select Pin Assignment C.[c] 08h = Select Pin Assignment D.[d] All other values are RESERVED.
31:16	RESERVED	RESERVED (always 0000h).

No Pin Assignment E

DP Capabilities VDO Update

Table 5-6: DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	**Port Capability**	00b = RESERVED. 01b = *DP* Sink Device Capable (including *DP* Branch device). 10b = *DP* Source Device Capable (including *DP* Branch device). 11b = Both *DP* Source and Sink Device Capable.
5:2	**Signaling for Transport of DisplayPort Protocol**	XXX1b = Supports *DP* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	**Receptacle Indication**	0 = *DP* interface is presented on a *USB-C* plug. 1 = *DP* interface is presented on a *USB-C* receptacle.
7	**USB 2.0 Signaling Not Used**	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	**DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)**	00000000b = *DP* Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	**DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)**	00000000b = *DP* Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
29:24	**RESERVED**	RESERVED (always 00h).
31:30	**DPAM Version[i]**	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 5-5: DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED. 01b = *DP* Sink device-capable (including *DP* Branch device). 10b = *DP* Source device-capable (including *DP* Branch device). 11b = Both *DP* Source and Sink device-capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = *DP* interface is presented on a *USB-C* plug. 1 = *DP* interface is presented on a *USB-C* receptacle.
7	USB 2.0 Signaling Not Used	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	DP Source Device Pin Assignments Supported (reported by a *DP* Source device receptacle or *DP* Sink device (direct-attach) plug)	00000000b = *DP* Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a *DP* Sink device receptacle or *DP* Source device (direct-attach) plug)	00000000b = *DP* Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
31:24	RESERVED	RESERVED (always 00h).

If SVDM Version is 2.1 or higher, DPAM Version field is applicable else this field shall be set to 00b.

A Bit More Background

From DisplayPort Alt Mode 2.0 Spec

Future versions of this Standard may describe other modes associated with the DP_SID. Such modes shall be identified by having a non-zero value in bits 31:24 of the VDO. The DFP_U shall examine the list of modes returned until it finds 0s in bits 31:24 of the VDO and a non-zero value in bits 23:0 of the VDO (i.e., DP Capabilities). The DFP_U and UFP_U shall use the corresponding offset (indexed from 1) as the Object Position in the following commands:

SOP DisplayPort Configurations VDO Update

Table 5-13: SOP DisplayPort Configurations

Bit(s)	Description	Values
1:0	**Select Configuration**	00b = Set configuration for *USB*.[a] 01b = Set configuration for UFP_U as a *DP* Source device.[b] 10b = Set configuration for UFP_U as a *DP* Sink device.[b] 11b = RESERVED.
5:2[c]	**Signaling for Cable Information Transport of DisplayPort Protocol**	XXX1b = Supports all defined *DP* bit rates up to HBR3 -or- capability is unknown XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[d]
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**Configure UFP_U Pin Assignment**	00h = Deselect pin assignment. 04h = Select Pin Assignment C.[e] 08h = Select Pin Assignment D.[f] 10h = Select Pin Assignment E.[g] All other values are RESERVED.
25:16	**RESERVED**	RESERVED (always 0000000000b).
26[h]	**Cable UHBR13.5 Support**	0 = Not supported.[i] ~~-or- capability is unknown~~ 1 = Supported.
27	**RESERVED**	RESERVED (always 0).
29:28[h]	**Cable Active Component**	00b = Passive -or- cable type is unknown 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30[j]	**DPAM Version**	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 5-8: DisplayPort Configurations

Bit(s)	Description	Values
1:0	Select Configuration	00b = Set configuration for *USB*.[a] 01b = Set configuration for UFP_U as a *DP* Source device.[b] 10b = Set configuration for UFP_U as a *DP* Sink device.[b] 11b = RESERVED.
5:2	Signaling for Transport of DisplayPort Protocol	0h = Bit rate is unspecified (used only when the Select Configuration field is programmed for USB Configuration). 1h = Select *DP* bit rates and electrical settings. All other values are RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	Configure UFP_U Pin Assignment	00h = De-select pin assignment. 04h = Select Pin Assignment C.[c] 08h = Select Pin Assignment D.[d] 10h = Select Pin Assignment E.[e] All other values are RESERVED.
31:16	RESERVED	RESERVED (always 0000h).

- This is the most challenging part for DPAM 2.1 DFP_U

DisplayPort Status Update VDO Update

Table 5-7: DisplayPort Status Update

Bit(s)	Description	Values
1:0	**DP Source/Sink Device Connected**	00b = Neither a *DP* Source device nor *DP* Sink device is connected, –or– the adapter is disabled. 01b = *DP* Source device is connected. 10b = *DP* Sink device is connected.[a] 11b = Both a *DP* Source and Sink device are connected.
2[b]	**Power Low**	0 = Adapter is not in low power state ~~is functioning normally or is disabled~~. 1 = Adapter has detected low power ~~and disabled *DP* support~~.
3[b]	**Enabled**	0 = Adapter *DP* functionality is disabled. 1 = Adapter *DP* functionality is enabled and operational.
4[d]	**Multifunction Preferred**	0 = No preference for multifunction. 1 = Multifunction is preferred.
5[c]	**DisplayPort/ USB Configuration Request**	0 = Request change to DisplayPort Configuration (if currently in USB Configuration). 1 = Request change to USB Configuration (if currently in DisplayPort Configuration).
6[c]	**Exit DisplayPort Alt Mode Request**	0 = Maintain the current mode. 1 = Request exit from DisplayPort Alt Mode (if currently in DisplayPort Alt Mode).
7[d]	**HPD State**	0 = HPD_Low. 1 = HPD_High.[e]
8[d]	**IRQ_HPD**	0 = IRQ_HPD has not been issued since the last status Message. 1 = IRQ_HPD.[f]
9[g]	**NO_DPAM_SUSPEND**	0 = UFP_U/ DP Sink device has no preference for entry into low power state. 1 = UFP_U/ DP Sink device prefers not to enter low power state.
31:10	**RESERVED**	RESERVED (always 0000000h).

Table 5-6: *DisplayPort Status Update*

Bit(s)	Description	Values
1:0	DP Source/Sink Device Connected	00b = Neither a *DP* Source device nor *DP* Sink device is connected, –or– the adapter is disabled. 01b = *DP* Source device is connected. 10b = *DP* Sink device is connected.[a] 11b = Both a *DP* Source and Sink device are connected.
2[b]	Power Low	0 = Adapter is functioning normally or is disabled. 1 = Adapter has detected low power and disabled *DP* support.
3[b]	Enabled	0 = Adapter *DP* functionality is disabled. 1 = Adapter *DP* functionality is enabled and operational.
4[b]	Multi-function Preferred	0 = No preference for multi-function. 1 = Multi-function is preferred.
5[b]	DisplayPort/ USB Configuration Request	0 = Request change to DisplayPort Configuration (if currently in USB Configuration). 1 = Request change to USB Configuration (if currently in DisplayPort Configuration).
6[b]	Exit DisplayPort Alt Mode Request	0 = Maintain the current mode. 1 = Request exit from DisplayPort Alt Mode (if currently in DisplayPort Alt Mode).
7[c]	HPD State	0 = HPD_Low. 1 = HPD_High.[d]
8[c]	IRQ_HPD	0 = IRQ_HPD has not been issued since the last status Message. 1 = IRQ_HPD.[e]
31:9	RESERVED	RESERVED (always 0000000h).

DPAM Version Resolution

Table 5-5: DPAM Version Resolution

DFP_U, Cable and UFP_U with DP SID	DFP_U	Cable	UFP_U	DPAM Version Resolution
DPAM Version	2.0 or earlier	2.0 or earlier	2.0 or earlier	2.0 or earlier[ab]
	2.1 or higher	2.0 or earlier	2.0 or earlier	2.0 or earlier[ab]
	2.0 or earlier	2.1 or higher	2.0 or earlier	2.0 or earlier[ab]
	2.0 or earlier	2.0 or earlier	2.1 or higher	2.0 or earlier[ab]
	2.1 or higher	2.1 or higher	2.0 or earlier	2.0 or earlier[ab]
	2.0 or earlier	2.1 or higher	2.1 or higher	2.0 or earlier[ab]
	2.1 or higher	2.0 or earlier	2.1 or higher	DPAM 2.1 or higher[c]
	2.1 or higher	2.1 or higher	2.1 or higher	2.1 or higher[d] (Shall support DPAM 2.1 or higher)

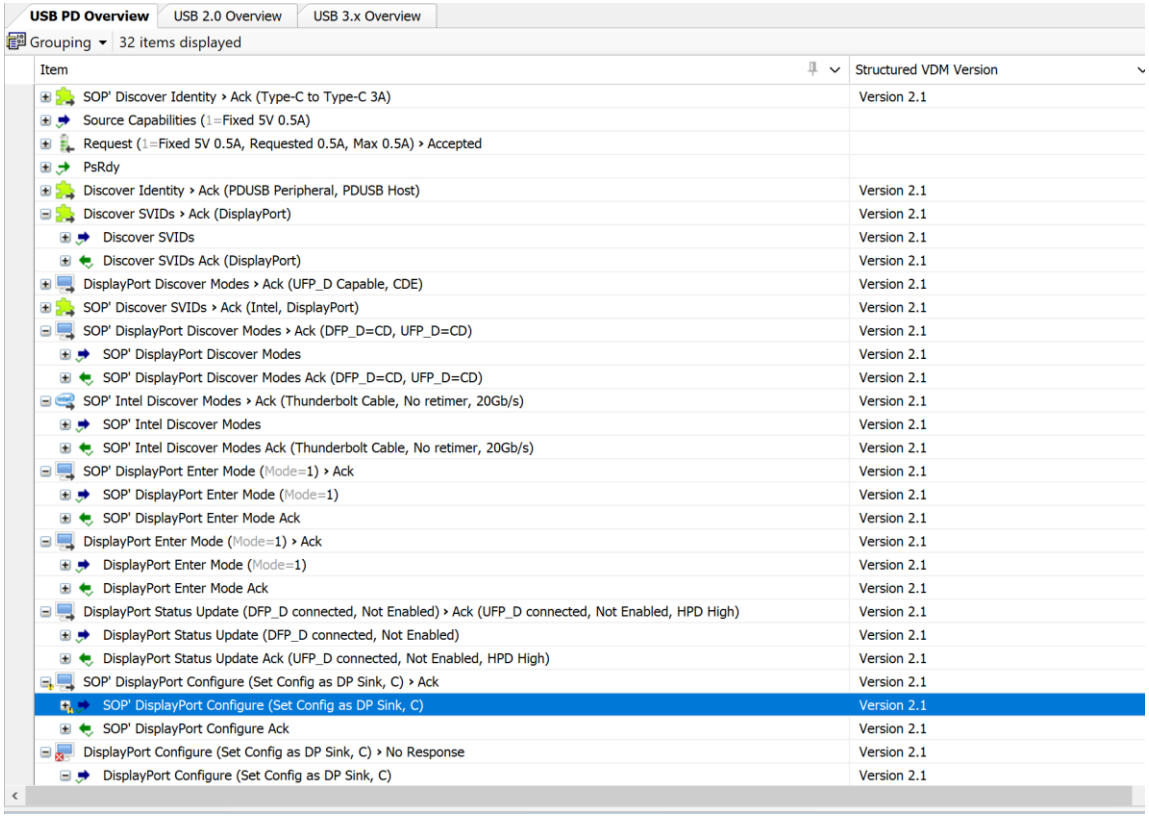
a. *If Initiator and Responder support SVDM Version 2.0 or earlier and if DisplayPort Alternate Mode is supported all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.0 or earlier.*

b. *If Initiator and Responder both support SVDM Version 2.1 or higher and if either Initiator or Responder supports DPAM Version 2.0 or earlier, then all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.0 or earlier.*

c. *When DPAM 2.1 or higher DFP_U and DPAM 2.1 or higher UFP_U are connected with a legacy active DPAM 2.0 cable, then the system shall exchange all DP Capabilities as per DisplayPort Alt Mode on USB Type-C specification 2.1 or higher but support HBR3 rates.*

d. *If Initiator and Responder both support SVDM Version 2.1 or higher and DPAM Version 2.1 all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.1 or higher.*

Typical DPAM 2.1 Flow



DisplayPort Alternate Mode 2.1a Update

- **DisplayPort Alt Mode v2.1a_SCR_on_Clarification on Device Types**
- **DisplayPort Alt Mode v2.1a_SCR_on_CableSupport**
- **DisplayPort Alt Mode v2.1a_SCR_on_Depricating DP40 Cables**
- **DisplayPort Alt Mode v2.1a_SCR_on_tAttentionToDPConfigure time**
- **DisplayPort Alt Mode v2.1a_SCR_on_mandatory PD Message support for DPAM2.1 Cables**

DisplayPort Alt Mode v2.1a_SCR_on_Clarification on Device Types

Table 5-1 USB-C and USB PD Power and Data Roles

12	USB-C-to-DP receptacle	V_{CONN}-powered accessory (Rd/Ra)	No	DFP_U and UFP_U	No Preference	Never VCONN Source
13	USB-C-to-DP cable adapter	V_{CONN}-powered accessory (Rd/Ra)	No	DFP_U and UFP_U	No Preference	Never VCONN Source

Table 5-2 USB PD Data Role Policies

Prefer UFP_U	Issue a *USB PD* ***DR_Swap*** Message to become a UFP_U If the *USB PD* ***DR_Swap*** Message is rejected, and port results in a DFP_U role, the port shall be responsible for discovering and initiating Alternate Mode entry

DisplayPort Alt Mode v2.1a_SCR_on_CableSupport

Table 5-15: DP Rates for TBTSID Capable cables

Cable Type	SVDM Version	DPAM Version	DP SID	TBT SID	TBT Alt Mode Response (see Appendix F of USB-C specification)			DP Alt Mode Response (see Table 4-5)	SOP DP Configure (see Table 5-13)	
					B25	B22	B[18:6]	B[5:2], B26 & B[29:28]	B[5:2]	B[29:28]
2,3 (See Table 2-1)	2.0	NA	No	Yes	0	0 Not Re-timer	001b, 010b or 011b	NA	001b or 010b = UHBR10 011b = UHBR20	00b
4 (See Table 2-2)	2.0	NA	No	Yes	Don't care	1 Re-timer		NA	No DP	NA

Note: If cable supports both DPSID and TBTSID, TBT VDO Bit 22 and Bit 25 can be used by the DP Source to determine the cable type (Passive, Re-driven, or Re-timed).

DisplayPort Alt Mode v2.1a_SCR_on_Depricating DP40 Cables

Reference Number in Tables 2-4	Cable Type	Minimum DP Bit-rate Capability[a]	DisplayPort Alt Mode Directionality and Main-Link Lane-count Capability[a]	Certification and Logo Applicability
1	Full-Featured Passive *USB-C USB 3.2* Gen 1 Cables (*USB-C* CC3G1-X)	HBR3[b] UHBR10[b]	Reversible 4 Lanes	*USB* certification and logo only **No VESA certification or logo**
2	Full-Featured Passive *USB-C USB 3.2* and *USB4* Gen 2 Cables and Thunderbolt Alt Mode Gen 2 Cables (*USB-C* CC3G2-X)	UHBR10 (DP54) UHBR13.5[d] (DP54)		
3	Full-Featured Passive *USB-C USB4* Gen 3 (or higher) Cables and Thunderbolt Alt Mode Gen 3 (or higher) Cables (*USB-C* CC4G3-X)	UHBR20[c] (DP80)		

DisplayPort Alt Mode v2.1a_SCR_on_tAttentionToDPConfigure time

1. Table 1-5 Glossary

Term	Definition
tAttentionToDPConfigure	Time between reception of USB PD Attention to transmission of DisplayPort Configure Message, this time is set to 500 ms. This time is applicable to DFPs in active state and functioning normally.

- **Port is a DFP_U in DisplayPort Alt Mode and DisplayPort Configuration** – Port shall change to USB Configuration by issuing an appropriate ***DisplayPort Configure*** Command to both the UFP_U and cable within *tAttentionToDPConfigure* time after receiving a *USB PD* ***Attention*** Command request with the DisplayPort/USB Configuration Request bit (bit 5) set to 1 in the ***DisplayPort Status Update*** (refer Table 5-7)
- **Port is a DFP_U in DisplayPort Alt Mode and USB Configuration** – Port shall change to an appropriate DisplayPort Configuration by issuing an appropriate ***DisplayPort Configure*** Command to both the UFP_U and cable within *tAttentionToDPConfigure* time after receiving a *USB PD* ***Attention*** Command request with the DisplayPort/USB Configuration Request bit cleared to 0 (refer Table 5-7)

DisplayPort Alt Mode v2.1a_SCR_on_mandatory PD Message support for DPAM2.1 Cables

Table 4-1: Cable eMarking Mandates

Reference Number in Tables 2-4	Cable Type	*USB PD Discover Identity*	DisplayPort Alt Mode *USB PD* Commands
1	Full-Featured Passive *USB-C USB 3.2* Gen 1 Cables (*USB-C* CC3G1-X)	Mandatory	Not Allowed
6	Captive Cable with *USB-C* connector	Mandatory When the DP Sink supports UHBR rates	**Optional** When the DP Sink supports HBR rates

DPAM 2.1 CTS Update - 1

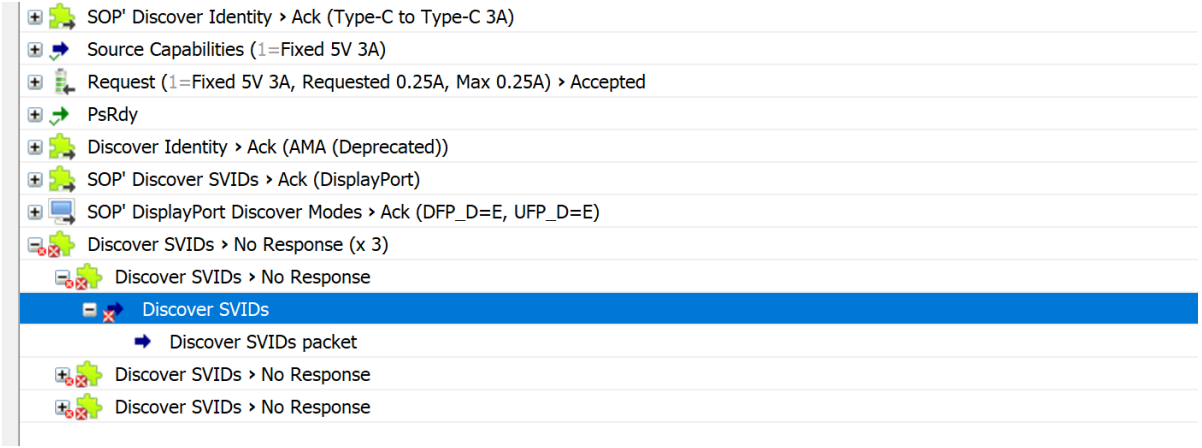
- 10.3.2 DPAM2.1 Entry with USB-C to USB-C non-emarked cable
- 10.3.3 DPAM2.1 Entry with USB-C to USB-C Passive TBT3 cable
- 10.3.4 DPAM2.1 Entry with Passive E-Marked USB-C to USB-C
- 10.3.5 DPAM2.1 Entry with USB-C to USB-C DP2.0 LRD Cable
- 10.3.6 DPAM2.1 Entry with USB-C to USB-C DP2.0 Active Retimer cable
- 10.3.7 DPAM2.1 Entry with USB-C to USB-C DP2.1 LRD cable
- 10.3.8 DPAM2.1 Entry with USB-C to USB-C Active Non-DP cable
- 10.3.9 DPAM2.1 Entry with USB-C to USB-C USB2.0 cable
- 10.3.10 DPAM2.1 Entry with USB-C to DP2.1 cable

- Make sure the DFP_U set correct cable information in DisplayPort Configurations VDO
- 10.3.5 and 10.3.6 Using TBT info is now optional (was mandatory)

DPAM 2.1 CTS Update - 2

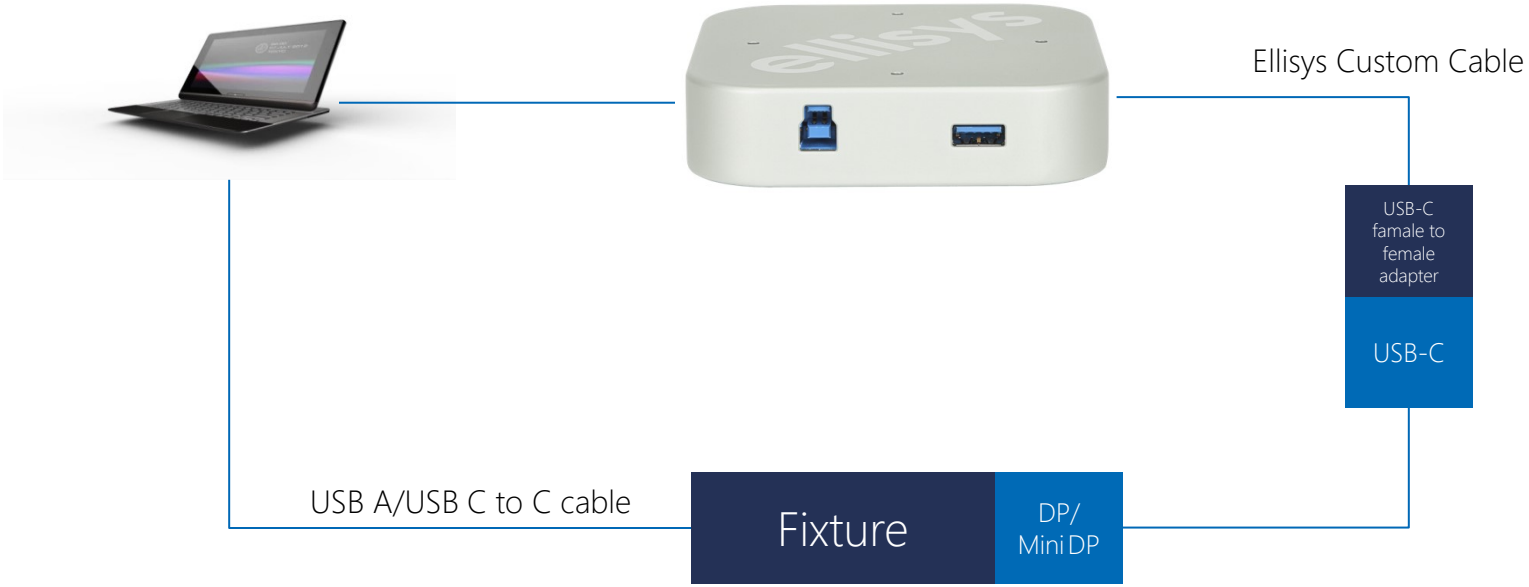
- **DPAM Version Resolution Tests**
  - **10.3.23 DPAM Version 2.1 DFP_U Connected to DPAM Version 2.0 or 2.1 UFP_U**
  - **10.4.3 DPAM Version 2.1 Cable Connected to DPAM Version 2.0 or 2.1 DFP_U**
  - **10.2.8 DPAM Version 2.1 UFP_U Connected to DPAM Version 2.0 or 2.1 DFP_U**

- **10.2.9 DPAM Discovery Interoperability Flow for UFPs**



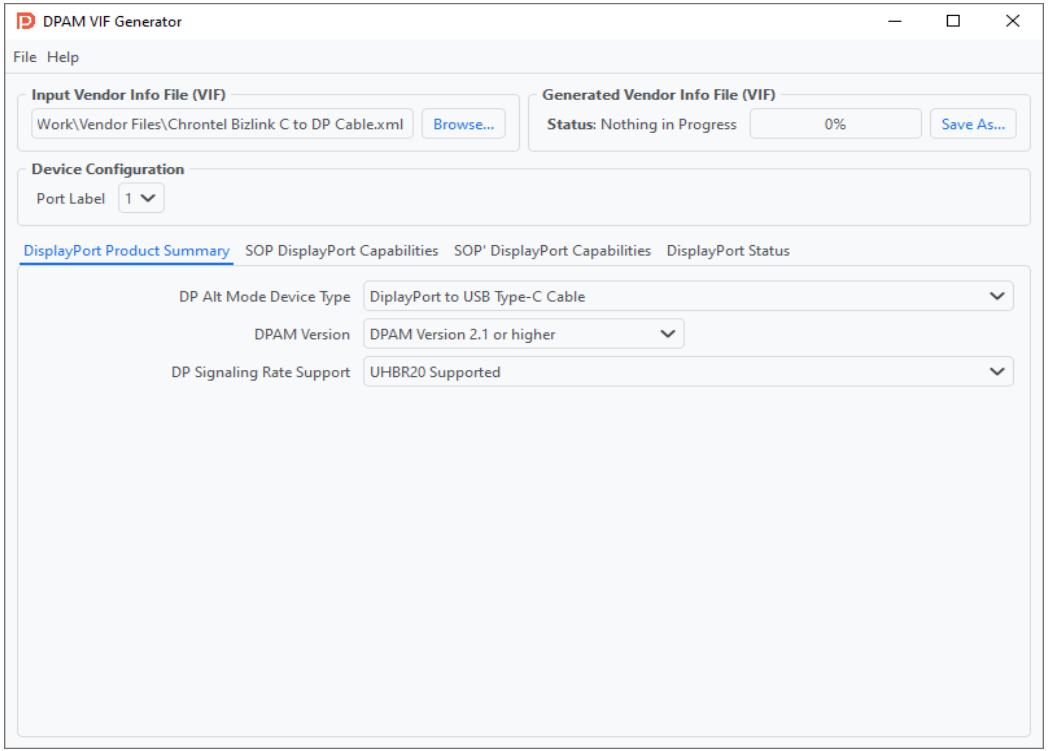
DPAM 2.1 CTS Update - 3

- **C to DP Adapter tests automation**



DPAM 2.1 CTS Update - 4

- **VESA VIF TOOL**



VESA

Questions?

VESA® DisplayPort®

DP LRD Active Cable Testing Challenges and DP2.1 Connector Certification

Lexus Lee

Allion Labs,Inc

2025/05/23

Overview

- VESA LRD Active Cable Testing Challenges
- VESA Enhanced Connector Compliance Test Introduction

Overview

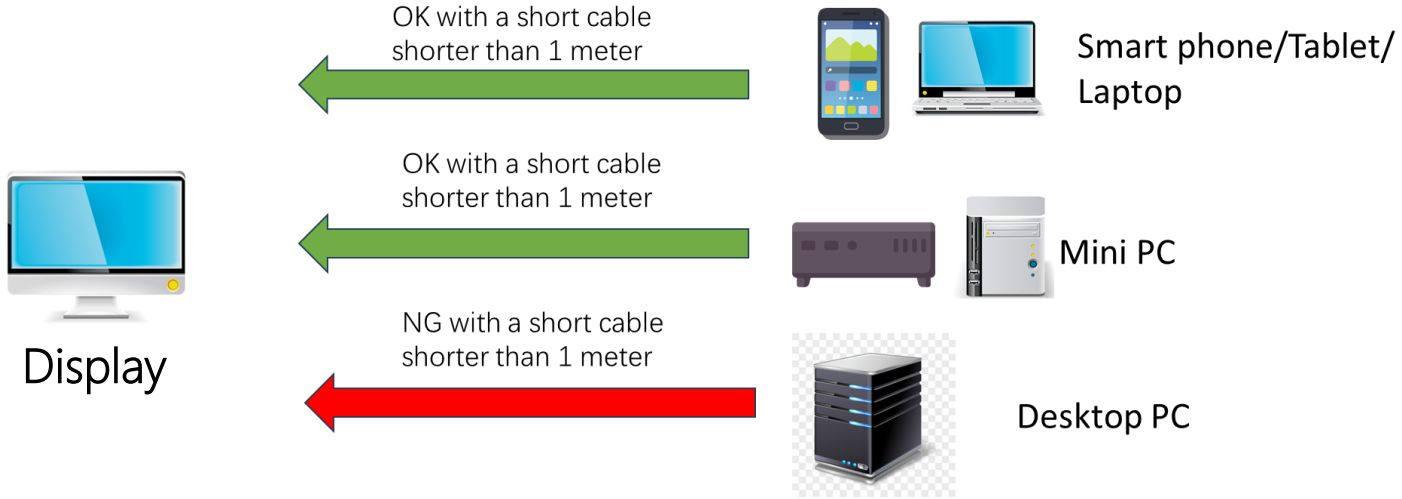
- VESA LRD Active Cable Testing Challenges
- VESA Enhanced Connector Compliance Test Introduction

The Current UHBR Passive Cable Status

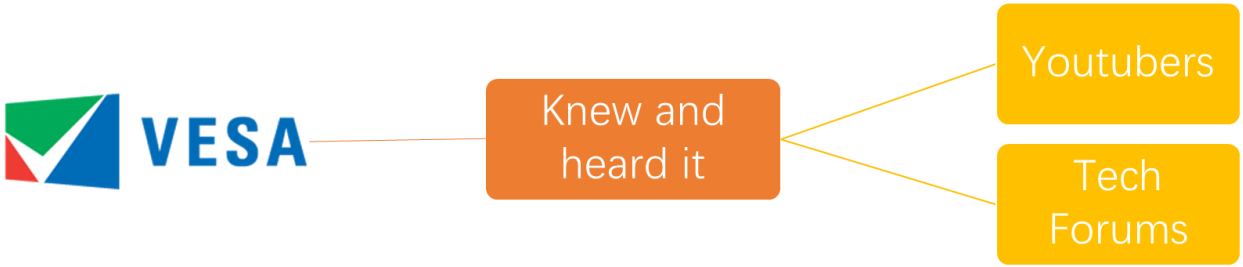
- DP to DP and USB-C to DP Passive cables for UHBR transmission
  - According to DP2.1a spec
    - UHBR 20-Capable Passive cable length: around 1 meter
    - UHBR 13.5-Capable Passive cable length: around 2 meters

- Criticism of UHBR20 ecosystem from youtubers and tech forums.

The Current UHBR Passive Cable Status Cont’



DisplayPort LRD Active Cable Solution

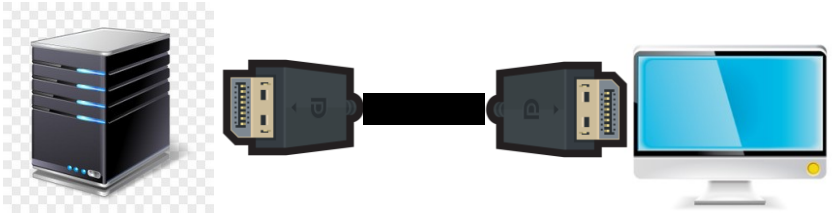


- VESA has brought us a solution to the criticism.
  - LRD Active Cable Solution
    - Get UHBR20 transmission to successfully work longer than 2 meter-long cable.
    - Creating a LRD Active Cable CTS

CTS Testing Challenges

- Knowledge to get DP LRD cable to work up
  - AUX and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Aux P: Pull down to GND
2. Aux N: Pull high to 2.89~3.6V.
3. DP_PWR:2.89~3.6V
4. Aux transaction if needed

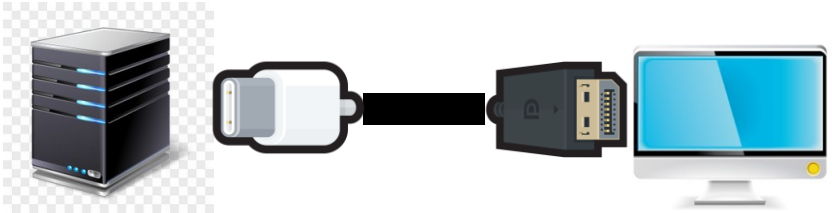


1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull high to 2.25~3.6V
5. Aux transaction if needed

CTS Testing Challenges Cont’

- Knowledge to get C to DP LRD cable to work up
  - Vconn, AUX, and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Vconn:3.0~5.5V
2. DP alt mode exerciser if needed.
3. Aux circuitry if needed.
4. Aux transaction if needed



1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull High to 2.25~3.6V
5. Aux transaction if needed

CTS Testing Challenges Cont’

- Power Consumption Check Before You Start Any Test
  - Do Link Training for
    - 1 Lane
    - 2 Lanes
    - 4 Lanes
  - Observe the current change of Vconn or DP PWR.
    - For example

	1 Lane	2 Lanes	4 Lanes
Current	80mA	170mA	380mA

CTS Testing Challenges Cont’

- Check How to Power up the LRD Cable Before You do Inrush Current Test
  - Supplying power to one end of a cable DUT ?
  - Supplying power to both ends of a cable DUT ?

	One End _Case	Both Ends_Case	Both Ends_but no power line used to connect the two LRD ICs.
Consuming Current	380 mA	190 mA	190mA

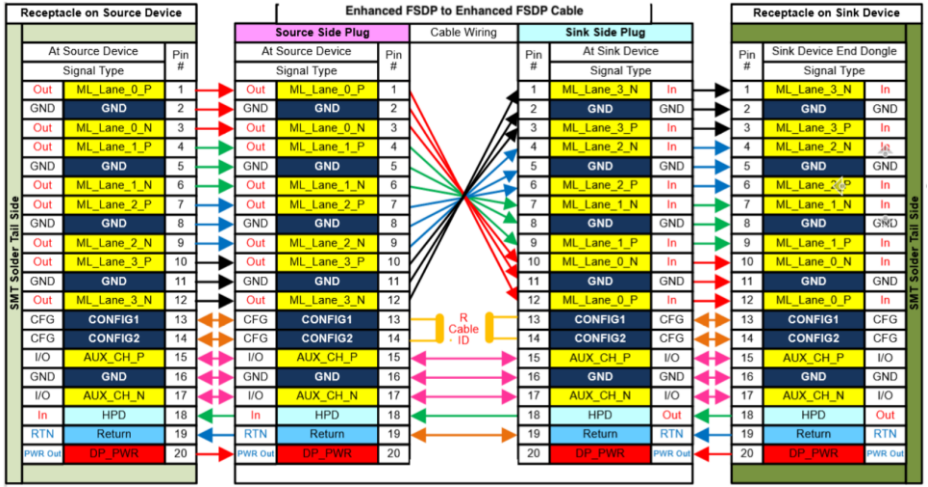
CTS Testing Challenges Cont’

- Why it matters
  - In order to get Maximum Inrush Current Energy

	One End _Case	Both Ends_Case	Both Ends_but no power line used to connect the two LRD ICs.
Measured Inrush Current Energy	4 mJ (wanted)	2 mJ (NOT wanted)	2 mJ (wanted)

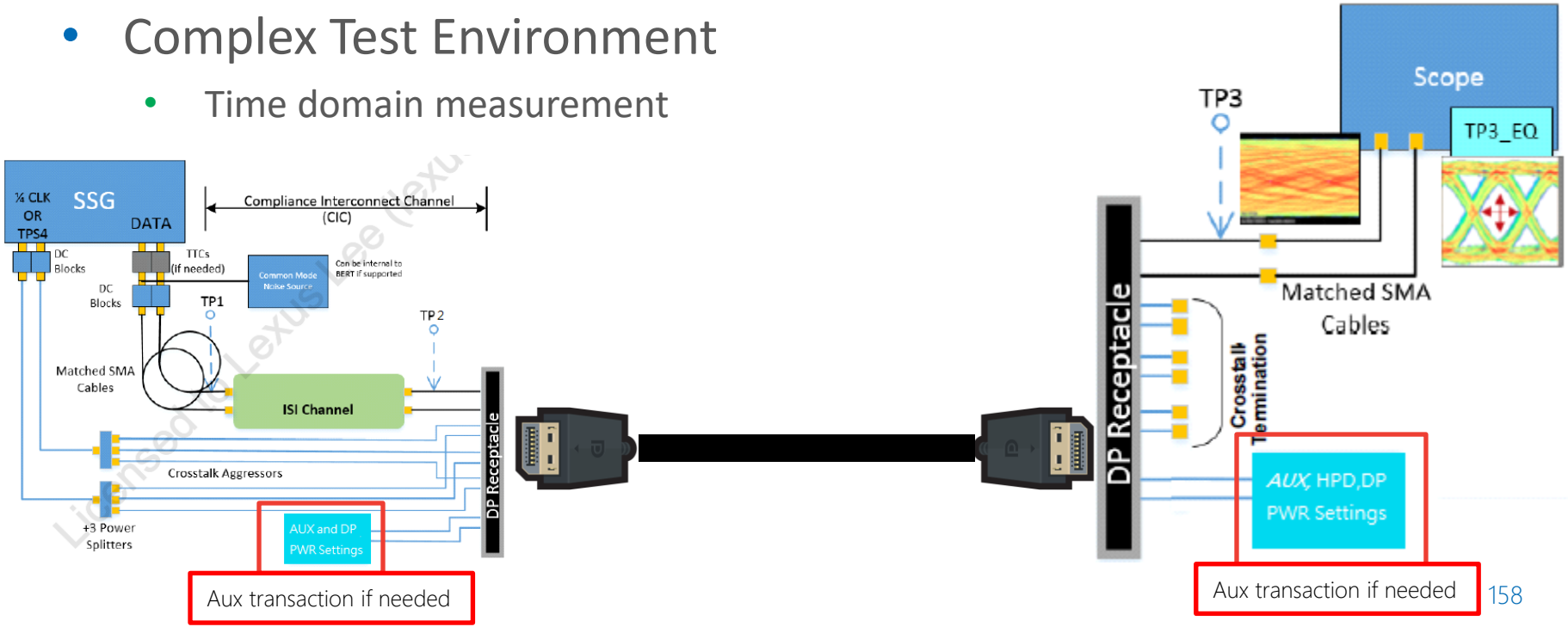
CTS Testing Challenges Cont’

- Know how the wires inside a DP cable are connected at both ends.
  - Look at high speed pairs, please



CTS Testing Challenges Cont’

- Complex Test Environment
  - Time domain measurement

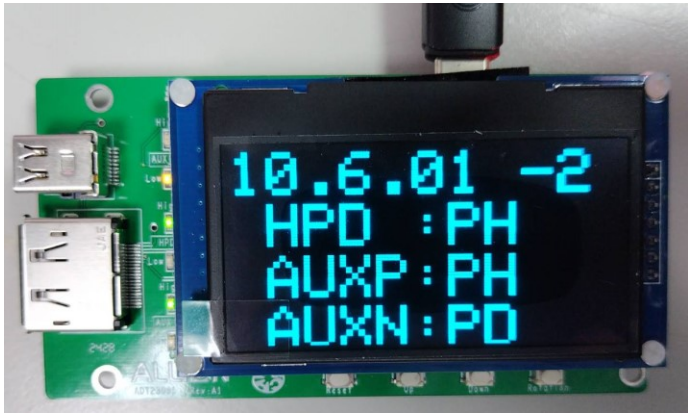


CTS Testing Challenges Cont’

- Complex Test Environment
  - Frequency domain measurement

CTS Testing Challenges Cont’

- Allion Test Fixture
  - Help to reduce the complex connection for your LRD cable testing.
    - Powered by USB-C port
    - Controllable HPD, AUX_P, and AUX_N

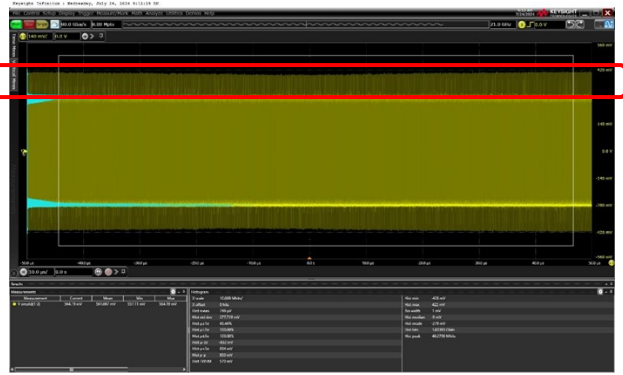


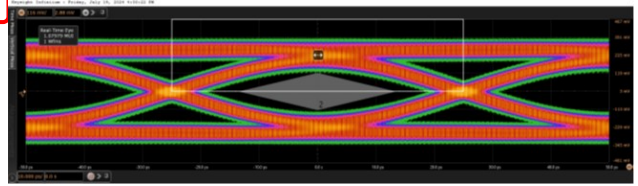
CTS Testing Challenges Cont’

- Stressed Signal Generator
  - Preset Calibration
    - Very important to stressed signal defined by DP spec.
    - Inaccurate preset number gets your stressed signal to highly not meet the expected ISI jitter, Eye Height, and Eye width.

Table 3-57: Preset FFE Coefficients[a] [b]

Preset Configuration #	Preshoot (dB)	De-emphasis (dB)	Informative Filter Coefficients		
			C_{-1}	C_0	C_{+1}
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0

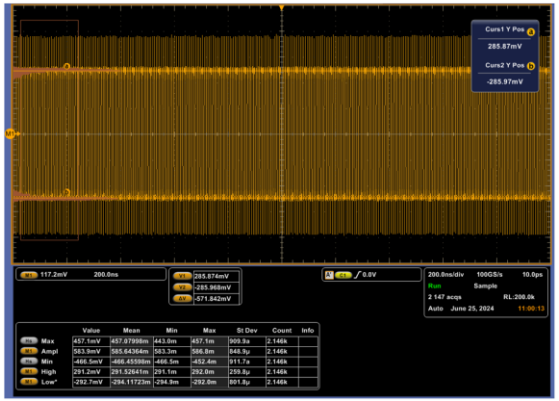


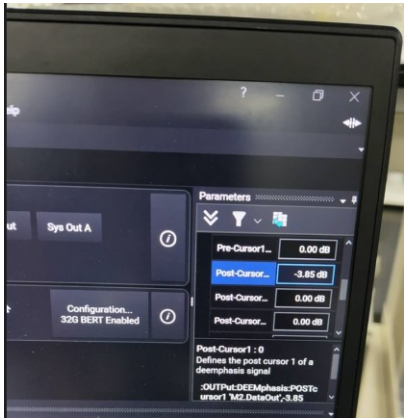


CTS Testing Challenges Cont’

- Stressed Signal Generator Cont’
  - Preset Calibration Cont’
    - Do not just enter the number that you want into your SSG FFE setting.

(SQ128) Rough De-emphasis: 20 log(585.6/923.4)=-3.95dB





Overview

- VESA LRD Active Cable Testing Challenges
- VESA Enhanced Connector Compliance Test Introduction

Latest DisplayPort Connector Spec Cont'

- Connector Types:

Type	Definition
Legacy	• Supports up to 8.1Gbps/lane(HBR3) • Includes both an fsDP and an mDP version
Enhanced	• Enhanced fsDP Type 1 connector supports up to 13.5Gbps/lane(UHBR13.5) • Enhanced fsDP Type 2 connector supports up to 20Gbps/lane(UHBR20) • Enhanced mDP connector supports up to 20Gbps/lane(UHBR20)

Latest DisplayPort Connector Spec Cont'

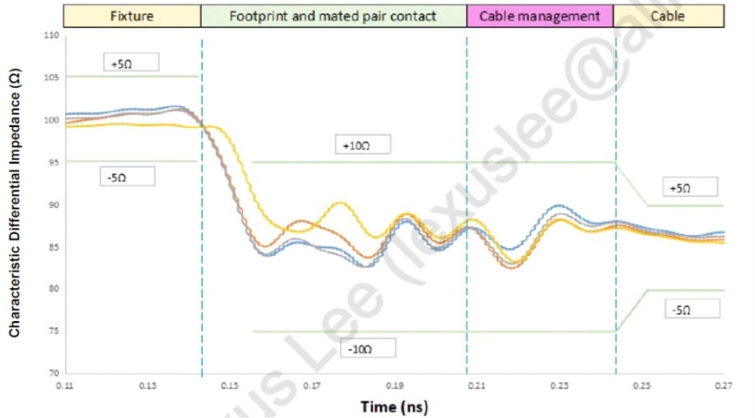
- Footprint Compatibility Matrix:

fsDP Conn/Footprint Type	Legacy PCB Footprint	Enhanced PCB Footprint Type 1	Enhanced PCB Footprint Type 2
Legacy	OK with HBR3	OK with HBR3	Ok with HBR3
Enhanced Type 1	N/A	OK with UHBR13.5	N/A
Enhanced Type 2	N/A	N/A	OK with UHBR20

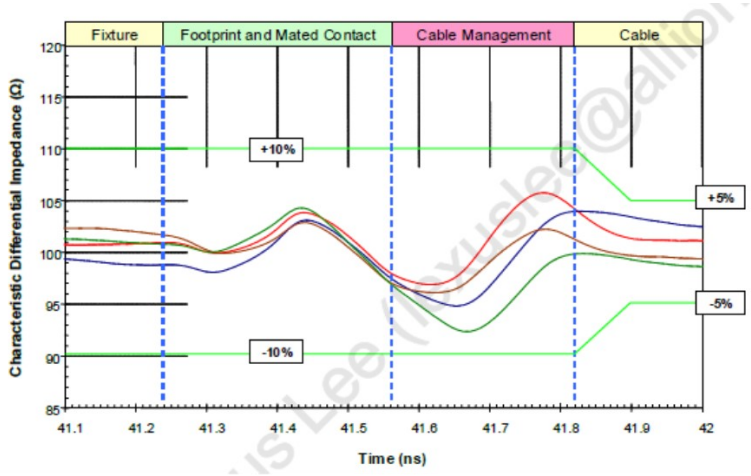
mDP Conn/Footprint Type	Legacy PCB Footprint	Enhanced PCB Footprint
Legacy	OK with HBR3	N/A
Enhanced	N/A	OK with UHBR20

Latest DisplayPort Connector Spec Cont'

- Discrepancy of Impedance:



Enhanced DP/mDP Connector

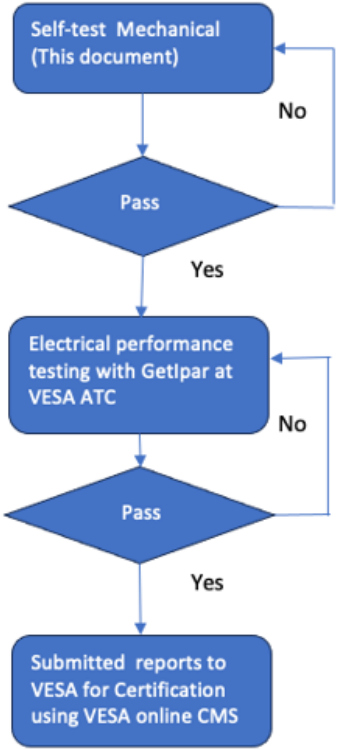


Legacy fsDP Connector

DP Enhanced Connector Compliance program

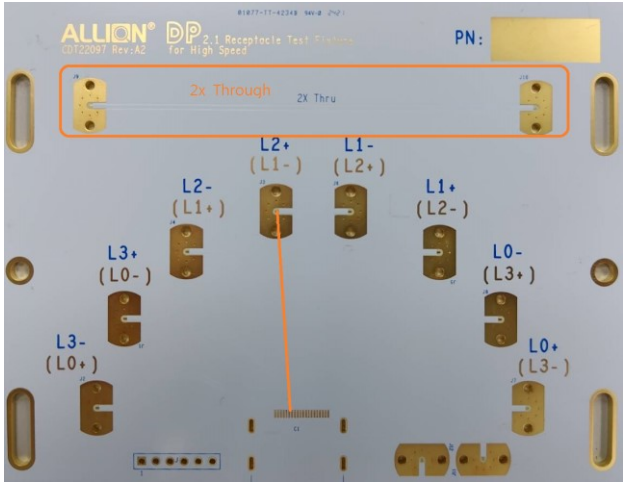
- Certification Flow:

VESA® DisplayPort™ Self-Test Report for Connectors
v2.1



DP Enhanced Connector Compliance Program Cont'

- Test Fixture Check:
  - Intra-pair skew < or = 2ps
  - 1x&2x thru accuracy check
    - (2x through length)/2 < or = 1x through length
    - In order to avoid compensating too much.



DP Enhanced Connector Compliance Program Cont'

- Test Concept:
  - Test the Connector DUT with a certified cable
    - Pass/ Fail Criteria based on the "cable" requirement defined in the DP2.1a spec.
  - Test the certified cable with one of the Known Good Receptacle fixtures(KGF)
    - KGF1 and KGF2 are Bizlink and Wieson respectively
    - Test data submitted as a reference

Thank you

Break

DPM Workgroup Review

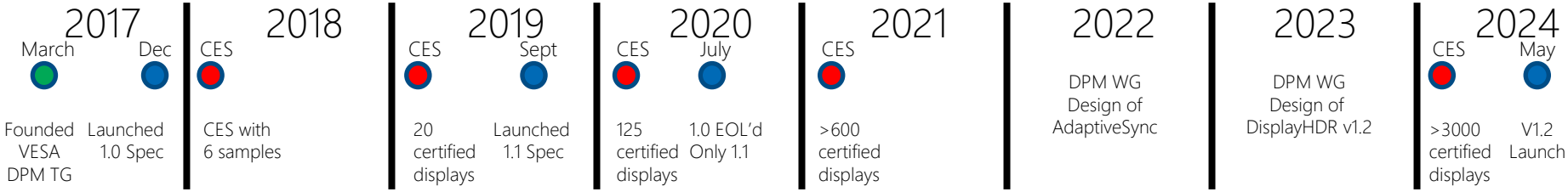
Roland Wooster: wooster@intel.com

Intel

May 2025

DisplayHDR v1.2

DisplayHDR – Timeline



- Surpassed 3000 certifications on DisplayHDR standard in 2023
- Averaging over 100 new certifications per month for DisplayHDR
- v1.2 is our most significant update to the standard since v1.0

DisplayHDR 1.2 Summary Changes

Test Tightening & Refinement

- Replaced the black background
- Color Gamut Increases
- Bit Depth Increases
- Precision & range of White Point

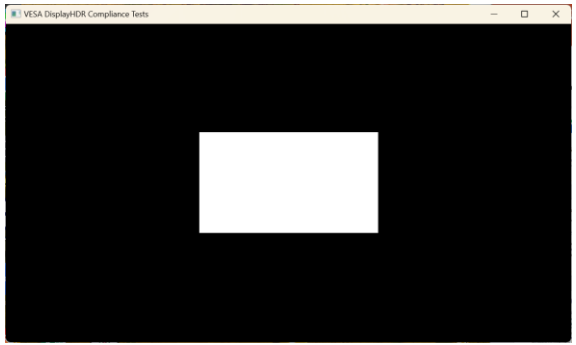
New Tests

- Static Contrast Ratio
- HDR Color Accuracy
- HDR vs SDR Black Level
- Black Crush
- Subtitle Flicker

VESA will continue to allow products to be certified under DisplayHDR v1.1 only through the end of May 2025 for monitors, and May 2026 for laptops, to allow for products already in development that have been designed to meet the previous spec

Replacing the Black Background

- We have replaced the black background with a “star field” pattern, with peak luminance of 100 cd/m2, and changed the test patch to an 8% square
- Designed to not change the Average Pixel Level (APL) from 10% on emissive screens, while switching on “all” of the backlight zones for local dimming in a better representation of normal usage



Color Gamut & Bit Depth Increases

- Bit Depth Requirement is now 8+2 at the DriverIC across the board
  - Previously VESA had allowed 8bit only w/o FRC for DisplayHDR 400 tier
- Color gamut for DisplayHDR 400 is elevated to 99% of sRGB and 90% of DCI-P3
  - Same requirement as the previous spec version (v1.1) for DisplayHDR 1000 tier
- Color gamut for DisplayHDR 500-1000 is elevated to 95% of DCI-P3
  - Same requirement as the previous spec version (v1.1) for DisplayHDR 1400 tier

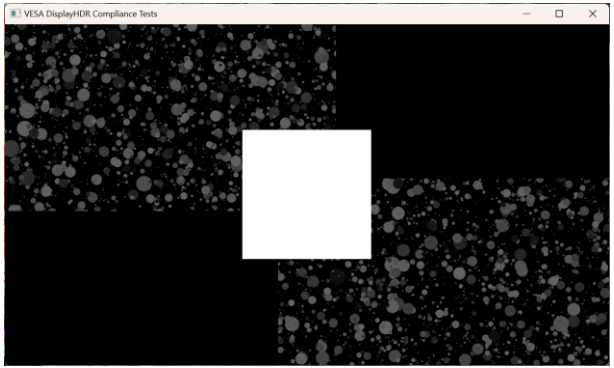
Luminance & White Point Accuracy

- V1.1 Test Range was from 5 cd/m^2 to 50% of Tier Level
- V1.2 increases the range ~10x: from 1 cd/m^2 to ~100% of Tier Level
- Delta-ITP requirements significantly tightened for all of the Luminance and White Point Accuracy tests at 15cd/m^2 and higher, some by as much as a third, going from a Delta-ITP tolerance of 15 down to 10

New: Static Contrast Ratio

- V1.2 introduces single image contrast ratio requirements using test patterns that ensure higher performance at DisplayHDR 400, at least 1D dimming for DisplayHDR 500 and 600, and 2D dimming for DisplayHDR 1000 and above

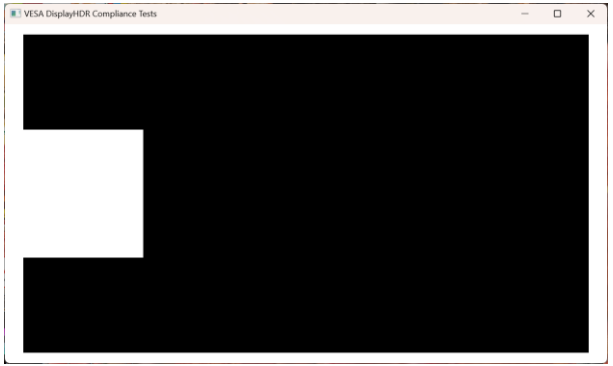
1D Pattern: DisplayHDR 400-600



Starfields are 30% of screen suitable for both 1D & 1.5D

Tier Level	CR
400	1300:1
500	7000:1
600	8000:1
1000	30K:1
1400	50K:1

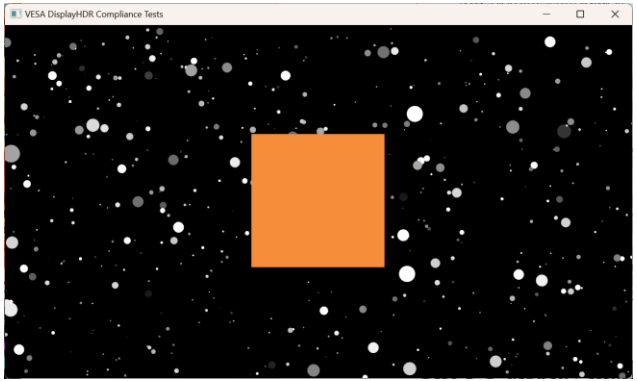
2D Pattern: DisplayHDR 1000+



Note the white border around the Four edges of the image. Requires 2D.

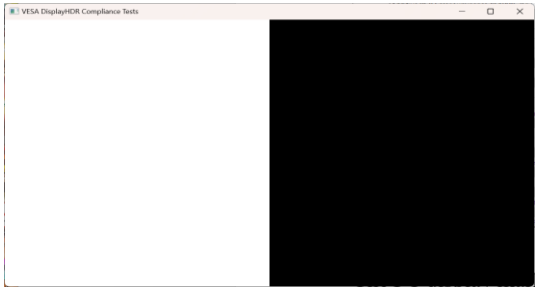
New: Color Accuracy Tests – Xrite ColorChecker SV

- V1.2 adds a huge HDR color accuracy test – almost 300 patches!
  - SDR systems typically measure using Delta-E (100 cd/m^2 white level)
  - HDR needs to measure at multiple luminance levels
- V1.2 tests 96 color patches at each of 50, 100, and 50% of Tier Level
  - We calculate the average Delta-TP for each of the three luminance sets of 96 colors. Each set must average less than the max Delta-TP tolerance for the tier level being tested. E.g. <6 Delta-TP for DisplayHDR 1000
- V1.2 uses the new starfield background
  - To ensure the backlight is on across the screen



New: HDR vs. SDR Black Level Test

- VESA has often found that HDR displays, while displaying SDR content with the OS in HDR mode, exhibit an elevated black level versus the same SDR content in SDR mode with the same white level
- Representing “an SDR app”, DisplayHDR v1.2 uses a 200 cd/m^2 white and black patch
- This simply compares the contrast ratio between white and black with the OS in both SDR and HDR mode to check that the black level is not elevated in HDR mode



New: Black Crush Test

- Dark black is great, but so are shadow details
- This test is designed to ensure the display is not crushing shadows to black
- Five full screen luminance tests at the following luminance levels:
  - 0, 0.05, 0.1, 0.3, 0.5 cd/m2
- V1.2 ensures that all five levels are distinguishable and that they haven't all been crushed to the same "zero level" (e.g. black + light leakage)
  - Note that this is a crush test, seeking 5 distinguished levels, not used to evaluate luminance accuracy.
- V1.2 also ensures that the levels increase from step to step

New: Subtitle Flicker Test

- This test was developed to ensure that suitable local dimming occurs that correctly manages both the backlight and LCD transparency in a local dimming solution to ensure minimum luminance flicker as the backlight needs to adjust for dramatic changes in luminance level
- The test uses a 10 cd/m2 grey patch and grey star field
- The subtitles are 100 cd/m2
- Subtitles appear and disappear
- Tolerance for the grey patch variance
- 13% for DisplayHDR 400-600
- 10% for DisplayHDR 1000+ & all True Black Tiers

AdaptiveSync v1.1a

AdaptiveSync – Timeline

- Over 250 Certified Displays in the first 3 years!
- DualMode adoption has been great – lots of consumer excitement

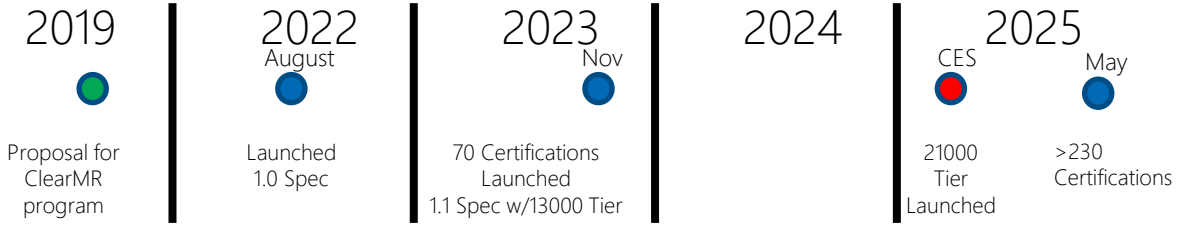
Program Background

- Designed to certify displays, using the open Adaptive Sync protocol of DisplayPort meet minimum requirements on:
- Primary focus: Flicker, Jitter, & frame rate ranges
- Also sub-logo program for MediaSync (video vs gaming)
- Most exciting technology is now “Dual Mode” – a single display that is optimized both for Content Creation with high resolution, and Gaming with high frame rate.

VESA

ClearMR v1.1

ClearMR – Timeline



- Over 230 Certified Displays in just under 3 years
- Other than updating for new performance tiers, and improving the testing process with v1.1 CTS, the standard has remained very stable with no end-user facing version updates.

Program Background

- A new standard to measure motion blur under rigorous and standardized testing procedures.
- Designed to replace MPRT and G2G standards which can easily be manipulated with excessive overdrive or temperature.

DPM Workgroup 2025

Work in progress

DPM's 2025 Activities – SCRs & New Logo Usage

- Released minor update to TrueBlack-1000 spec to support product releases at CES this year.
  - TrueBlack-1000 laptops now in retail.
- Expanded DisplayHDR logo usage to Measurement Devices that have been confirmed as suitable for DisplayHDR measurement.
- Expanding AdaptiveSync logo usage for TVs (HDMI displays) – SCR is WIP and not yet submitted.

DPM 2025

- VESA Certification Recognition in Windows
  - Microsoft, OEM INF registration method shared with VESA members
- DisplayHDR transitions from v1.1 to 1.2 at the end of May for monitors. Laptops have 1 more year.
- There has been interest raised by OEMs and a Test House to update DisplayHDR CTS to support AR/VR displays

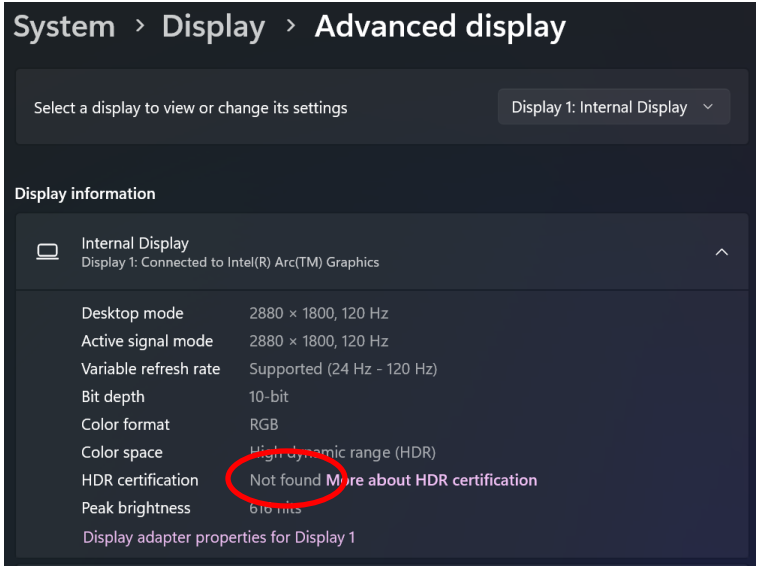
DisplayHDR - Pro

- Interest has been raised for development of a "DisplayHDR-Pro" variant of the DisplayHDR logo
- Content Creator / Pro level specs
- Higher performance specs / calibration / reflectivity
- Potentially the "Pro" logo could be an additional logo/modifier to the existing DisplayHDR / TrueBlack logos rather than a replacement, i.e. 2nd logo in addition.

Backup

HDR Certification listing in Windows

- Microsoft have an existing Manufacturer INF file creation process for OEMs
- Documentation at Partner Center: https://partner.microsoft.com/en-us/dashboard/collaborate/packages/16638

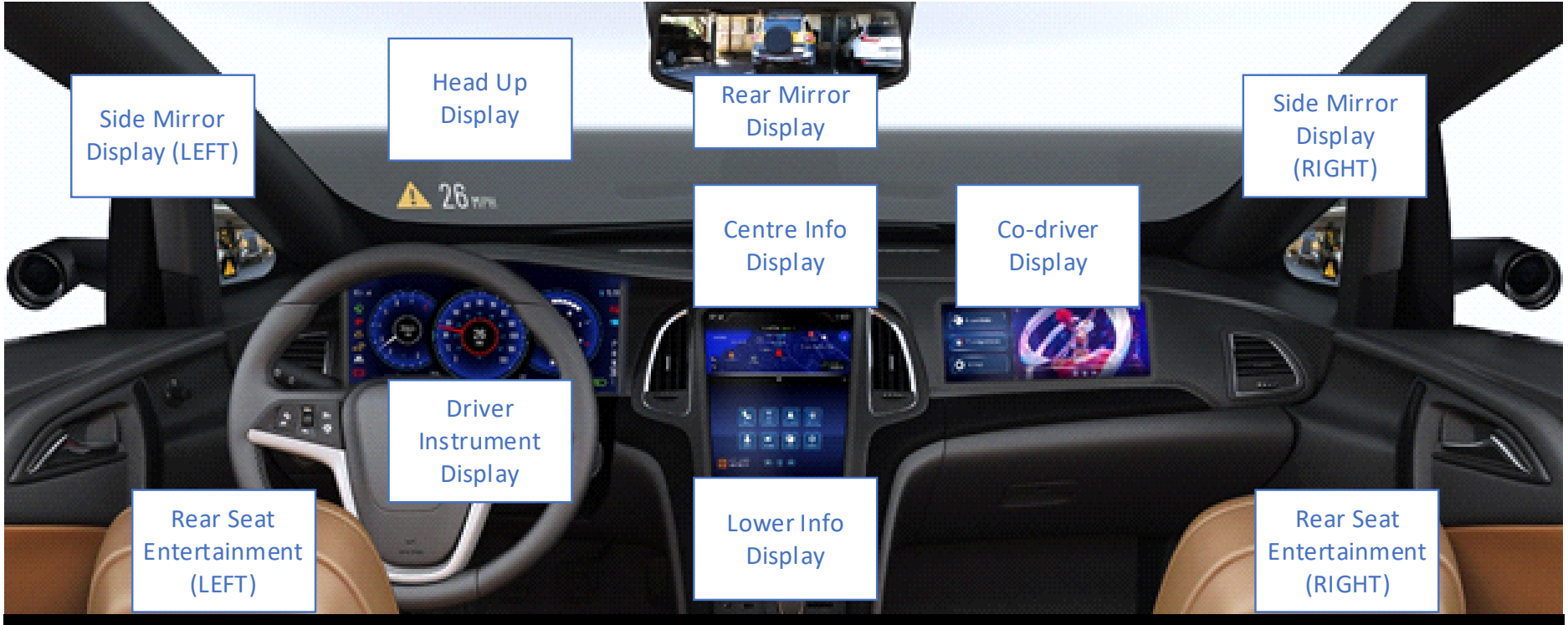


Introduction to VESA DisplayPort Automotive Extensions

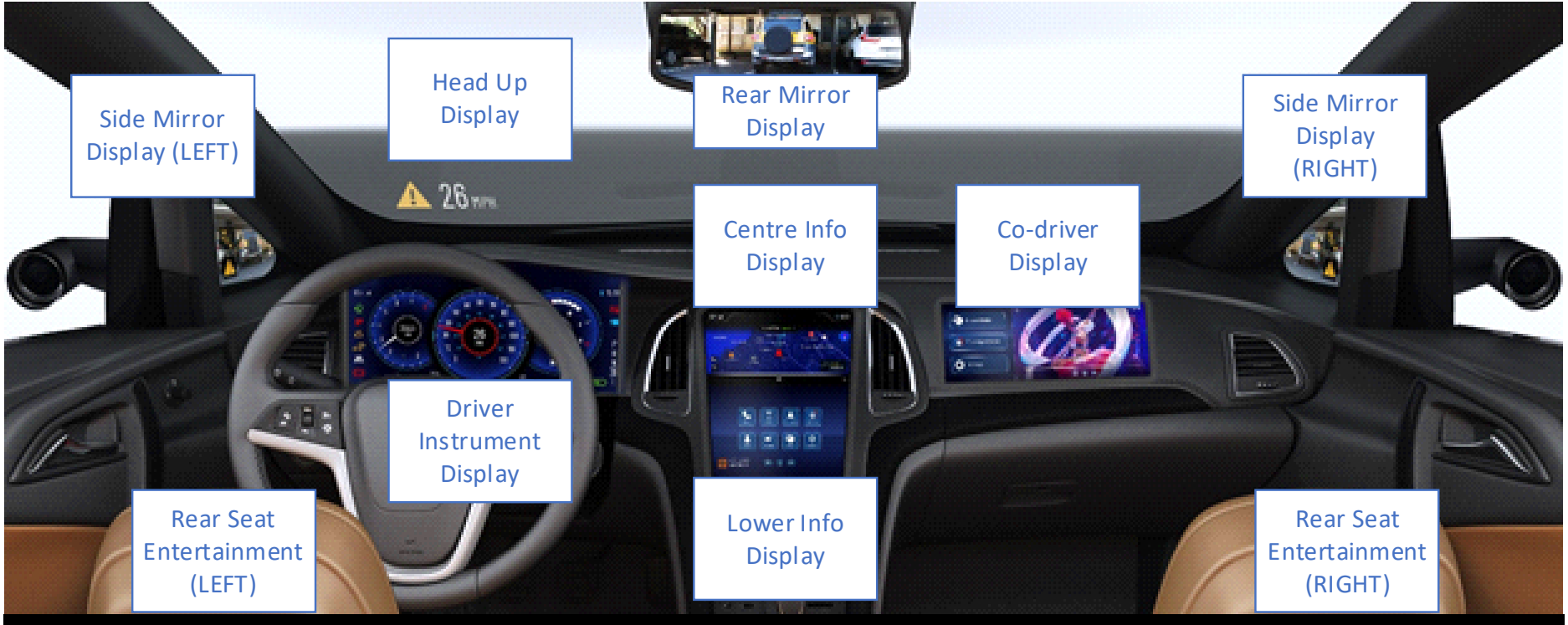
James Goel
DisplayPort Auto Extensions Sub-Group Chair
VESA Board Member

Tung-Sheng Lin
Senior Technical Manager
MediaTek Inc.

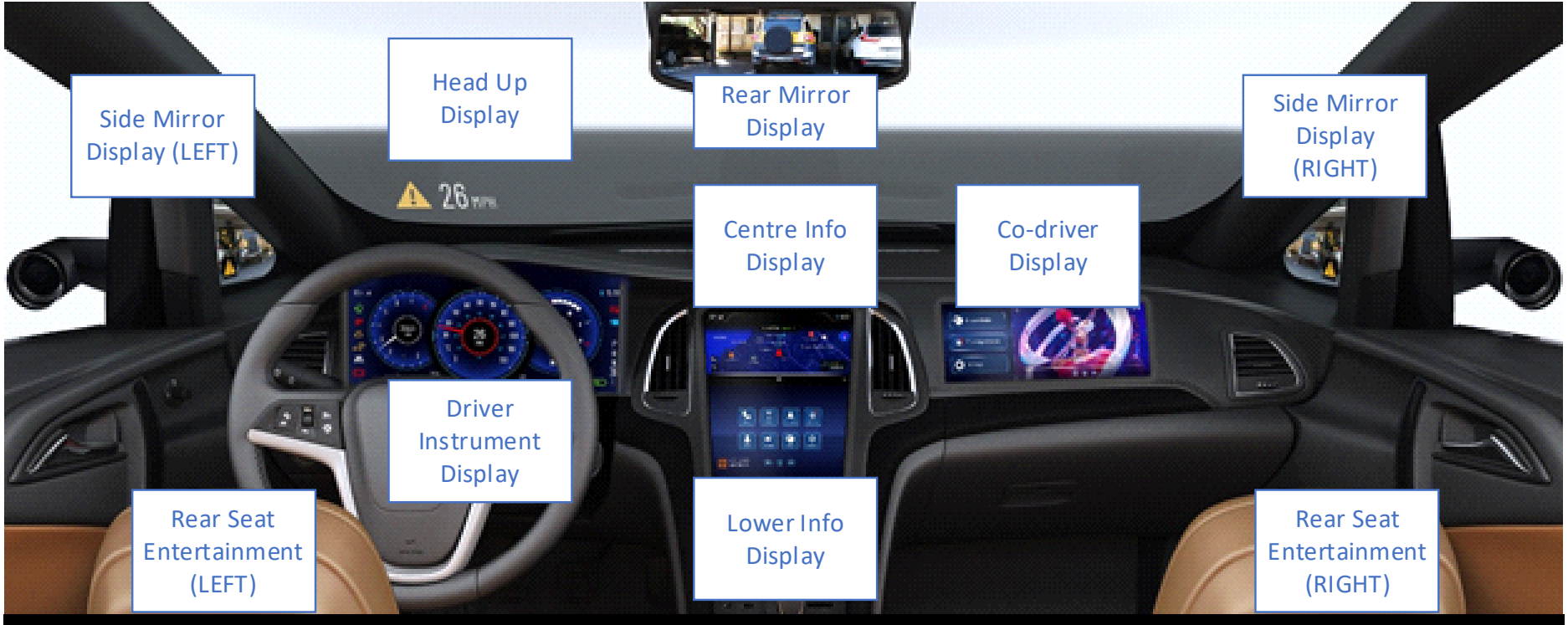

Side Mirror Display (LEFT)
Head Up Display
Rear Mirror Display
Side Mirror Display (RIGHT)
Centre Info Display
Co-driver Display
Driver Instrument Display
Rear Seat Entertainment (LEFT)
Lower Info Display
Rear Seat Entertainment (RIGHT)
GAME OVER



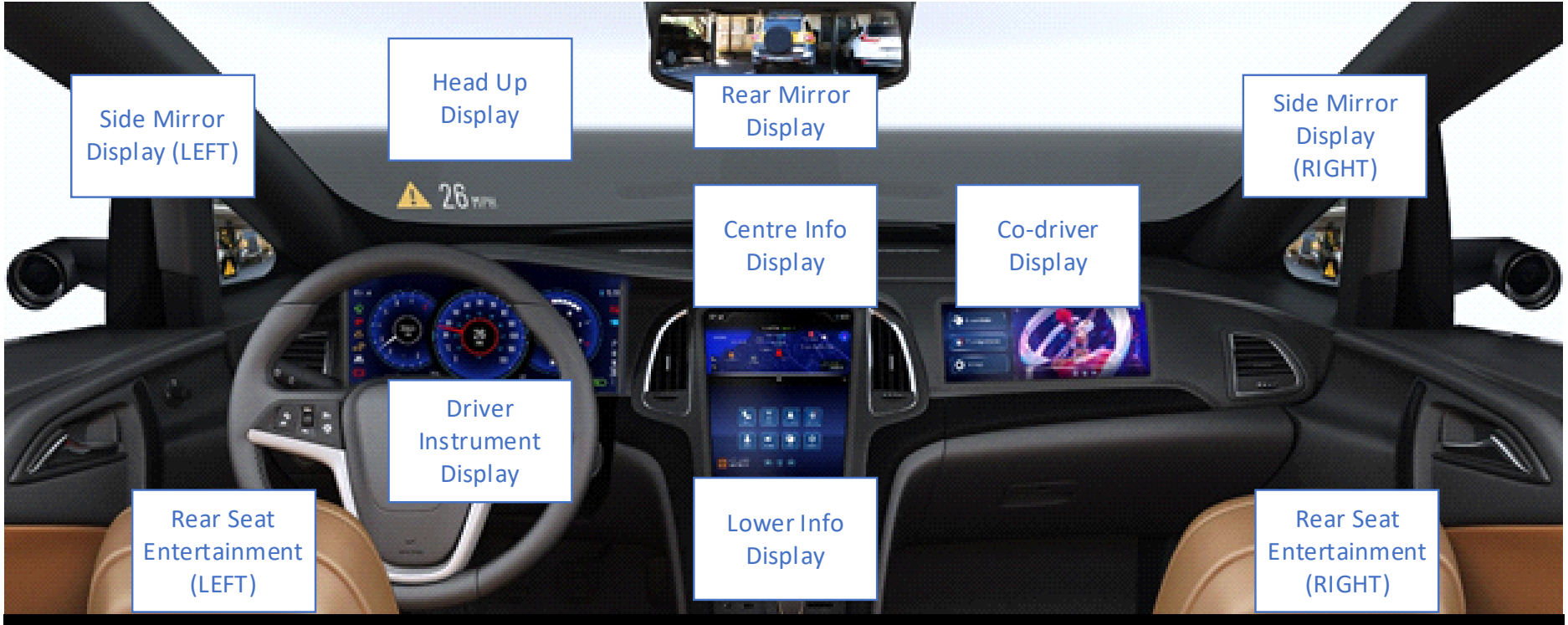
- Instrument clusters, HUDs, mirrors, and rear-seat entertainment.



- Instrument clusters, HUDs, mirrors, and rear-seat entertainment
- ASIL-D safety, UN155 and ISO 21434 security may be required



- Instrument clusters, HUDs, mirrors, and rear-seat entertainment
- ASIL-D safety, UN155 and ISO 21434 security may be required
- Existing DP/eDP protocols were not built with these challenges in mind.



- Instrument clusters, HUDs, mirrors, and rear-seat entertainment
- ASIL-D safety, UN155 and ISO 21434 security may be required
- Existing DP/eDP protocols were not built with these challenges in mind.
- Forcing OEMs into fragmented, non-standard solutions.

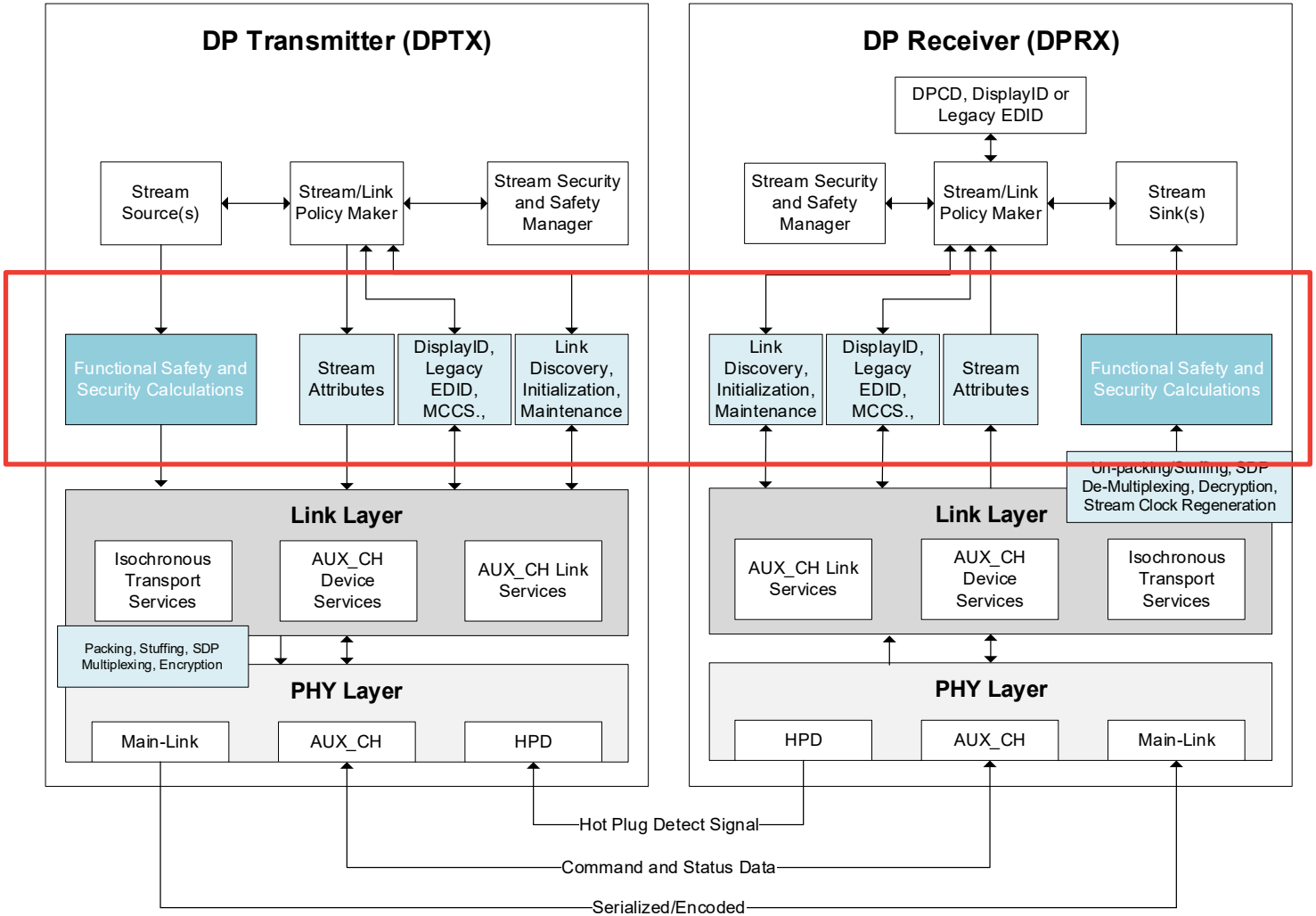

62 °F
12:30
AUTO
SRS AIRBAG
2550
RPM
26
MPH
KM/H
FUEL RANGE
278
MILES
E
F
H
C
MAINT REQD
P
R
N
D
L
TRIP A
1508 mi
22360 mi

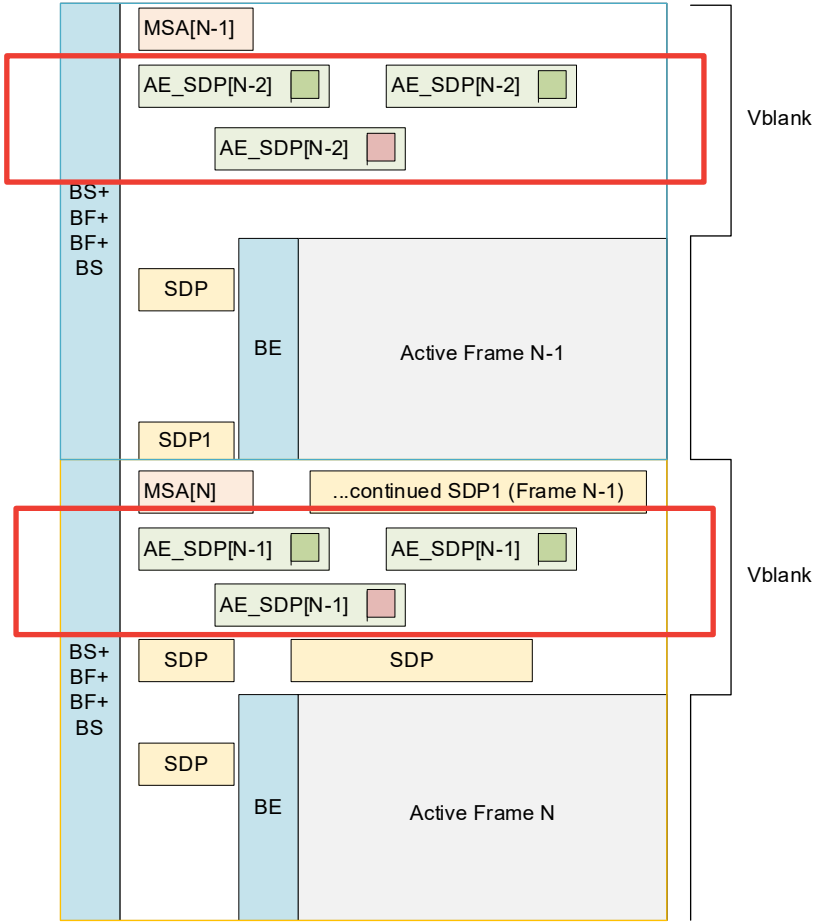
- Entire video frame protected by Cyclic-Redundancy-Check Codes
- Additional Automotive grade Security (DMTF SPDM, MAC, DP AUX Encryption) avail
- Important Regions-of-Interest protected with Cyclic-Redundancy-Check Codes

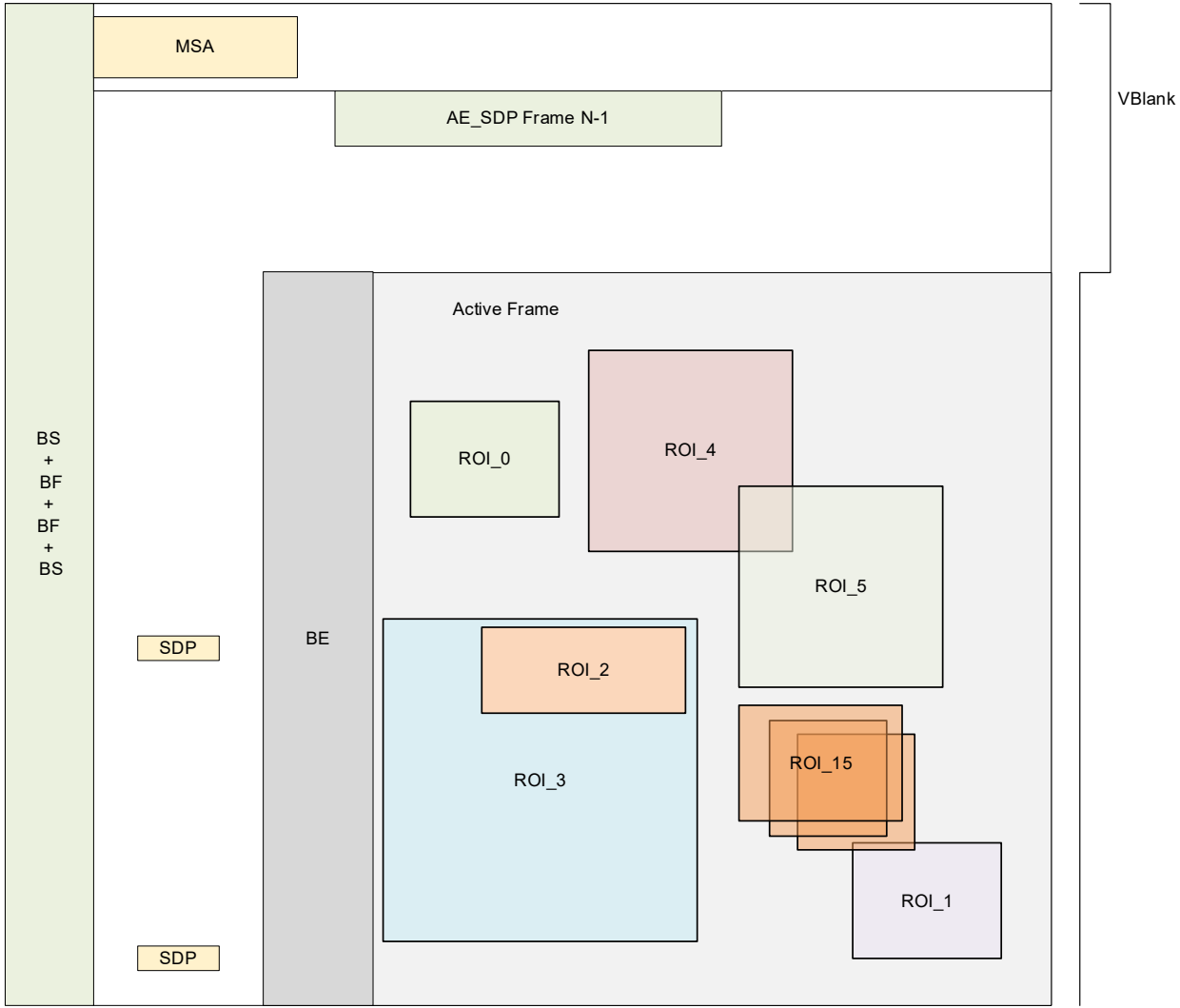
- Entire video frame protected by Cyclic-Redundancy-Check Codes
- Additional Automotive-grade Security (DMTF SPDM, MAC, DP AUX Encryption) avail
- Important Regions-of-Interest protected with Cyclic-Redundancy-Check Codes
- Display Safety Icons gain extra protection

Solution Summary – Introducing DisplayPort Automotive Extension (DP-AE)

- Builds on DP 2.1a / eDP 1.5a with safety & security enhancements
- Functional Safety via ROI CRCs, Frame Counters, Timeout Monitoring
  - Per region CRCs (up to 16 ROIs)
  - Automatic SafeState transitions
- Data Integrity with SPDM authentication & MAC tagging
- Secure AUX messaging & protocol stack isolation
- End-to-end Safety/Security supporting CRCs, MACs, SPDM-based authentication
- Support for Superframes and Subframes
- C-Model Emulator enables compliance testing
- Low complexity, high ecosystem readiness


DP Transmitter (DPTX)
DP Receiver (DPRX)
DPCD, DisplayID or Legacy EDID
Stream Source(s)
Stream/Link Policy Maker
Stream Security and Safety Manager
Stream Security and Safety Manager
Stream/Link Policy Maker
Stream Sink(s)
Functional Safety and Security Calculations
Stream Attributes
DisplayID, Legacy EDID, MCCS.,
Link Discovery, Initialization, Maintenance
Link Discovery, Initialization, Maintenance
DisplayID, Legacy EDID, MCCS.,
Stream Attributes
Functional Safety and Security Calculations
De-Multiplexing, Decryption, Stream Clock Regeneration
Link Layer
Isochronous Transport Services
AUX_CH Device Services
AUX_CH Link Services
Link Layer
AUX_CH Link Services
AUX_CH Device Services
Isochronous Transport Services
Packing, Stuffing, SDP Multiplexing, Encryption
PHY Layer
Main-Link
AUX_CH
HPD
PHY Layer
HPD
AUX_CH
Main-Link
Hot Plug Detect Signal
Command and Status Data
Serialized/Encoded


MSA[N-1]
AE_SDP[N-2]
AE_SDP[N-2]
AE_SDP[N-2]
Vblank
BS+
BF+
BF+
BS
SDP
BE
Active Frame N-1
SDP1
MSA[N]
...continued SDP1 (Frame N-1)
AE_SDP[N-1]
AE_SDP[N-1]
AE_SDP[N-1]
Vblank
BS+
BF+
BF+
BS
SDP
SDP
SDP
BE
Active Frame N
More AE_SDP chained packets to follow
No more AE_SDP chained packets to follow


MSA
AE_SDP Frame N-1
VBlank
BS
+
BF
+
BF
+
BS
SDP
SDP
BE
Active Frame
ROI_0
ROI_4
ROI_5
ROI_2
ROI_3
ROI_15
ROI_1

Addressing Functional Safety and Security Gaps

- New functional safety protocol enhancements
  - New protocols to aid ISO 26262 ASIL-D certification
  - CRC, Frame and Time-Out Monitoring
- New Automotive Compliant Security
  - UN155 Regulation Compliant and ISO21434 certifiable
  - Security Protocol using Standard DMTF™ SPDM and use of NIST Compliant Algorithms
  - Source, Sink and DP AUX Channel Protection (Integrity, Encryption)
- All these FuSa and security enhancements are included in the C-Model Emulator for CTS

Addressing Functional Safety and Security Gaps

New Automotive Compliant Security

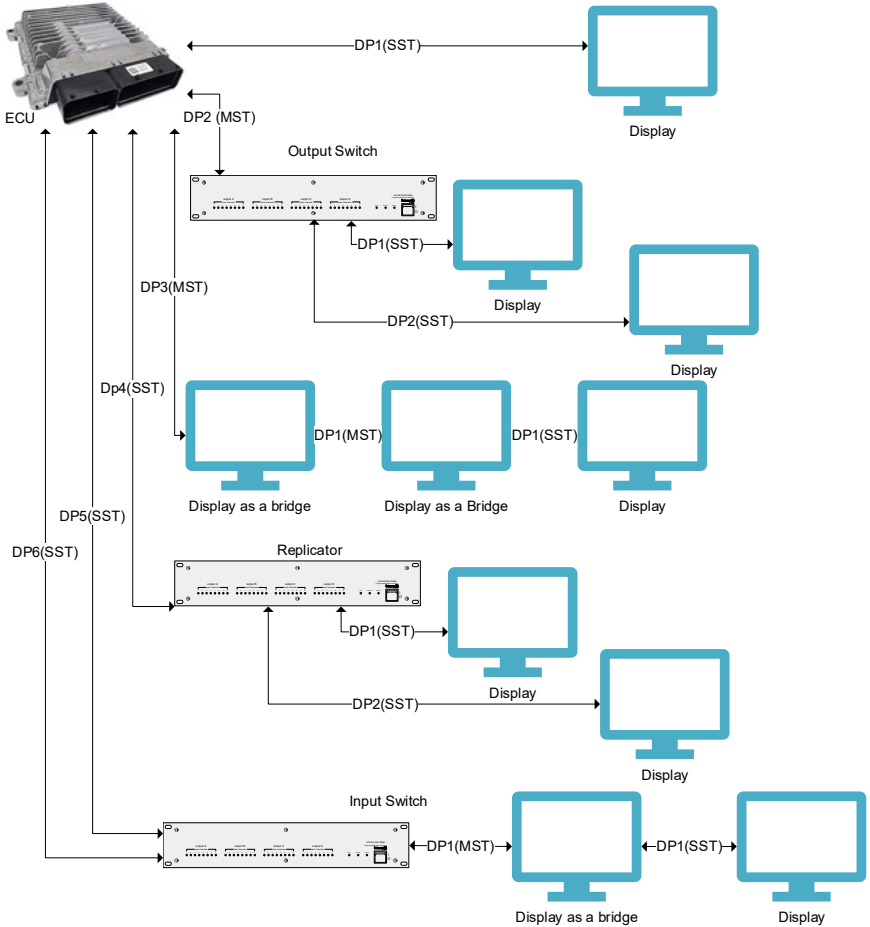
- **UN155** is a UN cybersecurity system that is being adopted by countries – specifically mandated in EU for all new passenger cars on public road from July 2024
- **ISO 21434** is an international standard for road vehicles providing a framework on requirements for cybersecurity risk management
- **NIST compliant algorithm** support such as AES-GMAC protection on the data plane and AES-GCM on the control plane

Security with Control and Data Plane Protection

- SPDM handshake for Source-Sink authentication
  - Defined set of SPDM Profiles
- Control Plane protection using AES-GCM/GMAC on DP AUX message clients
  - Configurable encryption handling
- Data Plane integrity protection using AES-GMAC on MSA, active frame data and AE_SDP
  - 128-bit or 256-bit security
- Secure session management via VSTL

System Topologies and Profiles

- Static topologies assumed for automotive (ROM config ready)
- Supports SST/MST, SerDes bridge, Branch/Composite Devices Profile 0–3 model:
  - Profile 0: Basic CRCs & DPCD access
  - Profile 3: Full MAC, SPDM, AUX protection

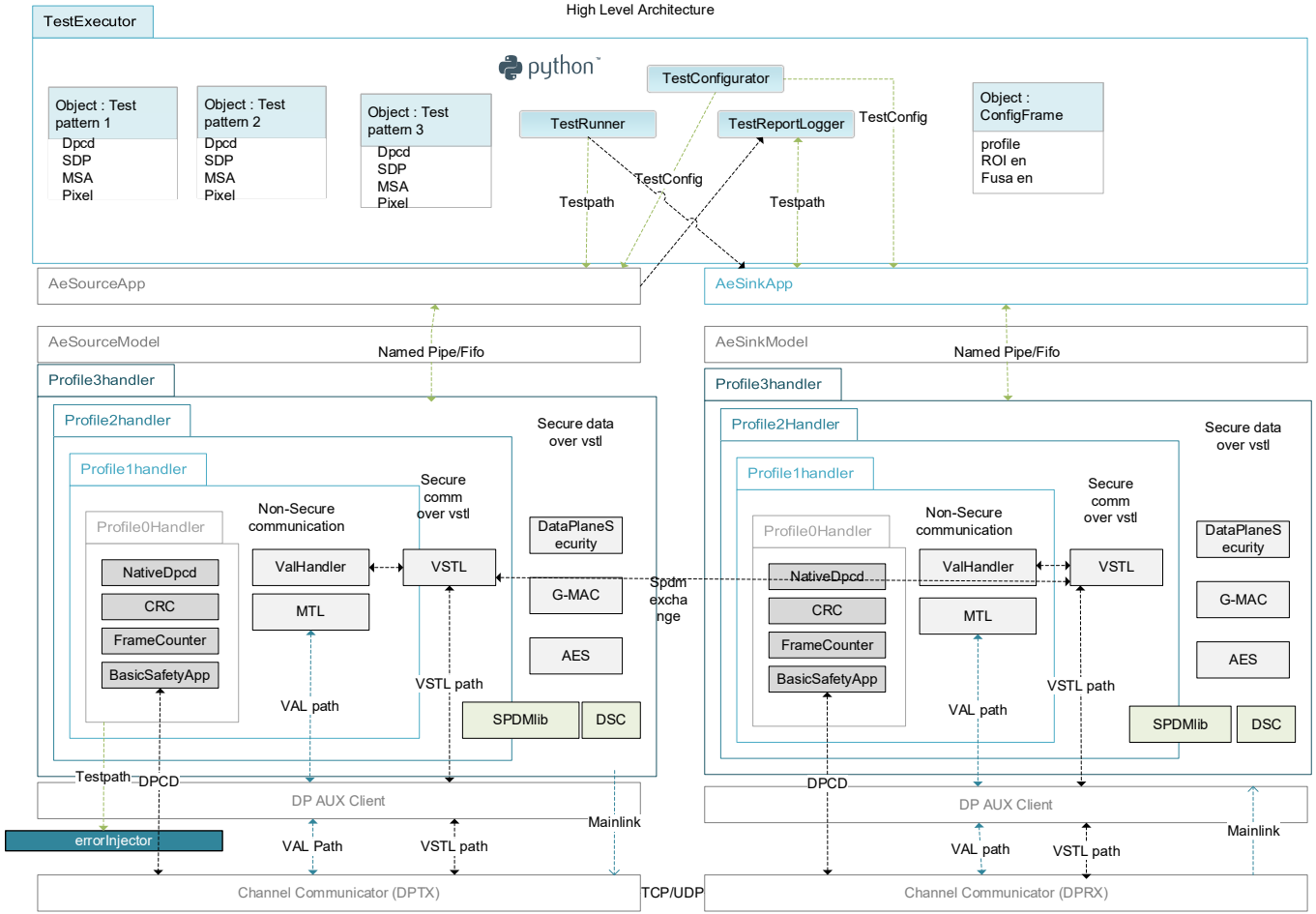

ECU
DP1(SST)
Display
DP2 (MST)
Output Switch
DP1(SST)
Display
DP3(MST)
DP2(SST)
Display
Dp4(SST)
DP1(MST)
DP1(SST)
Display as a bridge
Display as a Bridge
Display
DP5(SST)
DP6(SST)
Replicator
DP1(SST)
Display
DP2(SST)
Display
Input Switch
DP1(MST)
DP1(SST)
Display as a bridge
Display

AE Spec Feature	Normative Section All part shall be implemented	AE Spec Category	Basic FuSa		Advanced FuSa (Basic Ctrl Plane Security)	FuSa with Enhanced Security
			Profile 0	Profile 1	Profile 2	Profile 3
Uncompressed Pixel Frame CRC or Reconstructed Pixel CRC per Slice Column	Chapter 10 - DP Auto Extensions Functional Safety using CRC	FuSa	Normative	Normative	Normative	Normative
Compressed Pixel Frame CRC (see note 1)	Optional	FuSa	Optional	Optional	Optional	Optional
CRC on defined SDPs	Chapter 10 - DP Auto Extensions Functional Safety using CRC	FuSa	Normative	Normative	Normative	Normative
CRC on MSA	Chapter 10 - DP Auto Extensions Functional Safety using CRC	FuSa	Normative	Normative	Normative	Normative
CRC on Regions-of-Interest Support (Max 16)	Chapter 10 - DP Auto Extensions Functional Safety using CRC	FuSa	"Min ROI Req of 0"	"Min ROI Req of 4"	"Min ROI Req of 4"	"Min ROI Req of 4"
Frame drop/repeat and timeout monitoring check	Chapter 12 - Auto FuSa Frame Count and Timeout Monitor	FuSa	Normative	Normative	Normative	Normative
Basic Safety App (Direct DPCD Register access)	Chapter 6 - DPCD Regs	FuSa	Normative	Normative	Normative	Normative
Support for DP_AUX messaging client plus DPCD Reg Access	Chapter 8 - Control Plane Protocol Stack	Security	Not supported	Normative	Normative	Normative
Basic Safety App with Get_Measure using VAL	Chapter 8 - Control Plane Protocol Stack	FuSa	Not supported	Normative	Normative	Normative
VESA Secure Transport Layer (VSTL)	Ch 8 and 9 - Security	FuSa	Not supported	Not supported	Normative	Normative
"Data Plane Security (Only Auth and Integrity)"	Ch 8 and 9 - Security	Security	Not supported	Not supported	Not supported	Normative
MAC on Uncompressed Pixel/Compressed Bytes +MSA	Ch 8 and 9 - Security	Security	Not supported	Not supported	Not supported	Normative
Full Integrity Security on AE_SDP data	Ch 8 and 9 – Security	Security	Not supported	Not supported	Not supported	Normative
MAC on AE_SDP data	Ch 8 and 9 - Security	Security	Not supported	Not supported	Not supported	Normative
Data Plane Confidentiality	Ch 8 and 9 - Security	Security	Not supported	Not supported	Not supported	Not s[illegible]l
Super Frames	Chapter 11 - Superframes	FuSa	Optional	Optional	Optional	Optional

The VESA C-Model Emulator for Rapid Testing

- Virtual model implements the DP-AE protocol
- TCP/UDP-based simulation of AUX and frame channels
- Supports:
  - Fault injection
  - ROI on-the-fly changes
  - Self-testing and automation (Python API)
- Deployable across internal QA & OEM validation

C-Model Emulator Architecture

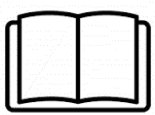


Executive Summary

VESA's new DisplayPort Automotive Extension (DP-AE) protocol brings critical functional safety and security features to the DisplayPort standard, enabling OEMs to meet ASIL-D certification requirements. DP-AE supports end-to-end CRC validation, secure AUX messaging, and SPDM-based device authentication.

The included C-Model emulator allows engineers to simulate, test, and verify DP-AE behaviour virtually, accelerating compliance cycles and reducing risk. With backward compatibility and a flexible profile system, DP-AE enables scalable adoption across the automotive display ecosystem.

MediaTek Development on VESA Automotive Extension



Spec collaboration

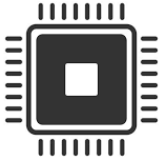
MediaTek aims to enhance the automotive application ecosystem by actively participating in spec development.

IP Simulation & Emulation

Pre-silicon development with SW simulation platform (VDK) and FPGA emulator.

CTS Verification

Utilize VESA's comprehensive CTS software model to pre-validate that the behavior of VESA AE IP complies with all specifications.

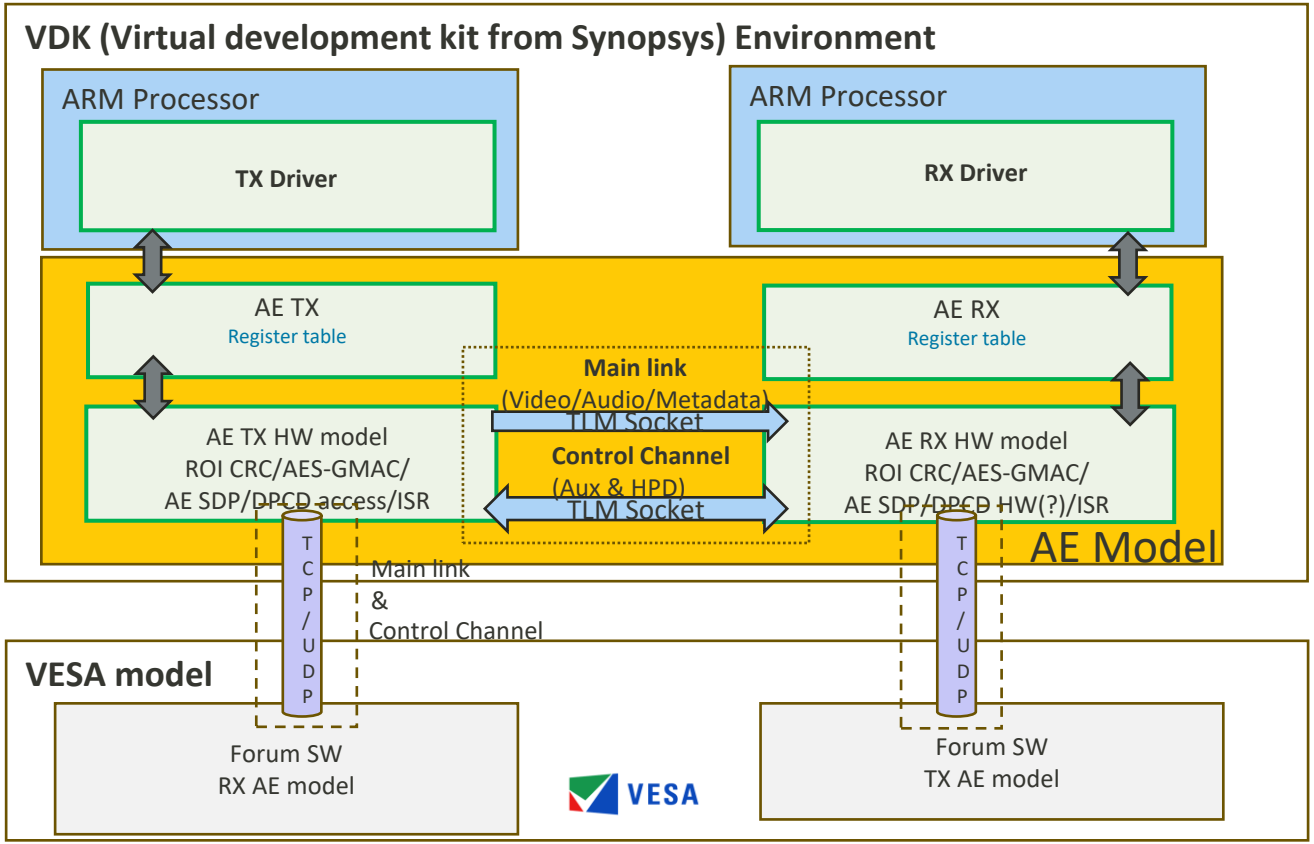


Design in Real Chip

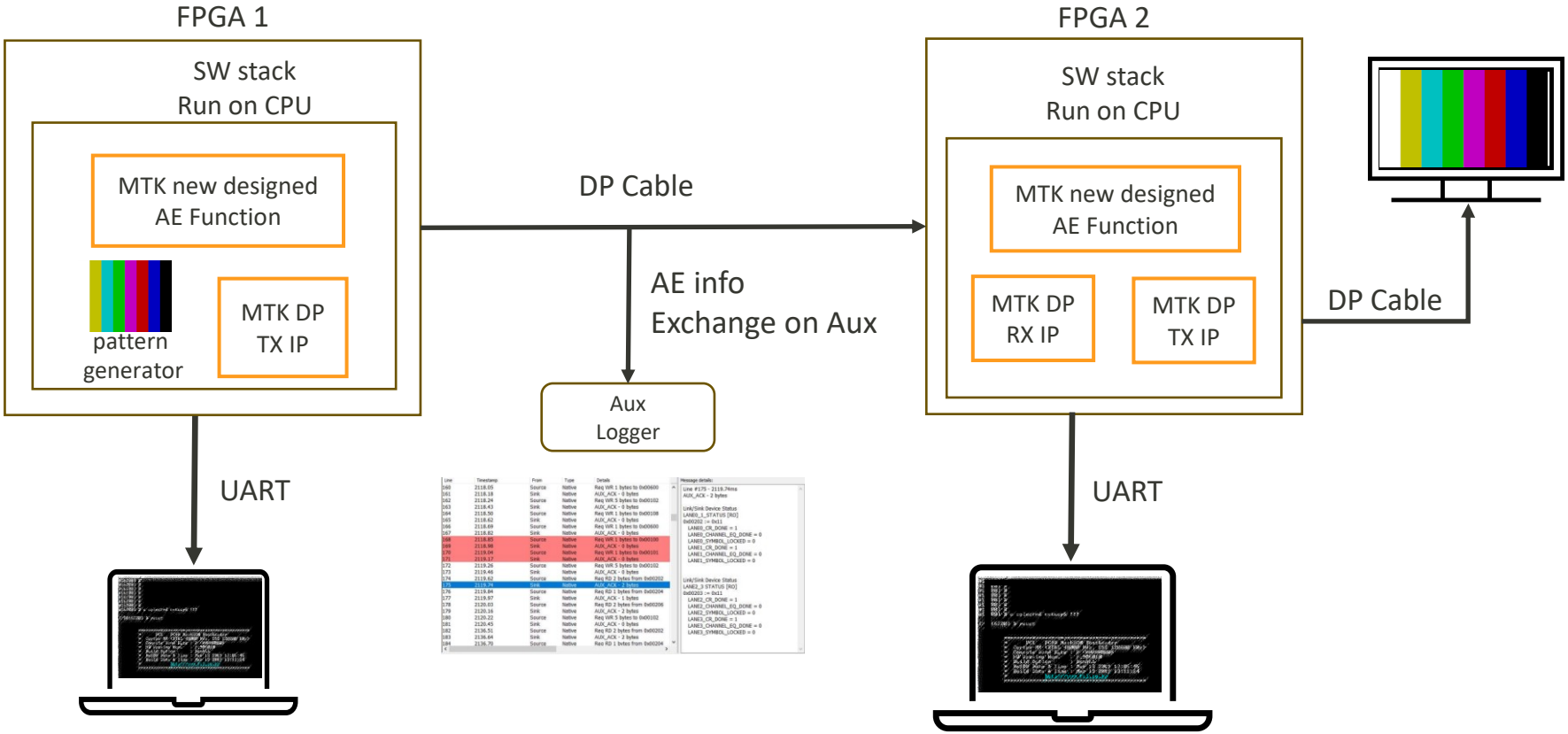
Integrate this comprehensive IP into the IC for future products to offer a complete solution.

MediaTek Comprehensive Verification for VESA AE

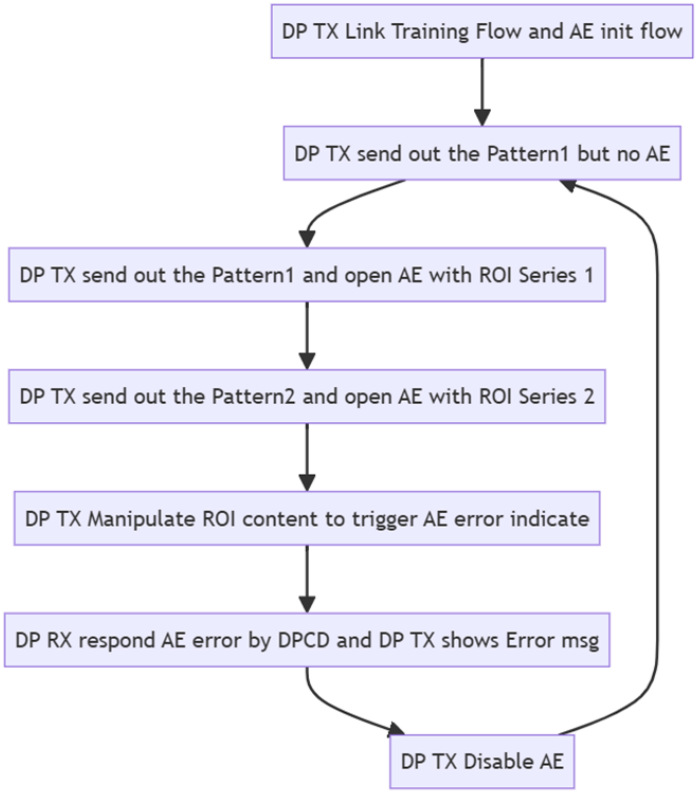
VESA AE IP in VDK for SW flow and abstract HW behavior verification



MediaTek's VESA DP AE Development on FPGA



MediaTek AE Demo Scenario



Info Shows On UART Text Interface:

Source:

Basic DP Link Status (Link Rate, Lane count..)
AE capability and status(AE active/inactive)
Configured AE SDP content
Operation Step
Error Status

Sink:

Basic DP Link Status (Link Rate, Lane count..)
AE capability and status(AE active/inactive)
Received AE SDP content
Received/Calculate ROI sets and correspond CRC value
Error Status

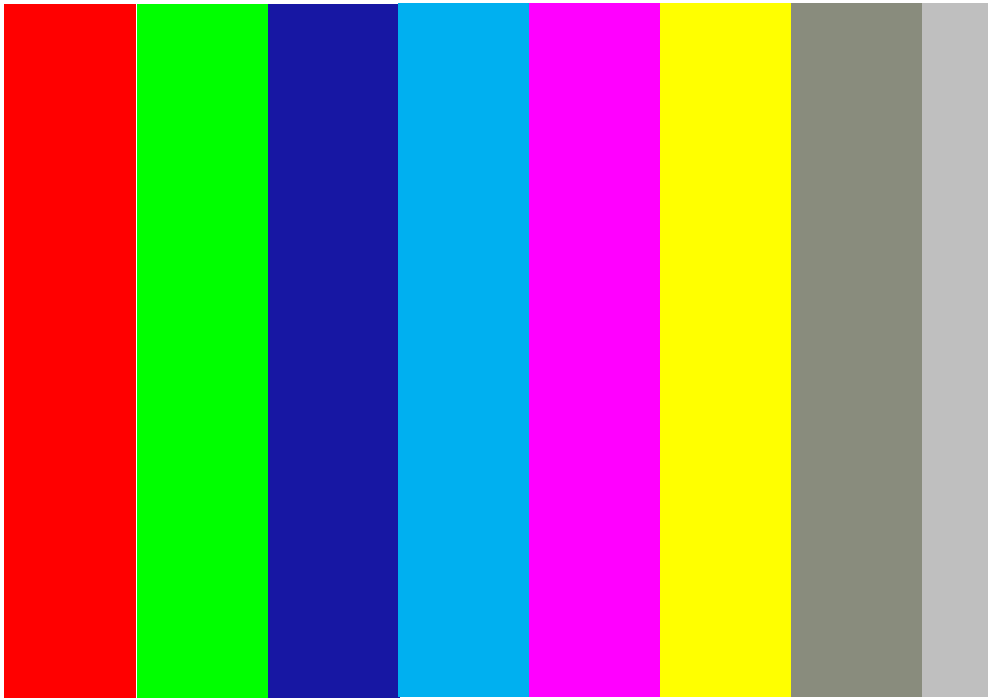
VESA DP AE Demo STAGE 1

STAGE 1
AE Disabled

STAGE 2
AE Enabled, ROI 1

STAGE 3
AE Enabled, ROI 2

STAGE 4
AE Enabled, ROI 2 with Error



VESA DP AE Demo STAGE 2

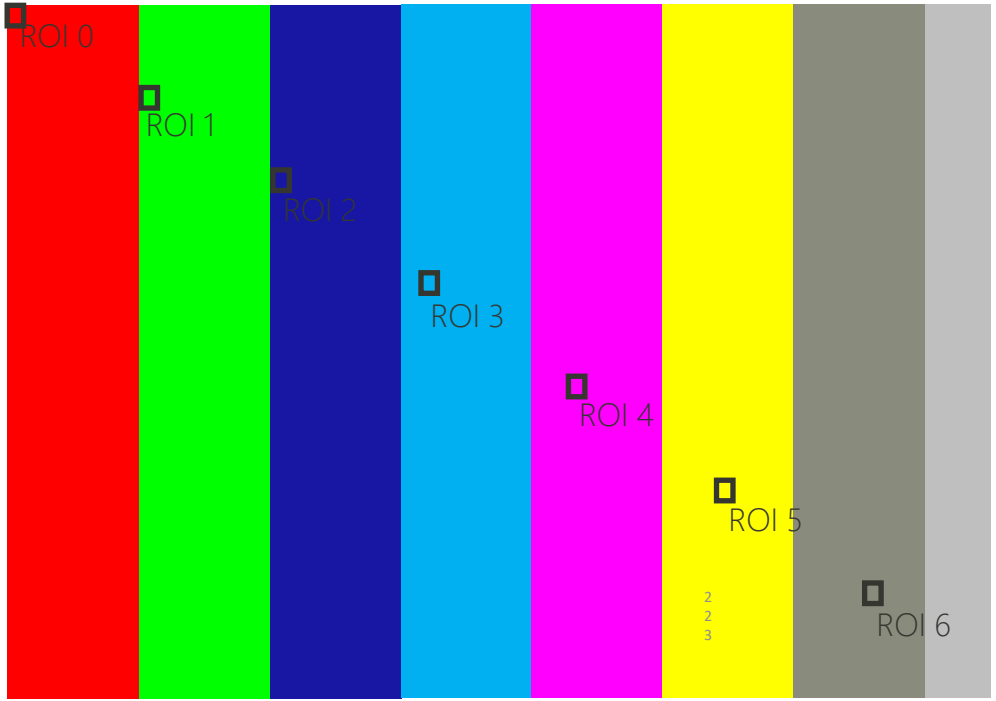
STAGE 1
AE Disabled

STAGE 2
AE Enabled, ROI 1

STAGE 3
AE Enabled, ROI 2

STAGE 4
AE Enabled, ROI 2 with Error

Regions-of-Interest (ROI) define specific areas within an active frame that require additional CRC protection to meet specific functional safety requirements.



VESA DP AE Demo STAGE 3

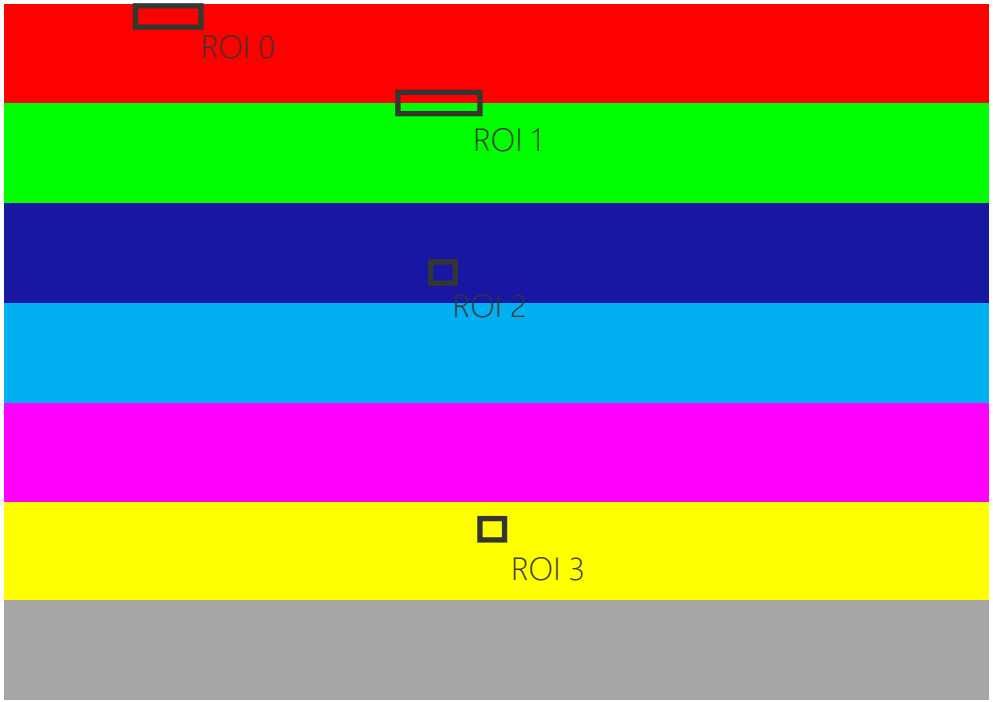
STAGE 1
AE Disabled

STAGE 2
AE Enabled, ROI 1

STAGE 3
AE Enabled, ROI 2

STAGE 4
AE Enabled, ROI 2 with Error

Regions-of-Interest (ROI) define specific areas within an active frame that require additional CRC protection to meet specific functional safety requirements.



VESA DP AE Demo STAGE 4

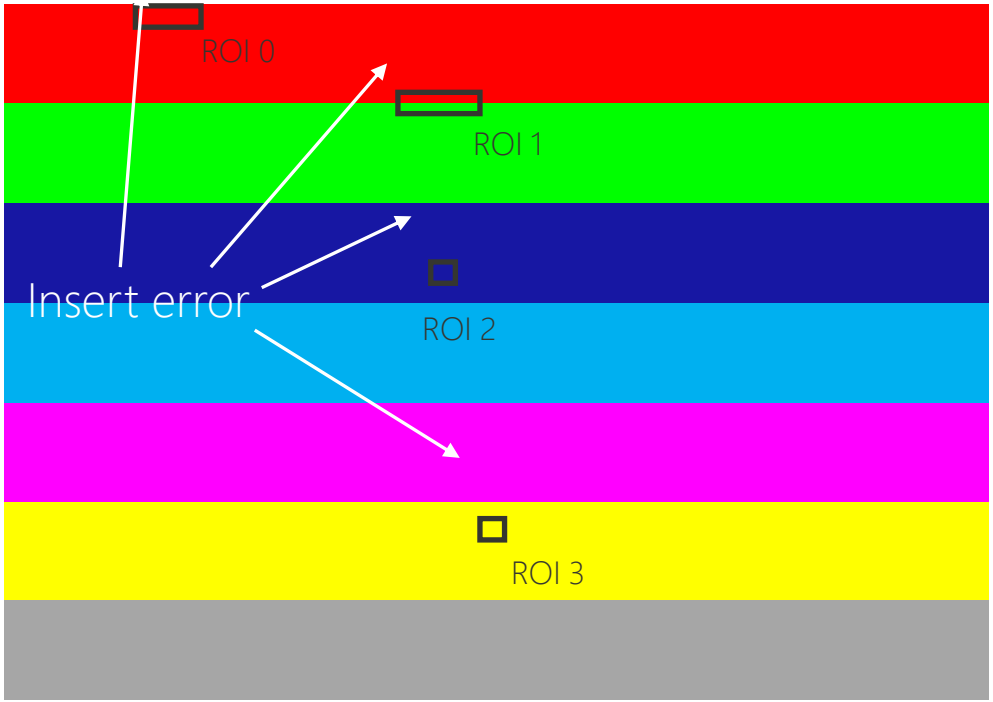
STAGE 1
AE Disabled

STAGE 2
AE Enabled, ROI 1

STAGE 3
AE Enabled, ROI 2

STAGE 4
AE Enabled, ROI 2 with Error

Regions-of-Interest (ROI) define specific areas within an active frame that require additional CRC protection to meet specific functional safety requirements.



Summary

Time	Topic	Speaker
10:00am	VESA Overview and Standards Updates, Including DisplayPort v 2.1b	Alan Kobayashi, VESA Board and DisplayPort Task Group Chair
10:30am	VESA Compliance Program	Jim Choate, VESA Compliance Manager
11:00am	DP2.1 Panel Replay and Advanced Link Power Management: Implementation and Testing Challenges	Marco Denicolai, Product Owner, IP Cores, Unigraf Oy
11:30am	DisplayPort Link Layer CTS v 2.1 MST Updates	Alok Soni, Software Lead, Teledyne LeCroy
12:00pm – 1:00pm	Lunch	
1:00pm	eDP and DP v 2.1 PHY CTS Overview and Updates	Abhijeet Shinde, Product Manager, Edge AI, Keysight Technologies
1:30pm	DP Alt Mode v 2.1a Overview and CTS Updates	Tim Wei, Senior Application Engineer, Ellisys
2:00pm	LRD/Active Cable Testing and DP 2.1 Enhanced Connector Certification	Lexus Lee, Technical Program Manager, Allion Labs
2:30pm – 2:45pm	Break	
2:45pm	VESA Display Panel Standards (ClearMR, DisplayHDR, AdaptiveSync)	Roland Wooster, Display Architect, Principal Engineer, Intel Corporation
3:15pm	Automotive Extension Services	Tung-Sheng Lin, Senior Technical Manager, MediaTek
3:35pm	Summary, Questions & Answers	Jim Choate, VESA Compliance Manager
3:50pm	Demo Stations Overview	

Summary

- Product shipments and certifications on based on VESA technologies continue to grow
- DP 2.1 UHBR capable product development and certifications ramped up 2024 and continue to increase in 2025
- VESA Enhanced cable and connector certification programs have been very successful with significant numbers of DP54 and DP80 cables certified
- DisplayPort over USB-C is a game changer for small form factor and portable products and is now the defacto standard for laptops, tablets and handheld devices
- Display Performance Standards adoption and certification have been extremely successful since introduction
- Development and adoption of new technologies continues to drive increases in VESA membership growth

Questions?

VESA

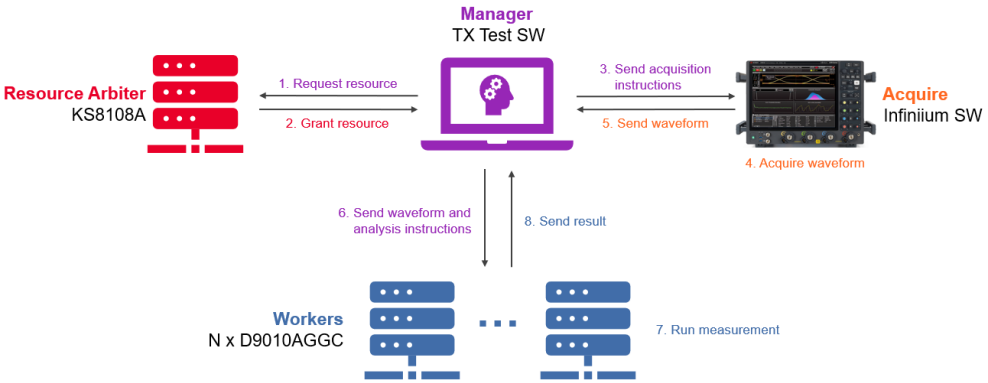
Demo Tables

KEYSIGHT

Maximizing Time Efficiency & Prepared for the Future

- Contact Information
  - Abhijeet Shinde
  - Abhijeet.Shinde@keysight.com

Keysight Technologies



Disaggregation: Time Efficiency

What are your costs?

- A comprehensive test plan leads to prolonged testing durations.
- A majority, about 75%, of the testing period is consumed by data processing.

What would be an optimal solution?

- Considerable reduction in test time through Measurement Disaggregation.
- Maximizes the use of your existing investment.
- $$$ Cost-effective savings.
- Enhances your current equipment and expertise.

M8050A: Prepared for the future

What are your costs?

- Investment in hardware to meet next-generation requirements
- Reduced passing margin

What would be the optimal solution?

- Reliable support for up to 120GBd and various PAM types
- Provides the lowest intrinsic noise, enhancing passing margin
- Facilitates hassle-free stress calibration, saving both time and money

Teledyne LeCroy Test Solutions for DisplayPort v2.1

M42de 80G Video Analyzer/ Generator

TELEDYNE LECROY
Everywhereyoulook™

Website: http://www.teledyne.com

Teledyne LeCroy DisplayPort Test Platforms

- **quantumdata M42de Analyzer / Generator**
  - DisplayPort 2.1 UHBR Lane Rates
  - Deep Capture / Analysis
  - T.A.P.4™ Passive Monitoring
  - Comprehensive DP 1.4 & 2.1 Compliance Coverage
  - qdPrime™ Automated Test Suite

- **quantumdata M21 Analyzer**
  - Portable DP Analyzer (up to UHBR 13.5Gb/s)
  - Aux Channel Monitoring

- **SDA8000HD**
  - 20 – 65 GHz bandwidth
  - 12-bit resolution
  - Up to 320 GS/s sample rate
  - Up to 8 Gpts memory per channel
  - 200 Mpts/ch standard

DisplayPort Alt Mode Compliance Testing and Analysis solutions

SYMBIOSYS ALLIANCE

Ellisys USB/DPAM Test and Analysis Solutions

USB Explorer™ 350

Multi-function USB Type-C®, USB 3.2, and Power Delivery Protocol Test Platform

VESA-Approved Tester for DisplayPort ALT Mode

Type-C Tracker™

Protocol and Electrical Analysis Tool for USB Type-C® Standards

Includes DP AUX and DP ALT Support

ellisys
Better Analysis

Unigraf UCD-500 Gen2

16K DP 2.1 Generator & Analyzer

DisplayPort

USB Type-C

- DP 2.1 Sinks and Sources up to 8K@60Hz
  (16K@60Hz with DSC up to UHBR 20 Bit Rate)
- Supports DP and USB-C connectors
  - UHBR 20 Gb max link rate for DP and USB-C connectors
- Adaptive Sync, DSC, FEC and LTTPR support
- DP 2.1 and DP 1.4a Link Layer CTS Tool
- LTTPR / DisplayID / EDID CTS / AdaptiveSync CTS Tool
- HDCP 2.3 Compliance Test Device for Transmitters, Receivers and Repeaters *(under development)*
- Color depth 6 to 16bpc
- Capture memory 16GB
- NEW Optional features of Link Analyzer, Panel Replay and eDP testing

UNIGRAF

CABLE TEST SOLUTION: DP80, DP54, DP8K

NEW ZNB3000

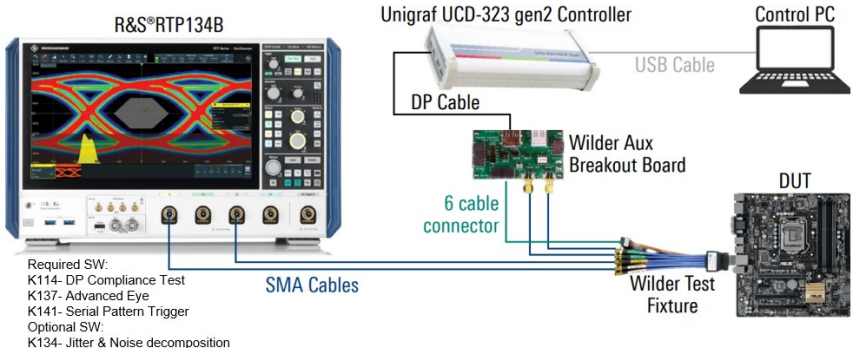
- VESA Approved
- Easy to follow Method of Implementation for each DP80, DP54, and DP8k passive cable test
- Utilizes R&S ZNB3020, ZNB20, or multi-port ZNBT20 (up-to 24 fully integrated test ports) to capture data
- Analyzes frequency domain results with Get_iPar (DP80/54) or IntePar (DP8k)

ZNB

ZNBT

TRANSMITTER TEST SOLUTION: DP 2.1 (HBR X)

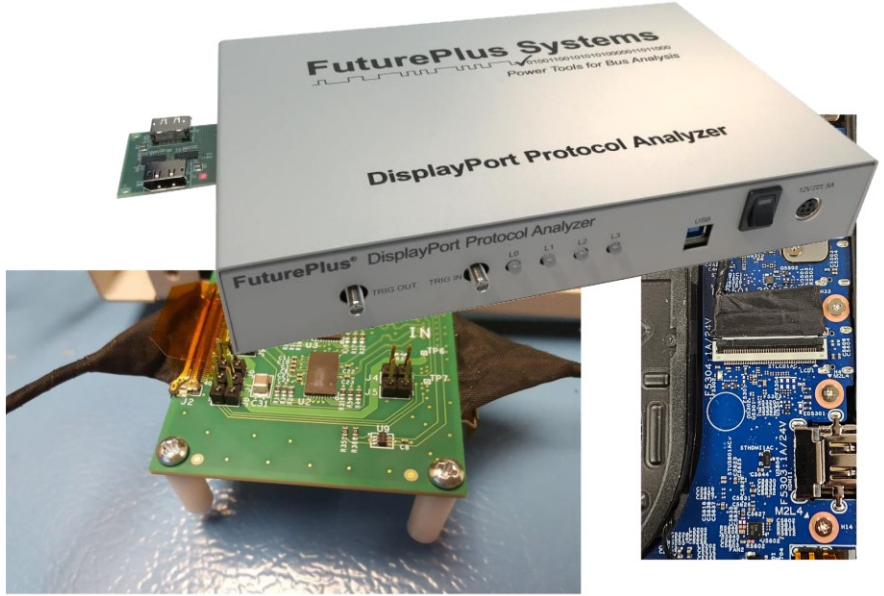
- VESA Approved for DP 2.1 (HBR X) (formerly known as DP1.4)
- Capable of supporting automated eDP (HBR X) (formerly known as eDP1.5) measurements
- Automates testing with R&S ScopeSuite automation software
- Utilizes Unigraf UCD323 gen2 AUX controller in test automation
- Fast, reliable, and easy to use for testing DP Tx



FuturePlus Systems

Advancing Technology Development

eDP and DisplayPort Protocol Analysis and Validation - Real Time



eDP 1.4b and 1.5a, DP2.1
USB-C and DisplayPort
Probes
UHBR10, UHBR13.5
Up to 4 Lanes
Single Stream Transport and
Multi-Stream Transport
and more....

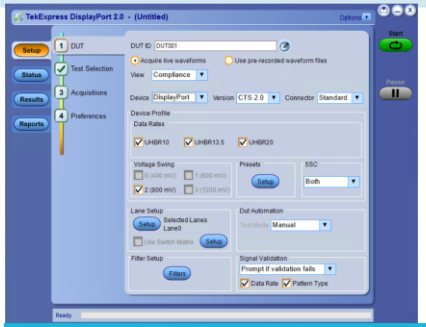
Something Special? We Like Challenges!

Tektronix DisplayPort Tx Compliance Testing Solution

Automated compliance

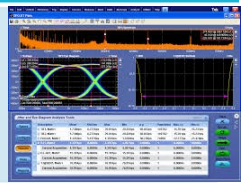
Fully automated compliance solution

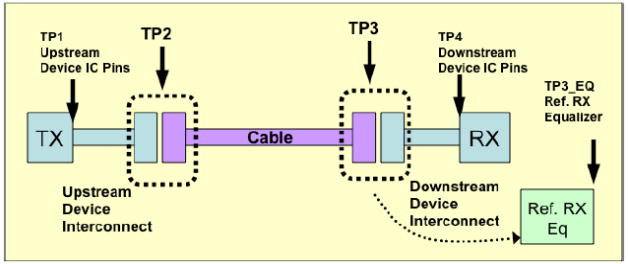
Supports all data rates till UHBR20



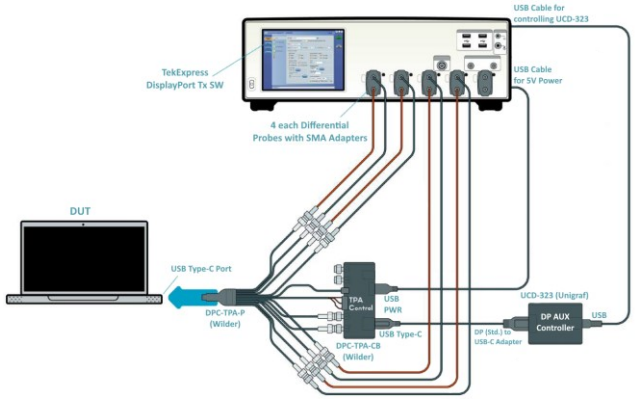
Debugging

Advanced Debugging capability





DisplayPort Test Setup



Compliance Test Points

Supports both TP2 & TP3EQ(CTLE) test points

USB4 cable model are used in the TP3EQ tests

Signal Validation

Pattern validation

Pre Recorded

Offline Mode

Cross Geo collaboration

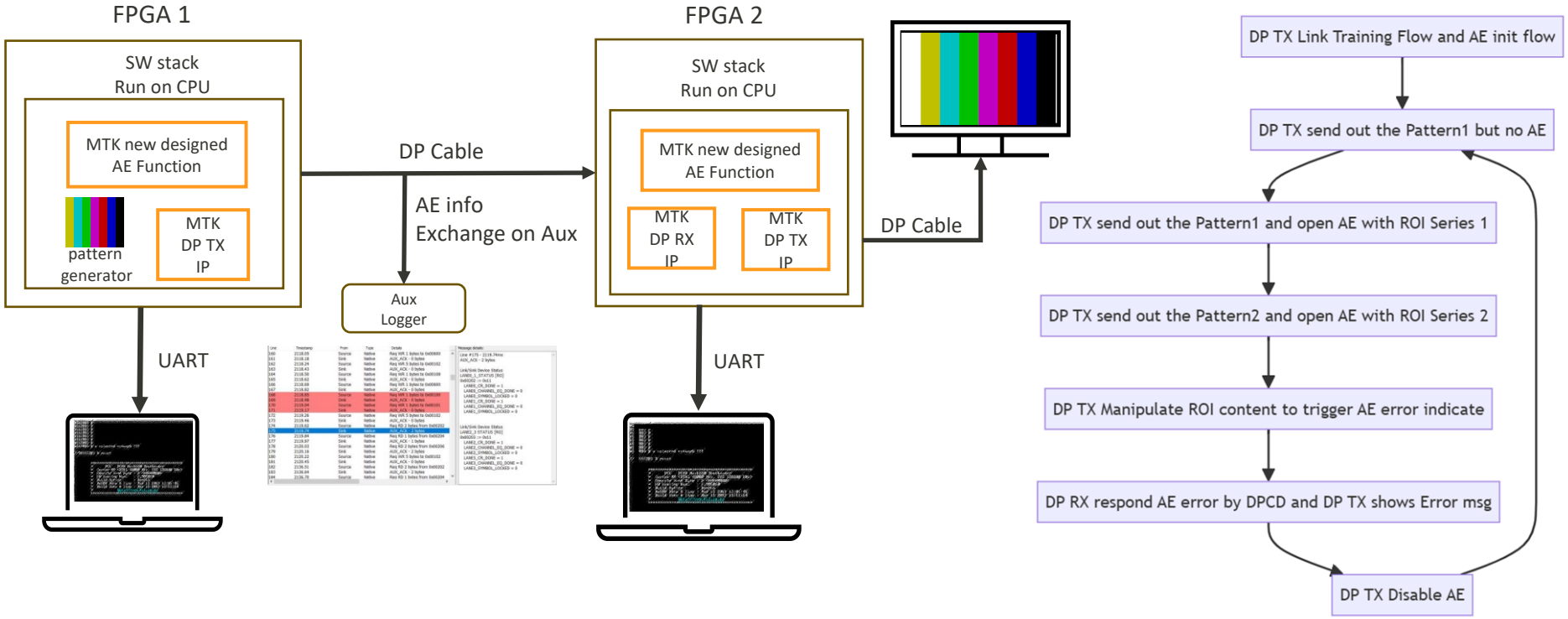
DUT control

Automation with UCD 323 and DPR100

Signal acquisition

Use P76XX series probe with compatible probe tips in absence of fixtures.

VESA DP Automotive Extension FPGA Demonstration



Thank you for attending the VESA Workshop
San Francisco, CA, USA
2025