



Welcome VESA Workshop Seoul, Korea 2025

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Time	Topic	Speaker
10:00am	VESA Overview and Standards Updates: DisplayPort v 2.1b and Display Panel Standards	Jim Choate, VESA CPM
10:30am	DisplayPort Link Layer CTS v 2.1 MST Updates	Neal Kendall, Senior Staff Product Marketing Manager, Teledyne LeCroy
11:00am	eDP and DP v 2.1 PHY CTS Overview and Updates	Jim Choate, VESA CPM
11:30am	DP v 2.1 Panel Replay and Advanced Link Power Management: Implementation and Testing Challenges	Sergey Grushin, Chief Technology Officer, Unigraf
12:00pm – 1:00pm	Lunch	-
1:00pm	VESA DisplayHDR and AdaptiveSync Specification Overview and Test	Do Kyun Kim, Wired Interface/Connectivity Standard Project Leader Seung Hyun Yoo, Wired Interface/Connectivity Standard Engineer, LG Electronics
1:30pm	ClearMR Specifications and Compliance Testing Overview	Dr. Yongwoo Yi, Principal Engineer, Samsung Display
2:00pm	DP Alt Mode v 2.1a Overview and CTS Updates	Tim Wei, Senior Application Engineer, Ellisys
2:30pm – 2:45pm	Break	-
2:45pm	VESA Compliance Program	Jim Choate, VESA CPM
3:15pm	Summary, Questions & Answers	Jim Choate, VESA CPM
3:30pm	Demo Stations Overview	Jim Choate, VESA CPM

VESA Overview and Standards Updates

Jim Choate

VESA Compliance Program Manager

October 31, 2025

Agenda

- VESA Overview
- DisplayPort Overview
- VESA Technology Development Areas
- Summary

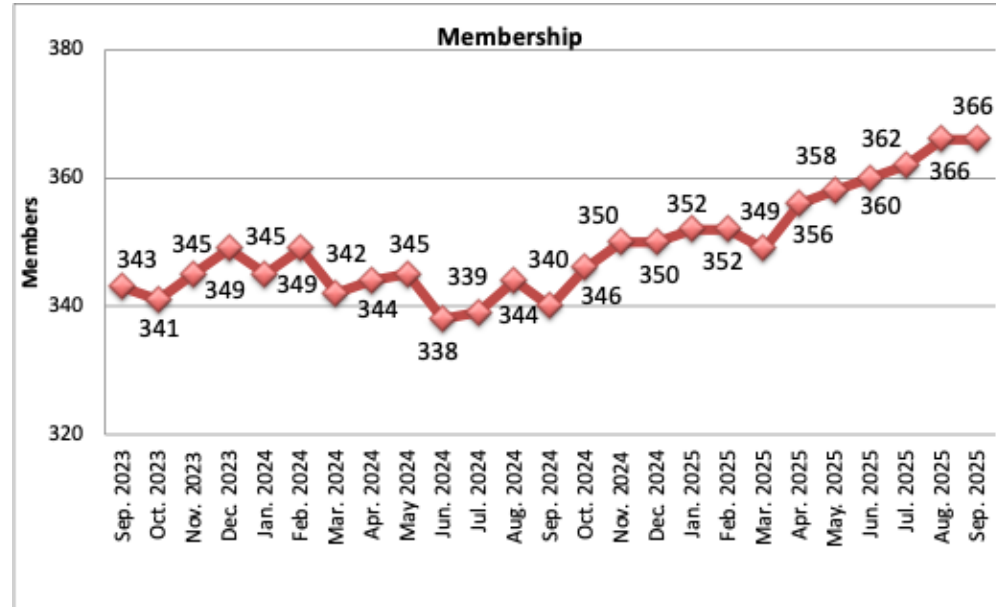
VESA OVERVIEW

VESA Vision

- VESA's vision is continual growth in technical standards development and evolution into an international trade association, with a **worldwide** membership driving standards initiatives, product implementations, and market implementation.

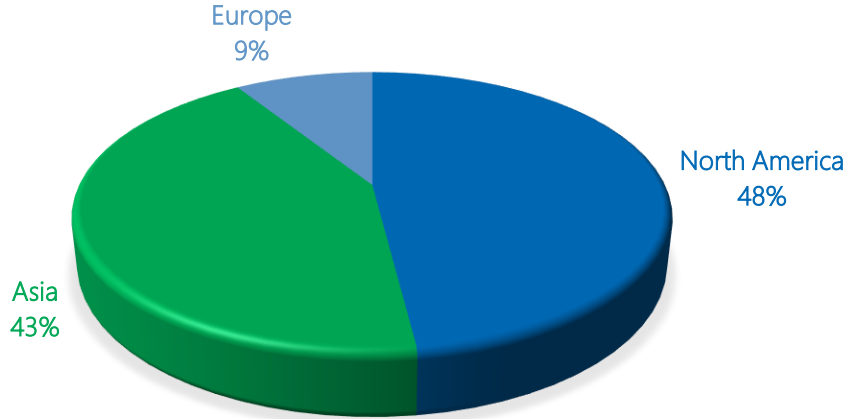
About VESA

- A growing global industry alliance with 366 members. Strong growth in membership.
- Mission to develop, promote and support ecosystem of vendors and certified interoperable products for the electronics industry.
- *Develops OPEN standards, contribution is open to all companies at all stages of development*



VESA Membership Growth

MEMBERSHIP BY REGION 2013



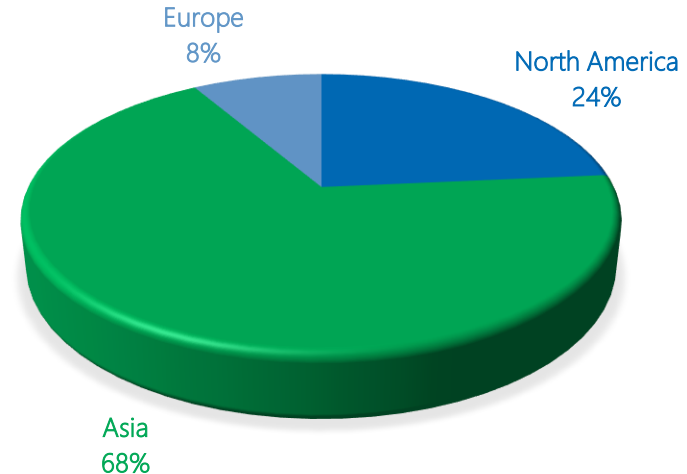
Changes from 2013:

Asia + 25%

North America – 24%

Europe – 1%

MEMBERSHIP BY REGION 2024



VESA Standards Enable Many Market Segments...



Monitors, PCs and laptops



Smartphones and tablets



Gaming consoles and headsets



Automotive



Multi-Stream Transport (MST)

*NEW: VESA DP AE
specification*

VESA Local Asian Support Capability

- VESA continues to provide local support to Asia to address growing regional membership needs
- **Kellen** is VESA's Representative in Asia
- This partnership provide members with a communication option in their native language. Kellen handles membership related activities including, new membership requests, renewals, event support and translation of VESA member messaging, etc.
- AsiaVESA@kellencompany.com or at +86 10 6580 0670

DisplayPort™ Overview

DisplayPort Market Penetration

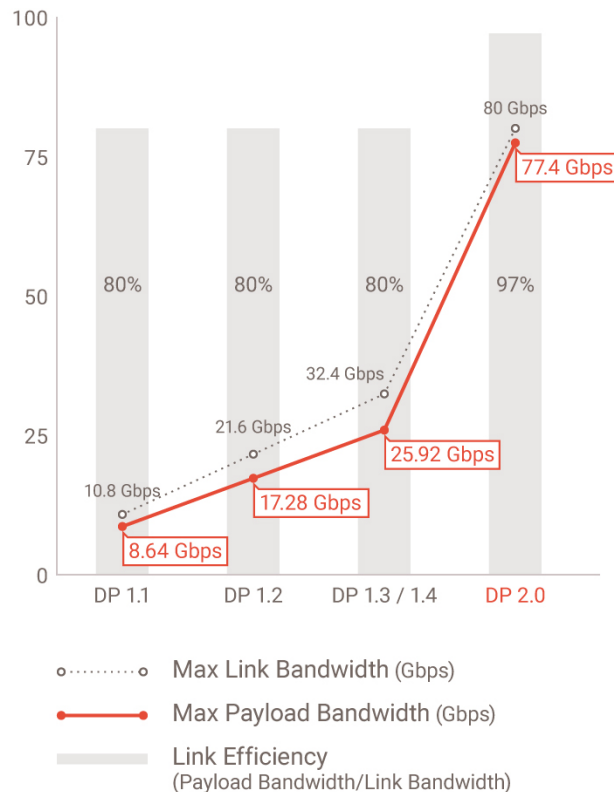
- DisplayPort adoption continues to grow in 2025
- DisplayPort and DisplayPort Alternate Mode over USB-C
 - The common monitor interface for personal computers
 - Supported on the USB-C interfaces
 - Mandated for USB4 and Thunderbolt
 - Automotive integration with DP AE specification
 - Mobile phones with USB-C
- Embedded DisplayPort (eDP)
 - ~95% penetration in notebook PCs, used in many high-end tablets and automotive

DisplayPort 2.1a Summary

- DisplayPort v2.1a was released in December 2023
- Major features added in v2.0/v2.1/v2.1a/v2.1b:
 - Added 128b/132b DP channel coding
 - Increase in data bandwidth performance (almost 3X) with new link rates up to 20 Gbps/lane
 - Panel Replay, similar to PSR (Panel Self Refresh) used for eDP
 - DSC support mandated
 - Enhanced DP connectors and cables (DP54 and DP80)
 - DP PHY specification alignment with USB4 PHY specification
 - Updated DP to HDMI v2.1 or higher protocol converter (PCON)
 - Corrects errata
 - Replaces DP40 cables with DP54 to expand higher rate cable length
 - Expanded Tunneling capability
 - Updates for DP AE Services specification
 - DP80LL cable spec section
 - LRD Active Cable Electrical Mandate section

- DisplayPort 2.1a enables up to 3X increase in video bandwidth performance vs DP 1.4
- 3 new data rates added. UHBR10, UHBR13.5 and UHBR20 provides up to 80Gbps link bandwidth for 4 lanes at 20Gbps.
- First standard to support 8K resolution (7680 x 4320) at 60 Hz refresh rate with full-color 4:4:4 resolution, including with 30 bits per pixel (bpp) for HDR-10 support
- Beyond 8K resolutions achieved with maximum link rate to up to 20 Gbps/lane and more efficient 128b/132b channel coding

EVOLUTION OF DISPLAYPORT DATA BANDWIDTH



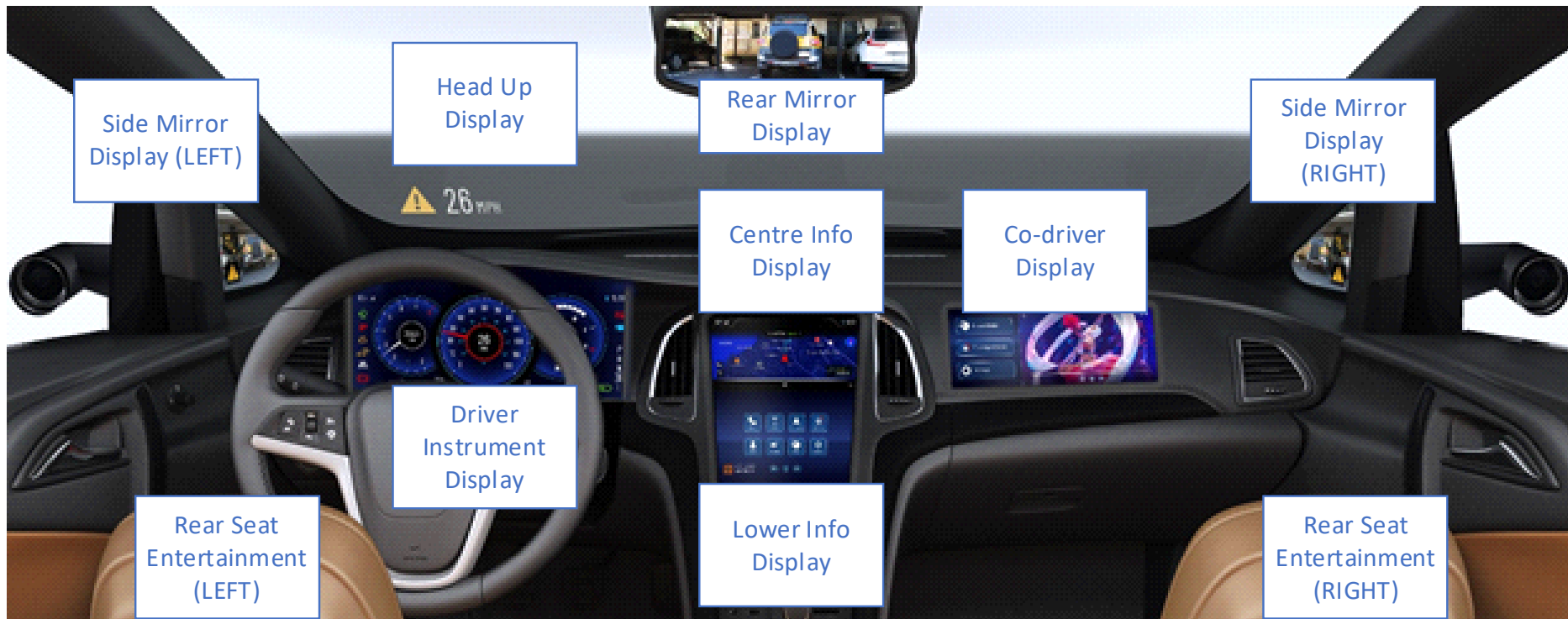
DisplayPort 2.1 Link Layer CTS Summary

- DP 2.1 LL CTS v1.1 will release in Q4 2025
- Major updates:
 - Updates to align with other published VESA standards and terminology
 - Incorporated many approved and published SCRs
 - For example: FEC, Audio, DisplayID, min Hblank/Vblank, etc
- Addition of new Source, Sink and Branch device MST tests (covered separately)

Introduction to VESA

DisplayPort

Automotive Extensions



- Instrument clusters, HUDs, mirrors, and rear-seat entertainment
- ASIL-D safety, UN155 and ISO 21434 security may be required
- Existing DP/eDP protocols were not built with these challenges in mind.
- Forcing OEMs into fragmented, non-standard solutions.

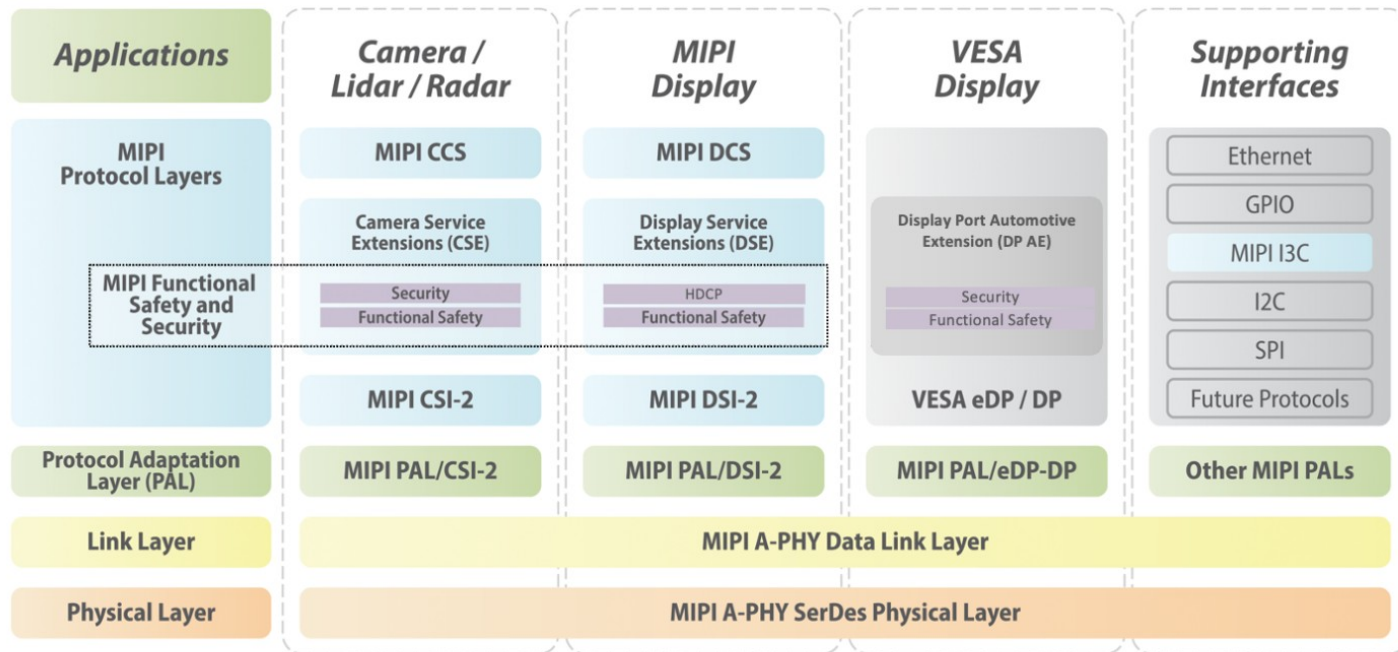
Introducing DisplayPort Automotive Extension (DP-AE)

- Builds on DP 2.1a/eDP 2.0 with safety & security enhancements
- Functional Safety via ROI CRCs, Frame Counters, Timeout Monitoring
 - Per region CRCs (up to 16 ROIs)
 - Automatic SafeState transitions
- Data Integrity with SPDM (Security Protocol and Data Model) authentication & MAC (Message Authentication Code) tagging
- Secure AUX messaging & protocol stack isolation
- End-to-end Safety/Security supporting CRCs, MACs, SPDM-based authentication
- Support for Superframes and Subframes
- C-Model Emulator enables compliance testing
- Low complexity, high ecosystem readiness

Key Takeaways

- Protocol level extension of DP 2.1 for the use of automotive display interface
 - Enablement with AES_SDP and extensive DPCD registers
- Features that facilitate the support of Functional Safety (FuSa) and security
 - ROI: region of interest
 - CRCs for Datapath, MSA, and SDP
 - Soft Fail/Hard Fail fault detection for robustness
 - SPDm-based device authentication
 - MACs for Datapath, MSA and Active Frame data
 - Automotive-grade encryption on control plane (DP AUX) and/or data plane (MSA, AES_SDP, active frame)
- Profiles 1-4 to accommodate various levels of FuSa and security requirements
- Use Superframe to simplify connectivity while maintaining the versatility of DP AE functions

As a Part of MIPI Automotive SerDes Solution (MASS) Ecosystem



Current Status and Timeline

- Spec:
 - 1.0 released in December 2023
 - 1.1 adoption vote: end of October 2025
- CTS:
 - First draft release: December 2025
 - TE implementation completion: end of March 2026
 - PlugTest to be held in Q1 or Q2 2026

VESA Technology Development Areas

VESA technology development

VESA members are collaborating on several key technology areas

- Embedded DisplayPort - v2.0 (published Sept 2024)
- DP Tunneling over USB4 – compliance testing has begun
- AR/VR Task Group
 - Focused on creating solutions roadmap to meet performance, power and implementation requirements for future AR/VR needs. Specification is released. Work on CTS underway
- DP Automotive Extension Task Group
 - Working with automotive industry to address needs for high-resolution performance in this market segment
 - Working on DP AE CTS and testing
- MST Compliance Test Updates
 - DP 2.1 LL CTS v1.1 near release and new tests were run at last weeks PlugTest event
- Display Performance Metrics Task Group
 - DisplayHDR, ClearMR, AdaptiveSync updates and proposals for future capabilities



DP2.1 Compliance Tests Update Rev 1.1

DP2.1 규정 준수 테스트 업데이트 개정판 1.1

Name: Neal Kendall (Alok Soni)

Company: Teledyne LeCroy

Date: 10/28/2025 (31-Oct-2025)

이름: Neal Kendall

회사: Teledyne LeCroy

날짜: 2025년 10월 28일 (2025년 10월 31일)



Overview of Test Updates for CTS Rev 1.1

테스트 업데이트 개요
CTS Rev 1.1의 경우

Section 4 Source Device Tests

- 4.2 Source Device Services Test Procedures.
- 4.3 Source Device Link Services Test Procedures.
- 4.4 Source Device Isochronous Transport Services Test Procedures.
- 4.5 Source Device FEC Test Procedures.
- 4.6 DSC Source Device Test Procedures.
- 4.7 Source Device DisplayPort DisplayID/EDID and Native DisplayID Test Procedures.
- 4.8 Source Device DisplayPort Adaptive-Sync Test Procedures.
- 4.9 Source Device LTTTPR Test Procedures.
- 4.10 Source Device MST Compliance Tests.
- 4.10.1 Source Device MST Protocol Tests.

섹션 4 소스 장비 테스트

- 4.2 소스 장비 서비스 테스트 절차.
- 4.3 소스 장비 링크 서비스 테스트 절차.
- 4.4 소스 장비 등시성 전송 서비스 테스트 절차.
- 4.5 소스 장비 FEC 테스트 절차.
- 4.6 DSC 소스 장비 테스트 절차.
- 4.7 소스 장비 DisplayPort DisplayID/EDID 및 기본 DisplayID 테스트 절차.
- 4.8 소스 장비 DisplayPort 적응형 동기화 테스트 절차.
- 4.9 소스 장비 LTTTPR 테스트 절차.
- 4.10 소스 디바이스 MST 컴플라이언스 테스트.
- 4.10.1 소스 장비 MST 프로토콜 테스트.

Section 5 Sink Device Tests

- 5.2 Sink Device Services Test Procedures
- 5.3 Sink Device Link Services Test Procedures
- 5.4 Sink Device Isochronous Transport Services Test Procedures
- 5.5 Sink Device FEC Test Procedures
- 5.6 Sink DSC Protocol
- 5.7 Sink Device DisplayPort DisplayID/EDID Test Procedures
- 5.8 Sink Device DisplayPort Adaptive-Sync Test Procedures
- 5.9 Sink Device Embedded LTTTPR Test Procedures

섹션 5 싱크 장비 테스트

- 5.2 싱크 장비 서비스 테스트 절차
- 5.3 싱크 장비 링크 서비스 테스트 절차
- 5.4 싱크 장비 등시성 운송 서비스 테스트 절차
- 5.5 싱크 장비 FEC 테스트 절차
- 5.6 싱크 DSC 프로토콜
- 5.7 싱크 장비 DisplayPort DisplayID/EDID 테스트 절차
- 5.8 싱크 장비 DisplayPort 적응형 동기화 테스트 절차
- 5.9 싱크 장비 임베디드 LTTTPR 테스트 절차

Section 6 Branch Device Tests

- 6.1 to 6.9 (Reserved)
- 6.10 Branch Device MST Tests (Normative)
 - 6.10.1 Branch Setup 1 Tests
 - 6.10.2 Branch Setup 2 Tests
 - 6.10.3 Branch Setup 3 Tests
 - 6.10.4 Branch Setup 4 Tests
 - 6.10.5 Branch Setup 5 Tests
 - 6.10.6 Composite Sink (Daisy-chainable Sink) Setup 1 Tests
 - 6.10.7 Composite Sink (Daisy-chainable Sink) Setup 2 Tests
 - 6.10.8 Composite Sink (Daisy-chainable Sink) Setup 3 Tests
 - 6.10.9 Composite Sink (Daisy-chainable Sink) Setup 4 Tests

섹션 6 분기 장비 테스트

- 6.1 - 6.9 (예약)
- 6.10 분기 장비 MST 테스트(사양)
 - 6.10.1 분기 설정 1 테스트
 - 6.10.2 분기 설정 2 테스트
 - 6.10.3 분기 설정 3 테스트
 - 6.10.4 분기 설정 4 테스트
 - 6.10.5 분기 설정 5 테스트
 - 6.10.6 복합 싱크대(데이지 체인 싱크대) 설정 1 테스트
 - 6.10.7 복합 싱크대(데이지 체인 싱크대) 세트 2 테스트
 - 6.10.8 복합 싱크대(데이지 체인 싱크대) 설정 3 테스트
 - 6.10.9 복합 싱크대(데이지 체인 싱크대) 설정 4 테스트

Sec. 7 LTTPR & DP Tunnel Device Tests

- 7.1 LTTPR and DP Tunnel Device Test Procedures

7절 LTTPR 및 DP 터널 디바이스 테스트

- 7.1 LTTPR 및 DP 터널 장비 테스트 절차



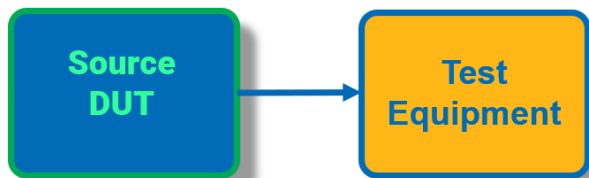
MST Source Tests

MST 소스 테스트

Approved DP 2.1 Compliance Tests

Source Device MST tests

- VESA Approved Tests with new numbers (4.10.1.1 to 4.10.1.21).



Source Setup - 1

승인된 DP 2.1 컴플라이언스 테스트

소스 디바이스 MST 테스트

- 새로운 번호(4.10.1.1에서 4.10.1.21)로 VESA 승인 테스트.

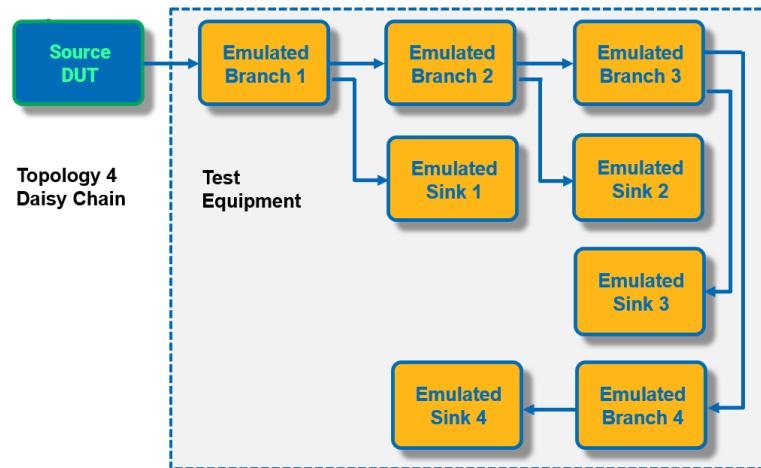
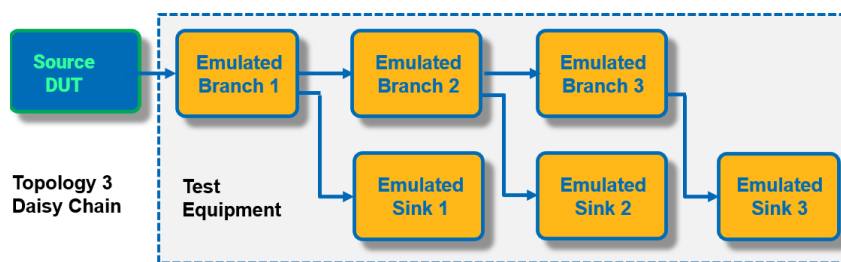
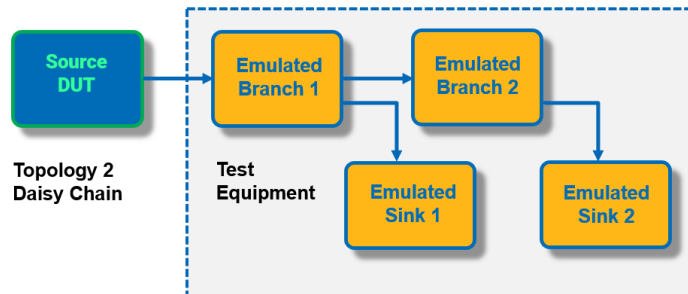
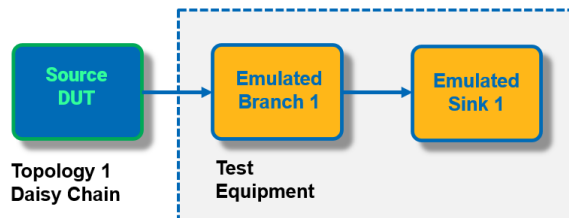


Approved DP 2.1 Compliance Tests

Source Device MST Test Setups

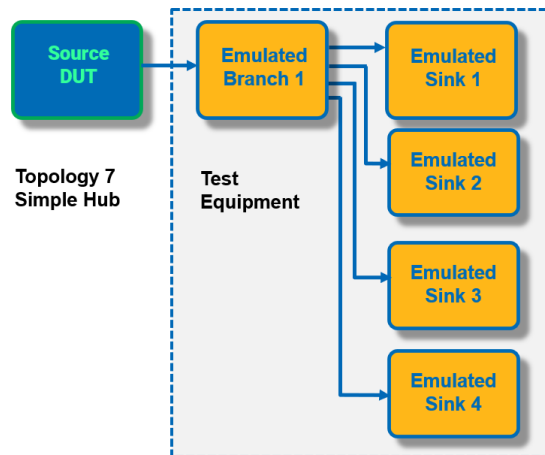
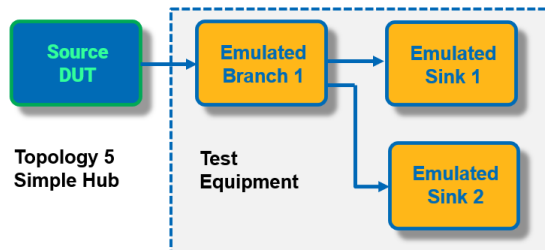
승인된 DP 2.1 컴플라이언스 테스트

소스 디바이스 MST 테스트 설정



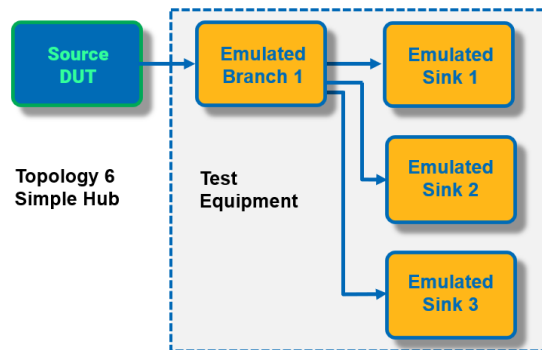
Approved DP 2.1 Compliance Tests

Source Device MST Test Setups



승인된 DP 2.1 컴플라이언스 테스트

소스 디바이스 MST 테스트 설정



MST Source CTS CDF entries

MST 소스 CTS CDF 항목

S.No	CDF Entry	Default Value
1	MST_TRANSMISSION	Yes
2	MST_MAX_STREAM_COUNT	4
3	MST_UP_REQUEST_SUPPORTED	Yes
4	MST_RSN_REQUEST_SUPPORTED	No
5	MST_MAX_DAISY_CHAIN_SINK_SUPPORTED	4
6	MST_POWER_UP_DOWN_PHY_SUPPORTED	Yes

MST Source Device Tests

Main validation points

- Capability read, Link Address, Path Enum Resources, Allocate Payload, Video Validation.
- Connection Status Notification (CSN) Up Request handling for addition, removal.
- Optional Resource Notification (RSN) update handling.
- EDID and NDID read, DSC & FEC capability read.
- Handling of error case (Unknown Up request, NACK, incorrect Down reply or timeout during down reply).
- MST to SST and SST to MST transition.
- In and out of Low Power Mode (Wake/Sleep).
- Writing unique GUIDs.

MST 소스 디바이스 테스트

주요 검증 포인트

- 기능 읽기, 링크 주소, 경로 열거형 리소스, 페이로드 할당, 비디오 유효성 검사.
- 연결 상태 알림(CSN) Up 추가, 제거를 위한 요청 처리입니다.
- 선택적 RSN(리소스 알림) 업데이트 처리.
- EDID 및 NDID 읽기, DSC 및 FEC 기능 읽기.
- 오류 사례 처리(알 수 없는 Up 요청, NACK, 잘못된 Down 응답 또는 다운 응답 중 시간 초과).
- MST에서 SST로, SST에서 MST로 전환합니다.
- 저전력 모드(깨우기/절전)의 안팎.
- 고유한 GUID 작성.



Branch Device Tests

분기 장비 테스트

Approved DP 2.1 Compliance Tests

MST Branch Device tests

- Branch Device Setup 1 (loopback to TE with no External Sink) (6.10.1.1 to 6.10.1.12)
- Branch Device Setup 2 (loopback to TE with 1 External Sink) (6.10.2.1 to 6.10.2.10)
- Branch Device Setup 3 (loopback to TE with 2 External Sink) (6.10.3.1 to 6.10.3.14)
- Branch Device Setup 4 (loopback to TE with 3 External Sink) (6.10.4.1 to 6.10.4.14)
- Branch Device Setup 5 (with 4 External Sink) (6.10.5.1 to 6.10.5.4)

승인된 DP 2.1 컴플라이언스 테스트

MST 분기 디바이스 테스트

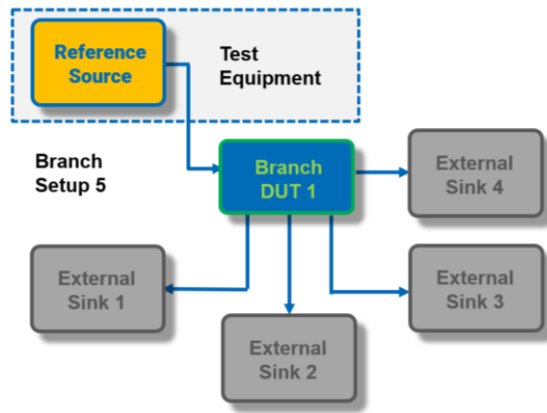
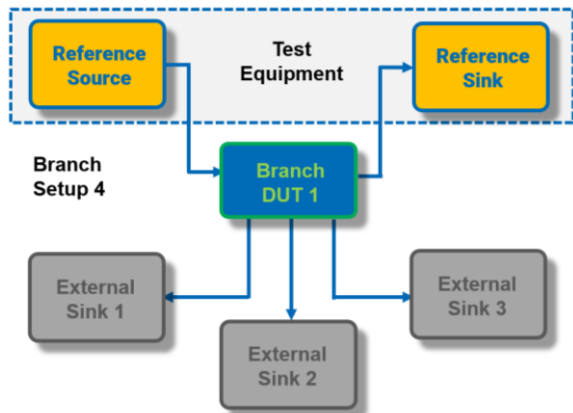
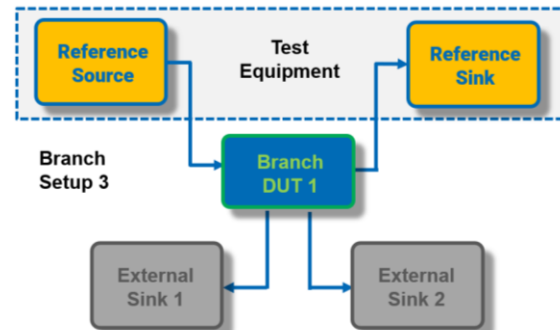
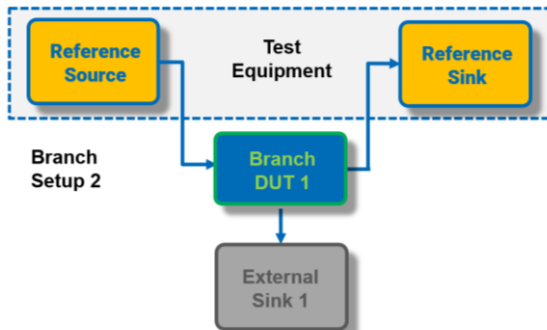
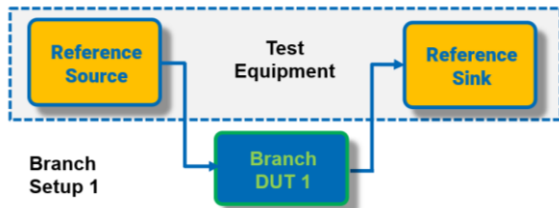
- 분기 디바이스 설정 1(외부 싱크 없이 TE로 루프백)(6.10.1.1 - 6.10.1.12)
- 분기 디바이스 설정 2(외부 싱크 1개를 사용하여 TE로 루프백)(6.10.2.1 - 6.10.2.10)
- 분기 디바이스 설정 3(2개의 외부 싱크를 사용하여 TE로 루프백)(6.10.3.1 - 6.10.3.14)
- 분기 디바이스 설정 4(3개의 외부 싱크가 있는 TE로 루프백)(6.10.4.1 - 6.10.4.14)
- 분기 장치 설정 5(외부 싱크 4개 포함)(6.10.5.1 - 6.10.5.4)

Approved DP 2.1 Compliance Tests

MST Branch Device Test Setups

승인된 DP 2.1 컴플라이언스 테스트

MST 분기 디바이스 테스트 설정



Branch Device CDF entries

분기 디바이스 CDF 항목

S.No	CDF Entry	Default Value	Range
1	BRANCH_DUT_NO_OF_DFP_DPPOINT	0	[1-4]
2	BRANCH_DUT_UFP_PORT_NUM_CONNECTED_TO_TE	0	[1-16]
3	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_TE	0	[1-16]
4	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK1	0	[1-16]
5	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK2	0	[1-16]
6	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK3	0	[1-16]
7	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK4	0	[1-16]
8	BRANCH_DUT_CSN_DFP_BROADCAST	No	Yes/No

Branch DUT tests

Main validation points

- Capability validation, forwards up/down request, response for Enum Path Resources, Query Payload, Video Validation for DSC and Non-DSC video.
- Remote DPCD read/write validation via TE internal memory.
- Timeslots calculation and allocations.
- Response for Remote I2C Read, Remote DPCD read/write, link address request.
- Low Power mode enter/exit.
- CSN Up/down request generation.
- Time slot increase/decrease/delete/addition.

분기 DUT 테스트

주요 검증 포인트

- 기능 유효성 검사, 업/다운 요청 전달, 열거형 경로 리소스에 대한 응답, 쿼리 페이로드, DSC 및 비 DSC 비디오에 대한 비디오 유효성 검사.
- TE 내부 메모리를 통한 원격 DPCD 읽기/쓰기 검증.
- 시간대 계산 및 할당.
- 원격 I2C 읽기, 원격 DPCD 읽기/쓰기, 링크 주소 요청에 대한 응답입니다.
- 저전력 모드 시작/종료.
- CSN 업/다운 요청 생성.
- 시간대 증가/감소/삭제/추가.



MST Composite Sink Device Tests

MST 복합 싱크
장비 테스트

Approved DP 2.1 Compliance Tests

MST Composite Sink Device tests

- Composite Sink Device Setup1 (loopback to TE from DP OUT port) (6.10.6.1 to 6.10.6.22).
- Composite Sink Device Setup2 (loopback to TE from DP OUT port) (6.10.7.1 to 6.10.7.21).
- Composite Sink Device Setup3 (loopback to TE from DP OUT port) (6.10.8.1 to 6.10.8.5).
- Composite Sink Device Setup4 (4 DUTs in Daisy chain) (6.10.9.1 to 6.10.9.3).

승인된 DP 2.1 컴플라이언스 테스트

MST 복합 싱크 장비 테스트

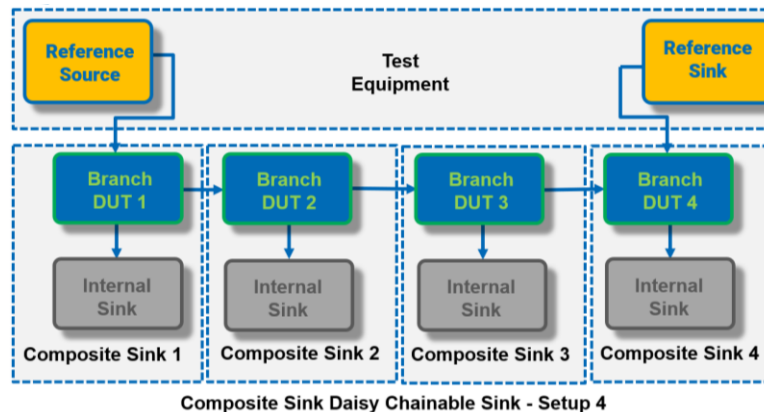
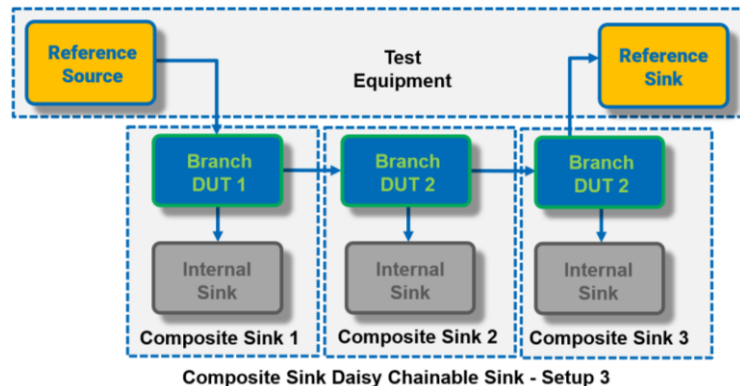
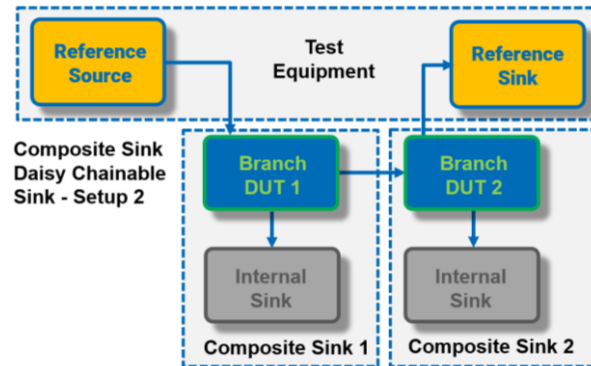
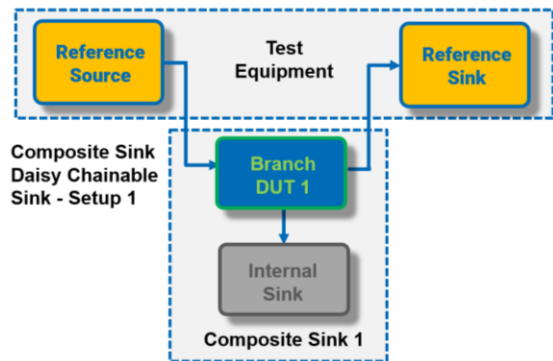
- 복합 싱크 디바이스 설정1(DP OUT 포트에서 TE로 루프백)(6.10.6.1 - 6.10.6.22).
- 복합 싱크 장비 설정2(DP OUT 포트에서 TE로 루프백)(6.10.7.1 - 6.10.7.21).
- 콤포지트 싱크 디바이스 설정3(DP OUT 포트에서 TE로 루프백)(6.10.8.1 - 6.10.8.5).
- 복합 싱크 장비 설정4(데이지 체인의 DUT 4개)(6.10.9.1 - 6.10.9.3).

Approved DP 2.1 Compliance Tests

Composite Sink Device Test Setups

승인된 DP 2.1 컴플라이언스 테스트

복합 싱크 장비 테스트 설정



MST Composite Sink DUT tests

Main validation points

- Capability validation, forward up/down request, response for Enum Path Resources, Query Payload, Video Validation for DSC and Non-DSC video.
- Remote DPCD read/write validation via TE internal memory.
- Timeslots calculation and allocations.
- Response for Remote I2C Read, Remote DPCD read/write, link address request.
- Low Power mode enter/exit
- CSN Up/down request generation.
- Time slot increase/decrease/delete/addition.

MST 복합 싱크 DUT 테스트

주요 검증 포인트

- 기능 유효성 검사, 전달 업/다운 요청, 열거형 경로 리소스에 대한 응답, 쿼리 페이로드, DSC 및 비 DSC 비디오에 대한 비디오 유효성 검사.
- TE 내부 메모리를 통한 원격 DPCD 읽기/쓰기 검증.
- 시간대 계산 및 할당.
- 원격 I2C 읽기, 원격 DPCD 읽기/쓰기, 링크 주소 요청에 대한 응답입니다.
- 저전력 모드 시작/종료
- CSN 업/다운 요청 생성.
- 시간대 증가/감소/삭제/추가.



EDID and NDID Tests

EDID 및 NDID 테스트

Unique Test Numbers

EDID & NDID tests

EDID Tests

- EDID Sink CTS (5.7.15.12) (5.7.16.11).

NDID Tests

- NDID Source CTS (4.7.4.5 to 4.7.4.8) (4.7.5.2)
- NDID Source Adaptive Sync (4.8.1.3 to 4.8.1.4) (4.8.2.4 to 4.8.2.6).
- NDID Sink CTS (5.4.7.10 to 5.4.7.18) (5.7.5.2) (5.7.6.6 to 5.7.6.10) (5.7.7.7 to 5.7.7.12) (5.7.8.7 to 5.7.8.12) (5.7.9.4 to 5.7.9.6) (5.7.10.4 to 5.7.10.6) (5.7.11.6 to 5.7.11.10) (5.7.12.5 to 5.7.12.8) (5.7.14.9 to 5.7.14.16) (5.7.17.6 to 5.7.17.10).
- NDID Sink Adaptive Sync (5.8.1.4 to 5.8.1.6).

고유 테스트 번호

EDID 및 NDID 테스트

EDID 테스트

- EDID 싱크 CTS(5.7.15.12)(5.7.16.11).

NDID 테스트

- NDID 소스 CTS(4.7.4.5 - 4.7.4.8)(4.7.5.2)
- NDID 소스 적응형 동기화(4.8.1.3 - 4.8.1.4)(4.8.2.4 - 4.8.2.6).
- NDID 싱크 CTS(5.4.7.10 - 5.4.7.18) (5.7.5.2) (5.7.6.6 - 5.7.6.10) (5.7.7.7 - 5.7.7.12) (5.7.8.7 - 5.7.8.12) (5.7.9.4 - 5.7.9.6) (5.7.10.4 - 5.7.10.6) (5.7.11.6 - 5.7.11.10) (5.7.12.5 - 5.7.12.8) (5.7.14.9 - 5.7.14.16) (5.7.17.6 - 5.7.17.10).
- NDID 싱크 적응형 동기화(5.8.1.4 - 5.8.1.6).



New Tests in CTS Rev 1.1

CTS Rev 1.1의 새로운 테스트

New Test Additions in Rev 1.1

Source Tests:

- 4.2.2.15 Verification of DPCD 110h Values on USB-C Cable Connect with Source DUT before Link Training.

Sink Tests:

- 5.2.2.11 Verification of DPCD 2217h Values on Upstream Device Disconnect and Power-on Reset.

Rev 1.1의 새로운 테스트 추가 사항

소스 테스트:

- 4.2.2.15 링크 교육 전에 소스 DUT와 USB-C 케이블 연결의 DPCD 110h 값 확인.

싱크 테스트:

- 5.2.2.11 업스트림 장치 분리 및 전원 켜기 재설정 시 DPCD 2217h 값 확인.



Updated Tests in CTS Rev 1.1

CTS Rev 1.1의 업데이트된 테스트

Test Updates in Rev 1.1

Source Device Tests

- Link Training Tests -
INTRAHOP_AUX_REPLY_INDICATION check before UHBR Link Training. If set only then Source driver shall write DPCD 102h=00h to clear it, else do not write 102h=00h to clear intra hop as it is already clear. This change affects all UHBR Link Training procedure validation.
- Link Training Tests - Same Link Configuration retry 1 time or 2 times, controlled by CDF and affect all Link Training fallback tests.

Rev 1.1의 테스트 업데이트

소스 장치 테스트

- 링크 트레이닝 테스트 – UHBR 링크 트레이닝 전에
INTRAHOP_AUX_REPLY_INDICATION 확인하십시오. 설정된 경우에만 소스 드라이버는 DPCD 102h=00h를 작성하여 지우고, 그렇지 않으면 이미 지워져 있으므로 인트라 홉을 지우기 위해 102h=00h를 작성하지 마십시오. 이 변경 사항은 모든 UHBR 링크 트레이닝 절차 검증에 영향을 미칩니다.
- 링크 트레이닝 테스트 – 동일한 링크 구성은 CDF에 의해 제어되며 모든 링크 트레이닝 대체 테스트에 영향을 주는 1회 또는 2회 재시도합니다.

Test Updates in Rev 1.1

Source Device Tests (continued)

- 4.3.1.21 update for 20 loop or max time budget during EQ loop not able to achieve EQ lock.
- 4.2.2.13 update check defer after LTTTPR discovery.
- 4.9.1.22 LTTTPR discovery check validation handling after HPD may not be the first transaction.
- 4.3.3.2 Least pack format change for 1L UHBR10 for video test.
- Minor update in 4.7.5.1.

Rev 1.1의 테스트 업데이트

소스 장치 테스트(계속)

- 4.3.1.21 20주기 또는 EQ 주기 동안 최대 시간 예산에 대해 EQ 잠금 업데이트가 불가능합니다.
- 4.2.2.13 LTTTPR 검색 후 업데이트 확인이 지연됩니다.
- 4.9.1.22 HPD 이후의 LTTTPR 검색 확인 유효성 검사 처리는 첫 번째 트랜잭션이 아닐 수 있습니다.
- 4.3.3.2 비디오 테스트용 1L UHBR10의 포장 형식은 가장 적게 다릅니다.
- 4.7.5.1의 사소한 업데이트

Test Updates in Rev 1.1 Sink Device Tests

- 5.2.2.5 DPCD Address Range - Do not check Vendor Specific fields
- 5.3.1.5 Successful Link Training at Lower Link Rate/Bandwidth Due to Loss of Symbol Lock during Channel Equalization Sequence - EQ Done bit validation removed. Only use Symbol lock for validation.
- Some Sink Tests will be skipped if DP Tunnel is detected.
- Minor update in 5.7.14.1 EDID – DTD Type X Block Revision (Byte #1).
- Minor updates in 5.6.2.[12/13/14] – DSC Interrupt tests.

Rev 1.1의 테스트 업데이트 싱크 장비 테스트

- 5.2.2.5 DPCD 주소 범위 - 공급업체별 필드가 선택되지 않았습니다.
- 5.3.1.5 채널 이퀄라이제이션 시퀀스 중 심볼 잠금 손실로 인해 더 낮은 링크 속도/대역폭에서 성공적인 링크 트레이닝 - EQ 전체 비트 검증이 제거되었습니다. 확인을 위해 기호 잠금만 사용합니다.
- DP 터널 감지되었습니다.
- 5.7.14.1 EDID – DTD 유형 X 블록 개정판(바이트 #1)의 사소한 업데이트.
- 5.6.2의 사소한 업데이트. [12/13/14] – DSC 인터럽트 테스트.

Test Updates in Rev 1.1

LTPR Device Tests

- 7.1.1.4 Phy Repeater Link Rate Validation test
- Wait for 10 second cable unplug before switching to Non-LTPR Mode. Update clarification for Tunnel working as retimer.
- 7.1.5.1 LTPR 8b/10b DP Symbol Error Validation Test, With 0 Emulated LTPRs, Symbol Error Counter Validation at Max Supported Lane Count and 8b/10b DP Link Rate - Correction of Symbol error counter setting on LTPR Address range, not the sink DPCD.

Rev 1.1의 테스트 업데이트

LTPR 장치 테스트

- 7.1.1.4 PHY 리피터 링크 속도 검증 테스트 - 비 LTPR 모드로 전환하기 전에 케이블이 분리될 때까지 10초 동안 기다리십시오. 리타이머로서의 터널에 대한 설명을 업데이트했습니다.
- 7.1.5.1 시뮬레이션된 LTPR이 0인 LTPR 8b/10b DP 심볼 오류 검증 테스트, 지원되는 최대 채널 수 및 8b/10b DP 링크 속도에서 심볼 오류 카운터 검증 - 수신기 DPCD가 아닌 LTPR 주소 범위의 심볼 오류 카운터 설정을 수정합니다.

Questions?

질문?

DisplayPort Electrical Testing Overview

Jim Choate

VESA Compliance Program Manager

10/31/2025

Agenda

- DP2.1 Electrical Compliance Test Requirements
- DP2.1 PHY Updates
- DP2.1 Transmitter Test
- DP2.1 Receiver Test
- eDP PHY Electrical Conformance Testing

DP2.1a Electrical Compliance Test Requirement

DisplayPort Interface

Main Link

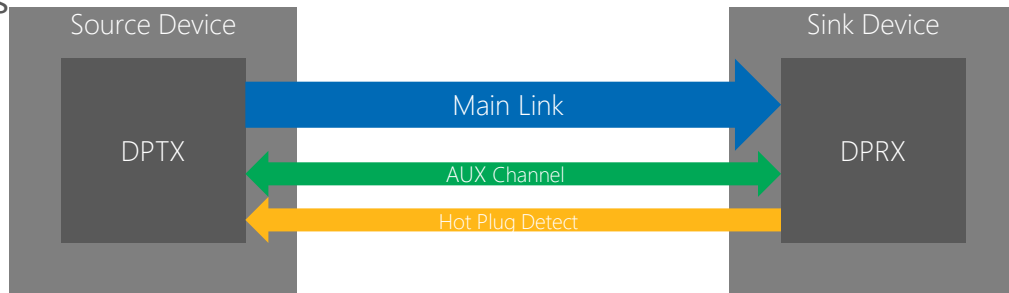
- Display data transfer
- 4 unidirectional high-speed lanes
- Multiple bitrates supported

AUX Channel

- Link management
- Test mode control
- 1 bidirectional low-speed lane

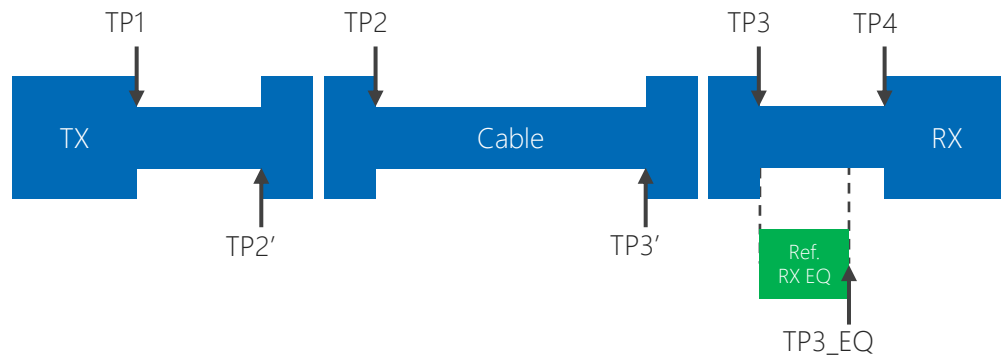
Hot Plug Detect

- Source detects presence of sink
- Sink notifies of status changes via IRQ



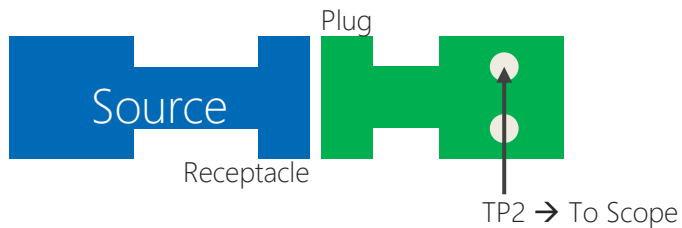
Test Points

Test Point	Definition
TP1	Source transmitter pins.
TP2	Test interface of a TPA, next to mated connection to a DP source.
TP2'	RX JTOL signal injection point for DUTs with plug.
TP2_CTLE	RX JTOL calibration and test point for DUTs with plug.
TP3	Test interface of a TPA, next to mated connection to a DP sink.
TP3'	Signal injection point to a DP sink.
TP3_EQ	TP3 using a defined DP cable model with equalization applied.'
TP3_CTLE	TP3 using a defined HBR3 cable model with CTLE applied.
TP3_DFE	TP3 using a defined HBR3 cable model with CTLE and DFE applied.
TP4	Sink receiver pins.

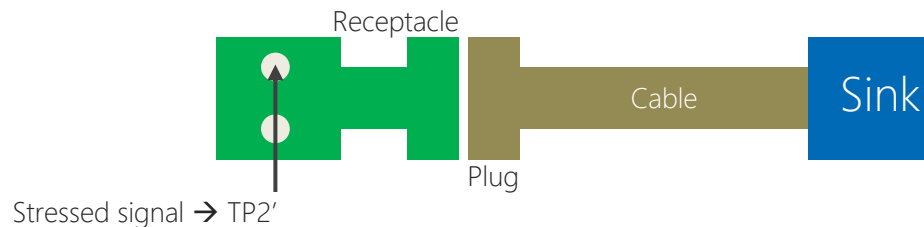
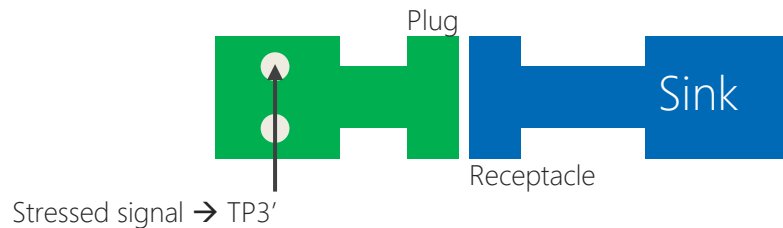


Test Point Access Examples

DPTX Testing



DPRX Testing



How to test the PHY layer?

Source

- Configure the source to output test patterns with certain drive settings → **AUX controller**
- Embed worst-case channels, apply equalization on the oscilloscope
- Run measurements

Sink

- Generate the stress signal with a pattern generator
- Guide the sink through Link Training → **AUX controller**
- Read built-in error counter → **AUX controller**

DP2.1 PHY Updates

Electrical Updates from DP2.1 to DP2.1a to DP2.1b

- There are minimal changes in 8b/10b electrical compliance testing.
- A new DP54 cable has been introduced in DP2.1a for UHBR13.5.
- The UHBR13.5 Source Enhanced FSDP testing will utilize the new DP54 cable model.
- A new DP80LL cable has been introduced in DP2.1b for UHBR20.
- The UHBR20 Source with 9dB loss budget will utilize the DP80LL cable.
- Changes in test limits primarily affect Source Testing.

- UHBR10
 - DPTX TP2
 - Total Jitter = 380 mUI
 - Data-Dependent Jitter = 160 mUI
 - Eye Width = 600 mUI
 - Eye Height = 242 mV
- UHBR13.5
 - DPTX TP2
 - Eye Height = 185 mV
 - DPTX TP3_EQ
 - Total Jitter = 450 mUI
 - Data-Dependent Jitter = 200 mUI
 - Eye Width = 540 mUI
 - Eye Height = 115 mV
 - DPRX TP3_EQ
 - Total Jitter = 485 mUI
 - Data-Dependent Jitter = 240 mUI
 - Eye Width = 540 mUI
 - Eye Height = 112 mV
- UHBR20
 - DPTX TP2
 - Total Jitter = 435 mUI
 - Data-Dependent Jitter = 200 mUI
 - Eye Width = 540 mUI
 - Eye Height = 240 mV
 - DPTX TP3_EQ
 - Total Jitter = 455 mUI
 - Data-Dependent Jitter = 210 mUI
 - Eye Width = 560 mUI
 - Eye Height = 100 mV
 - DPRX TP3_EQ
 - Data-Dependent Jitter = 255 mUI
 - Eye Width = 520 mUI
 - Eye Height = 96 mV



- UHBR10
 - DPTX TP2
 - Total Jitter = 440 mUI
 - Data-Dependent Jitter = 220 mUI
 - Eye Width = 550 mUI
 - Eye Height = 162 mV
 - UHBR13.5
 - DPTX TP2
 - Eye Height = 200 mV
 - DPTX TP3_EQ
 - Total Jitter = 515 mUI
 - Data-Dependent Jitter = 245 mUI
 - Eye Width = 520 mUI
 - Eye Height = 80 mV
 - DPRX TP3_EQ
 - Total Jitter = 530 mUI
 - Data-Dependent Jitter = 260 mUI
 - Eye Width = 520 mUI
 - Eye Height = 73 mV
 - UHBR20
 - DPTX TP2 EnhDP
 - Total Jitter = 495 mUI
 - Data-Dependent Jitter = 220 mUI
 - Eye Width = 530 mUI
 - Eye Height = 170 mV
 - DPTX TP3_EQ EnhDP
 - Total Jitter = 510 mUI
 - Data-Dependent Jitter = 242 mUI
 - Eye Width = 550 mUI
 - Eye Height = 84 mV
 - DPRX TP3_EQ EnhDP
 - Data-Dependent Jitter = 265 mUI
 - Eye Width = 510 mUI
 - Eye Height = 80 mV
- DPTX TP2 USB-C
 • Total Jitter = 480 mUI
- DPTX TP3EQ USB-C
 • Total Jitter = 500 mUI

- UHBR20

- DPTX TP2 EnhDP

- Total Jitter = 495 mUI
 - Data-Dependent Jitter = 220 mUI
 - Eye Width = 530 mUI
 - Eye Height = 170 mV

- DPTX TP3_EQ EnhDP

- Total Jitter = 510 mUI
 - Data-Dependent Jitter = 242 mUI
 - Eye Width = 550 mUI
 - Eye Height = 84 mV

- DPRX TP3_EQ EnhDP

- Data-Dependent Jitter = 265 mUI
 - Eye Width = 510 mUI
 - Eye Height = 80 mV

DPTX TP2 USB-C

- Total Jitter = 480 mUI

DPTX TP3EQ USB-C

- Total Jitter = 500 mUI



- UHBR20

- DPTX TP2 EnhDP DP80

- Total Jitter = 480 mUI
 - Data-Dependent Jitter = 200 mUI
 - Eye Width = 540 mUI
 - Eye Height = 240 mV

- DPTX TP2 EnhDP DP80LL

- Total Jitter = 495 mUI
 - Data-Dependent Jitter = 220 mUI
 - Eye Width = 530 mUI
 - Eye Height = 170 mV

- DPTX TP3_EQ for all connector Type

- Total Jitter = 500 mUI
 - Data-Dependent Jitter = 210 mUI
 - Eye Width = 560 mUI
 - Eye Height = 100 mV

- DPRX TP3EQ for all connector type

- Data-Dependent Jitter = 255 mUI
 - Eye Width = 520 mUI
 - Eye Height = 96 mV

DP2.1 PHY CTS Errata

- Clarification on 8b/10b SSC Modulation Deviation Limit
- Test fixture insertion loss update
- FFE Preset 15 measurement update
- LTTPR Frequency Variation test update
- Eye Height and Mask requirement update for UHBR Rates
- BERT Preset Calibration

DP2.1 Transmitter Test

Electrical Transmitter Tests

Item	Name	Normative/ Informative
3.1	Eye Diagram Test	Normative
3.2	HBR/RBR Non-PE Level Verification Test	Normative
3.3	HBR/RBR PE Level Verification and Maximum Differential Peak-to-Peak Voltage Test	Normative
3.4	HBR3/HBR2 PE Level and Equalization Verification Test	Normative
3.5	HBR3/HBR2 $V_{TX_DIFF-P_MAX}$ Test	Normative
3.6	Inter-pair Skew Test	Informative
3.7	Intra-pair Skew Test	Informative
3.8	AC Common Mode Noise Test	Informative
3.9	Non-ISI Jitter Measurement Test	Normative
3.10	HBR3 TX Differential RL Test	Informative
3.11	TJ/RJ/DJ Measurement Tests	Normative
3.12	Main-Link Frequency Compliance Test	Normative
3.13	Spread-spectrum Modulation Frequency Test	Normative
3.14	Spread-spectrum Modulation Deviation Test	Normative
3.15	dF/dT Spread-spectrum Deviation High-frequency Variation Test	Informative
xx	Embedded Re-timer Frequency Variation Test	Normative

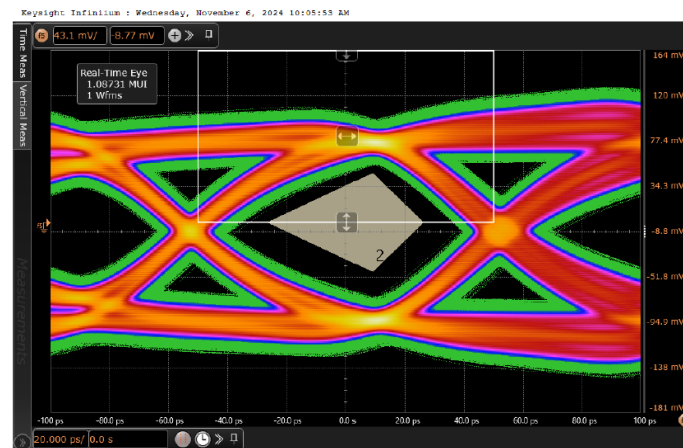
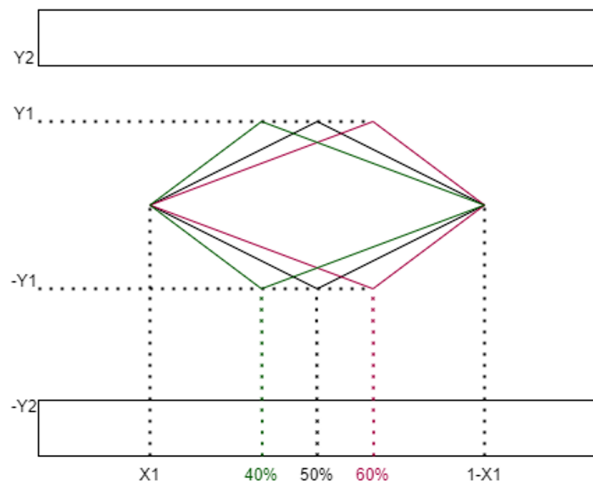
8b/10b

Item	Name	Normative/ Informative
4.2	Preset and CTLE-DFE Declaration	Normative
4.3	UHBR Source Transmitter Equalization	Normative
4.4	UHBR Bit Rate	Normative
4.4	UHBR Unit Interval	Informative
4.5	UHBR SSC Down Spread Range, Rate, Phase Deviation, and Slew Rate	Normative
4.6	UHBR Embedded Re-timer Frequency Variation	Informative
4.7	UHBR TP2 Eye at 1E-6 BER	Normative
4.8	UHBR TP2 Jitter at 1E-9 BER	Normative
4.9	UHBR AC Common Mode Noise Test	Informative
4.10	UHBR TP3_EQ Eye at 1E-6	Normative
4.11	UHBR TP3_CTLE Jitter at 1E-9	Informative
4.12	UHBR Transmitter Return Loss	Informative

128b/132b

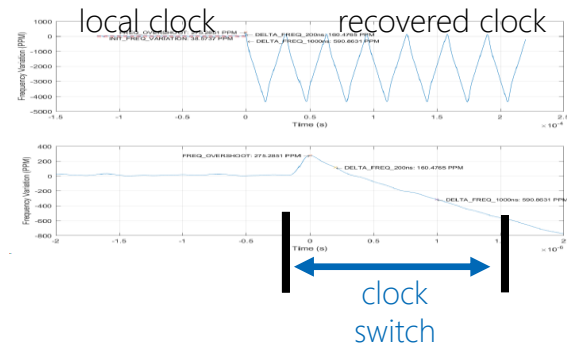
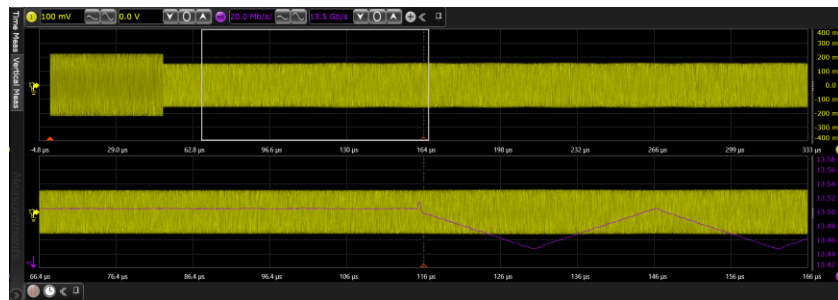
UHBR Eye Mask Update

- If original eye mask fails, then modified mask will be used to re-test.
- Modify mask must comply the Y1 and X1 as per the DP 2.1 PHY CTS



LTTPr Frequency Variation Test

- LTTPrs are needed as total channel loss increases with the PHY rate
 - Longer channel
 - More complex link training
- LTTPr Re-timer Clock Switch Test Mode
 - DPCD 0x0010B – 0x0010Eh [7] =1
- Initial Test Challenges
 - **Entering** Clock Switch test mode
 - **Triggering** on LTTPr local clock event



DP TX testing challenges

- The test time for DP TX is significant
- DP Source not supporting PHY Test Automation
 - DP Source does not transmit the compliance pattern
- VESA is currently discussing DP TX and DP RX reduced PHY test plan for reducing test time

DP2.1 Receiver Test

Electrical Receiver Tests

Item	Name	Normative/ Informative
5.1	8b/10b DP Sink JTOL Test	Normative

Item	Calibration Point	Name
5.1.3.1.1	TP1-TP3	HBR3 Jitter Calibration
5.1.3.1.2	TP1-TP3	HBR2 Jitter Calibration
5.1.3.1.3	TP1-TP3	HBR Jitter Calibration
5.1.3.1.4	TP2/TP3	HBR3 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR2 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR Eye Height and Total Jitter Calibration
5.1.3.1.5	TP1/TP3	HBR3/HBR2/HBR Crosstalk Calibration
5.1.3.2	TP2/TP3	RBR Jitter Calibration
5.1.3.2	TP3	RBR Eye Height Calibration
5.1.3.2.1	TP3	RBR Crosstalk Calibration

Item	Name	Normative/ Informative
6.1	128b/132b DP UHBR Sink JTOL Test	Normative

Item	Calibration Point	Name
6.1.3.1.4.1	TP1	AC Common-Mode Interference Calibration
6.1.3.1.4.2	TP1	Random Jitter Calibration
6.1.3.1.4.3	TP1	Periodic Jitter Calibration
6.1.3.1.4.4	TP1	Total Jitter Calibration
6.1.3.1.4.5	TP1	Eye Height Calibration
6.1.3.1.5	TP3	Insertion Loss Calibration
6.1.3.1.6	TP3	Eye Diagram Calibration

BERT Preset Calibration

- To verify the BERT FFE as outlined in the DP 2.1 PHY CTS specification
- The Preset calibration check can assist in identifying setup problems.

Set	Preset []	Expected Preshoot [dB]	Measured Preshoot [dB]	Expected Deemphasis [dB]	Measured Deemphasis [dB]	Coeff_1 []	Coeff0 []	Coeff1 []	Pass/Fail
1		0.00	0.10	-1.90	-1.75	0.030	0.870	-0.100	Pass
2		-3.10	-3.16	-3.60	-3.57	0.130	0.690	-0.180	Pass
3		0.00	0.03	-5.00	-4.81	0.030	0.750	-0.220	Pass
4		0.00	-0.20	-8.40	-8.25	0.030	0.655	-0.315	Pass
5		0.90	1.13	0.00	0.20	-0.035	0.965	0.000	Pass
6		1.10	1.18	-1.90	-1.86	-0.020	0.880	-0.100	Pass
7		1.40	1.35	-3.80	-3.60	-0.020	0.810	-0.170	Pass
8		1.70	1.65	-5.80	-5.61	-0.020	0.750	-0.230	Pass
9		2.10	2.03	-8.00	-7.89	-0.020	0.690	-0.290	Pass
10		1.70	1.82	0.00	0.13	-0.080	0.920	0.000	Pass
11		2.20	2.49	-2.20	-2.24	-0.080	0.820	-0.100	Pass
12		2.50	2.31	-3.60	-3.47	-0.060	0.790	-0.150	Pass
13		3.40	3.57	-6.70	-6.64	-0.070	0.700	-0.230	Pass
14		3.60	3.67	0.00	0.01	-0.170	0.830	0.000	Pass

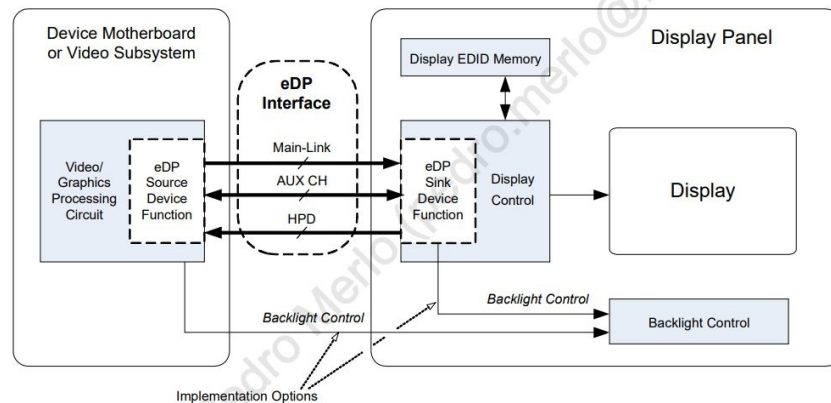
DP RX testing challenges

- Error count registers not enabled in DP Sink
 - Error count register always report 0 errors
 - USB-C Lane orientation causing failure in error counter and link training
- Calibrations take a significant amount of time
 - Different setup needs for 8b/10b and 128b/132b

Embedded DisplayPort

eDP

- Standardized features and interoperability guidelines
 - Feature set determined by the system integrator
- Current specification is eDP2.0
 - Based on DP2.1
- No compliance program = Conformance Test!!



eDP2.0 Update

- eDP2.0 v1.0 published in September 2024
- Supports 128b/132b encoding
- Supports UHBR data rates
 - UHBR10, UHBR13.5 and UHBR20
- Leverages worst-case end-to-end link budget from DP2.1

Key Differences eDP2.0 vs DP2.1

Required

- DPCD registers for eDP
- Reduced AUX timing
- Enhanced framing
- Fast link training (sink)
- eDP-specific sink noise/jitter budget, reference EQ

Optional

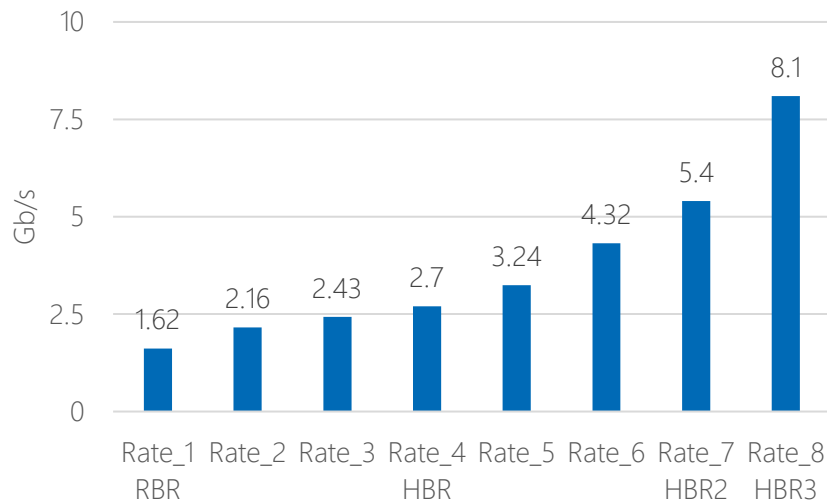
- Low AUX voltage swing
- Source detection by way of AUX CH
- STREAM_STATUS_CHANGED bits support
- GUID registers support
- Fast link training (host)
- Reduced main-link voltage swing level
- EDID
- HPD pin on sink device

Recommended

- Fewest number of lanes possible

Main Link Differences

- Eight 8b/10b rates, and Three UHBR rates
- Custom rates supported



- TP3_EQ total jitter budget
- $BER = 10^{-9}$

Test Point	Description	I/N	DJ _{MAX}	TJ _{MAX}
TP1	eDPTX package pin	Informative	0.17 UI	0.27 UI
TP2	Source device eDP cable connector	Informative	N/A	N/A
TP3	Sink device (panel) eDP cable connector	-	-	-
TP3_EQ	After reference RX equalizer	Normative	0.41 UI	0.50 UI
TP4	eDPRX package pins	Informative	0.46 UI	0.55 UI

AUX Channel Differences

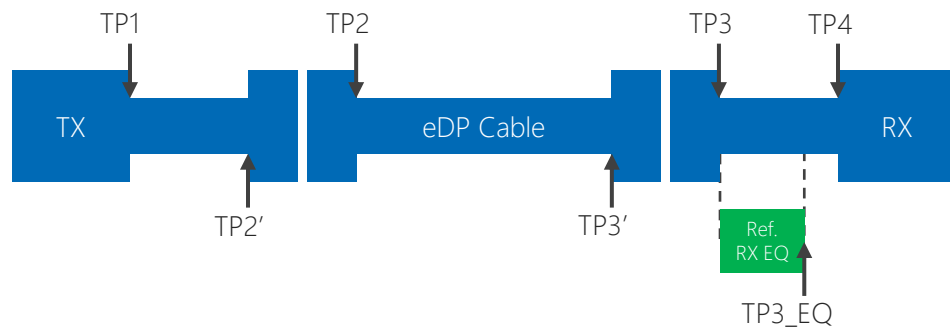
- No AC-coupling capacitors on Sink device side
- No pull-up/-down resistors
- Why?
 - The Sink device does not monitor the common mode voltage on AUX_CH_P and AUX_CH_N for Source device Hot Plug/Unplug and powered/unpowered detection

eDP Electrical Specification

- Low voltage swing levels
- Framework to apply optional customized voltage swings
- Reduced RX differential voltage sensitivity
- New transfer rates
- Framework to apply jitter specifications to optional customized frequencies
- Same Link Training procedures and voltage swing tables like DP, but with lower signal voltages

eDP Transmitter Test

- Test Point/Fixture

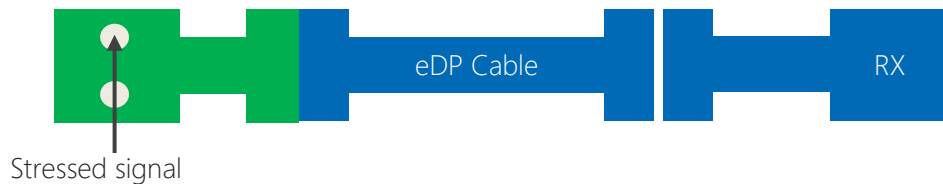


Recommended Source Main-Link TX Electrical Specification

Link Rate
Unit Interval
Total Jitter
Residual ISI
Non-ISI
Eye Diagram

eDP Receiver Test

- Test Point/Fixture



RX Test
Sink JTOL Test

Calibration Point	RX Calibration
TP1	Sinusoidal Jitter Calibration
TP1	Random Jitter Calibration
TP3	Residual ISI
TP3	Eye Diagram
TP3	Crosstalk

Thank You!

DP2.1 Panel Replay and Advanced Link Power Management: Implementation and Testing Challenges

Sergey Grushin

Unigraf Oy

October 2025

Agenda

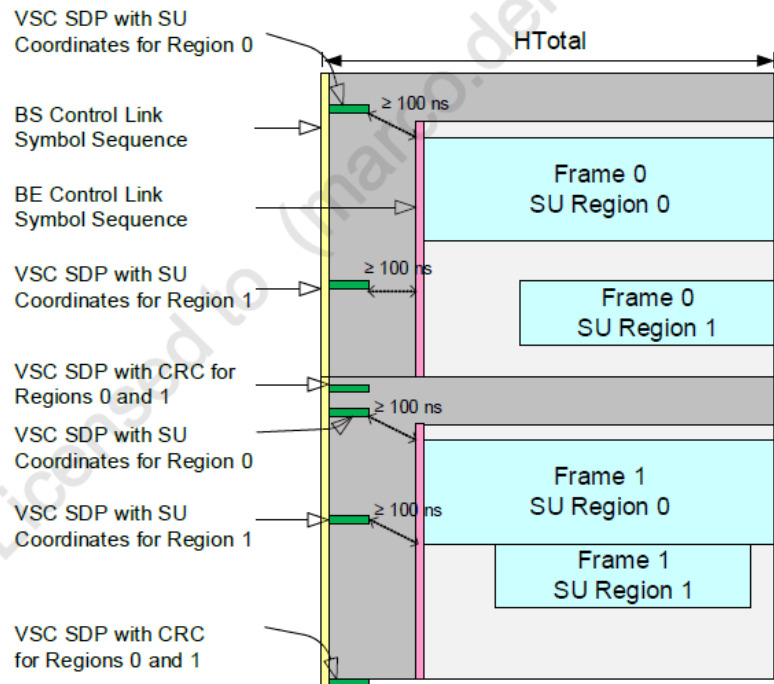
- Saving power with Panel Replay (PR)
- Saving power with Advanced Link Power Management (ALPM)
- Interaction with FEC, MST and HDCP

DisplayPort system-level power conservation

- Optional Panel Replay (PR) can be enabled to turn the Main Link off when no data is being transferred and save power.
- When PR is in Active state, the Sink will use the image captured in its Remote Frame Buffer (RFB) to refresh the display.
- During PR Active state, the Source can either continue to transmit a frame-rate-governed video timing (discarded by the Sink) or, optionally, turn the Main Link off.
- Optional Main Link power on/off management uses Advanced Link Power Management (ALPM) in AUX-less mode.

Panel Replay overview

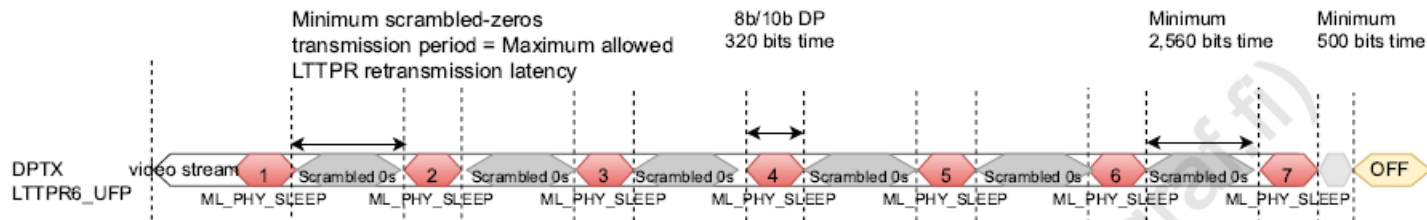
- Transitions between Live Frame mode and PR Active state happen using VSC SDPs.
- The Source can transmit a Full Frame update, or one or more smaller Selective Update (SU) Regions, each starting at their respective video scan line position.
- SU Region coordinates and dimensions are defined using a VSC SDP transmitted at least 100ns before the start of the SU region.
- After a SU Region, the Source may optionally transmit a VSC SDP containing the CRC accumulated for all of the SU Regions of the frame.
- Optional SU Region Early Transport support: the first SU Region is transmitted starting from the first active video scan line instead of its real position. The following regions are transmitted preserving the relative distance between them.



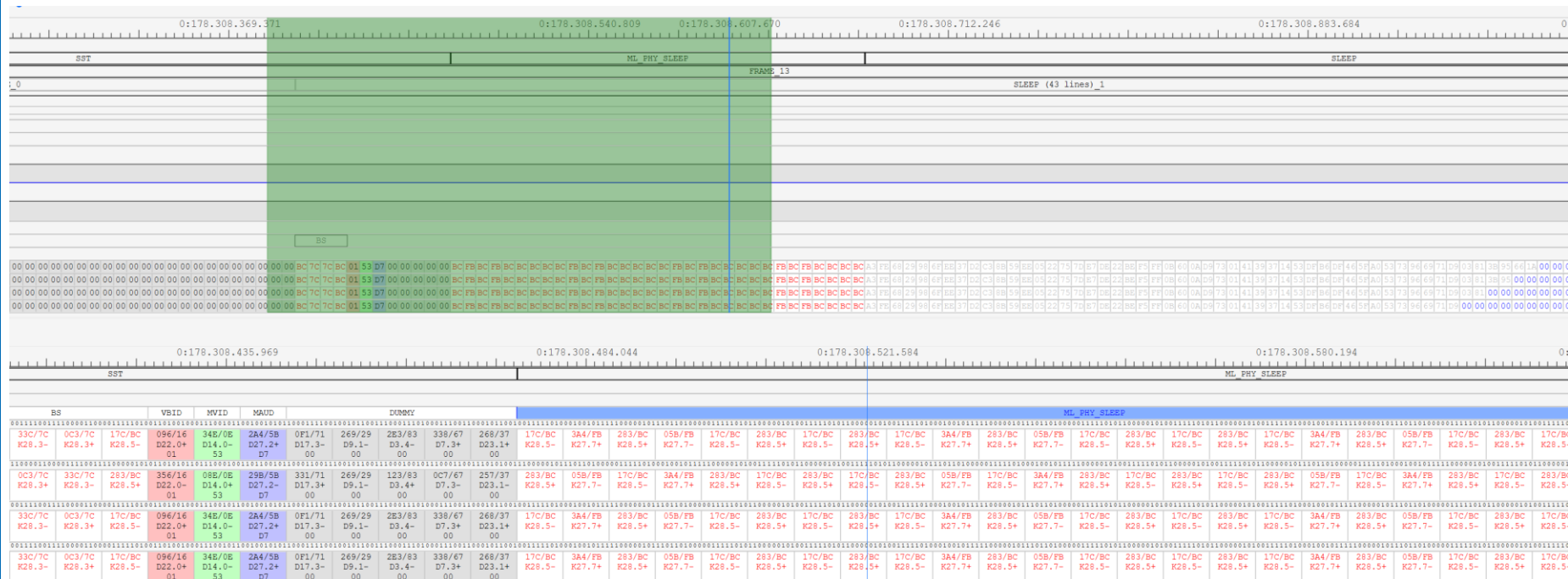
ALPM: Main Link Power-off

- The Source uses the ML_PHY_SLEEP sequence followed by scrambled zeroes to signal LTTPrs and Sink that the Main Link will be powered-off.
- The ML_PHY_SLEEP sequence consists of:
 - 8b/10b: a sequence of [K28.5, K27.7, K28.5, K27.7, K28.5, K28.5, K28.5, K28.5], with correct disparity
 - 128b-132b: a special 129-bit supersymbol [CDI=1 + 89898989h, 89898989h, 89898989h, 89898989h]. CDI is XORed according to standard rules, then precoded
- The Source transmits four consecutive ML_PHY_SLEEP sequences followed by scrambled 0s:
 - Once for each connected LTTPr
 - Once for the Sink

- The ML_PHY_SLEEP sequence must not overwrite BS+VBID, MSA, SDP data or FEC control link symbols.
- The Sink must look for two consecutive ML_PHY_SLEEP sequences and allow for max 4 symbol errors within them.
- Mandatory minimum ALW_SLEEP time after power-off sequence: 15us



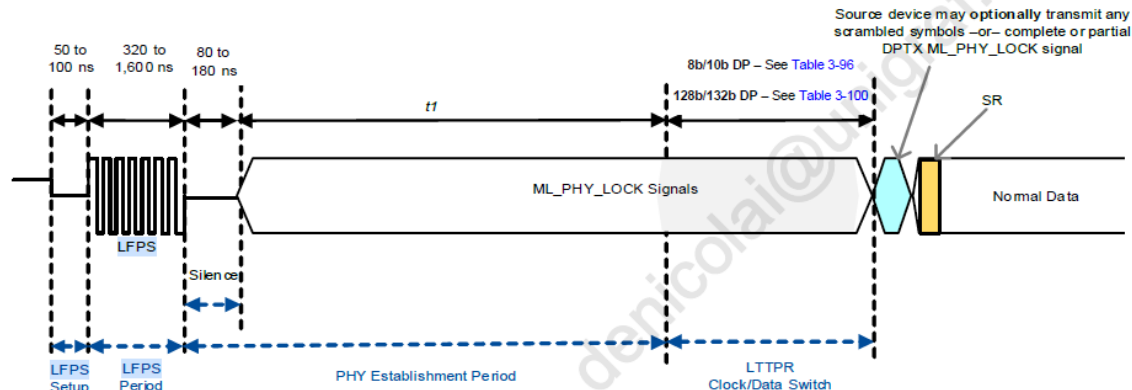
ALPM: Main Link Power-off (cont.)



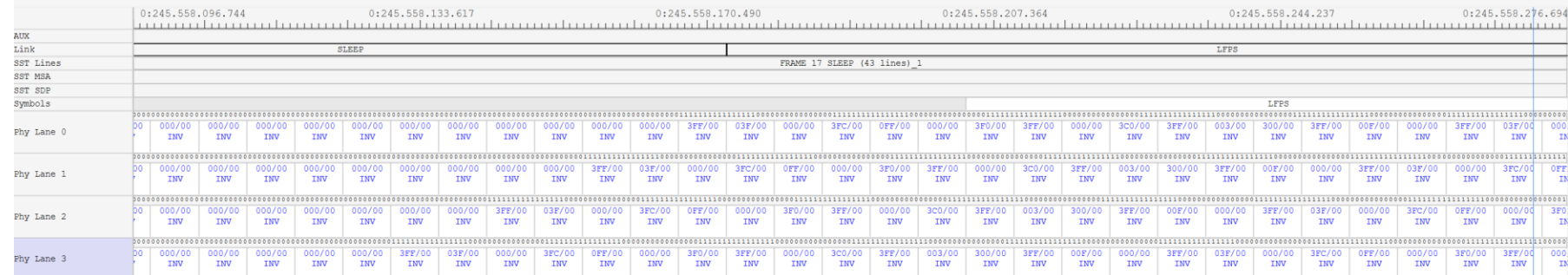
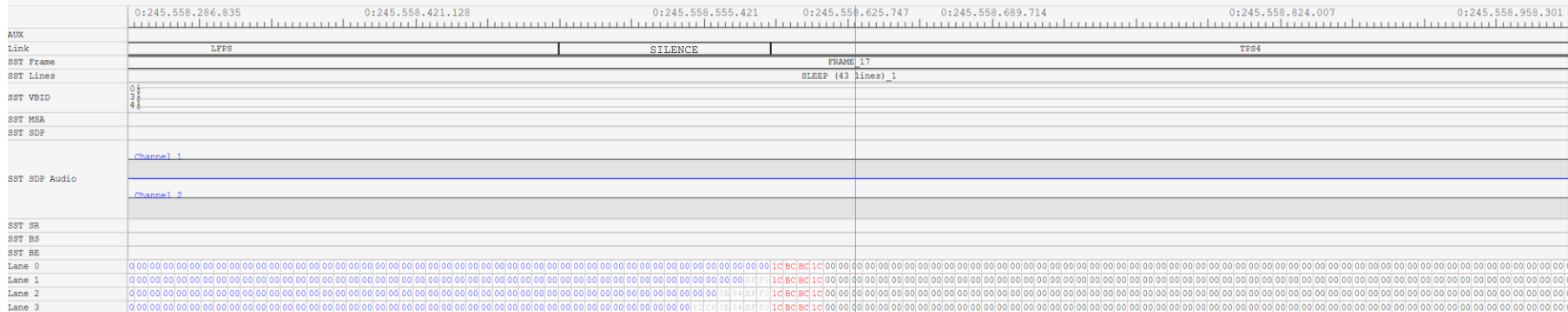
ALPM: Main Link Power-on (aka “wake”)

- The Source uses the ML_PHY_WAKE sequence to signal LTTPrs and Sink that the Main Link has been powered back on.
- The ML_PHY_WAKE sequence is composed by LFPS period (square wave at 12.5...50 MHz, at least 16 pulses, no more than 1.6us long) followed by a silence period and ML_PHY_LOCK pattern.
- ML_PHY_LOCK pattern:
 - 8b/10b – same as TPS4
 - 128b/132b – same as 128b_132b_TPS2 but with reduced intervals between LT_SCRAMBLER_RESET symbols (4 logical frames instead of 16)

- LFPS can have different common mode voltage amplitude than the ML data. Switch to ML common mode voltage is performed during the silence period
- The shortest duration of ML_PHY_LOCK is 50us. The Sink must complete EQ adaptation within this time. This is significantly shorter than usual link training



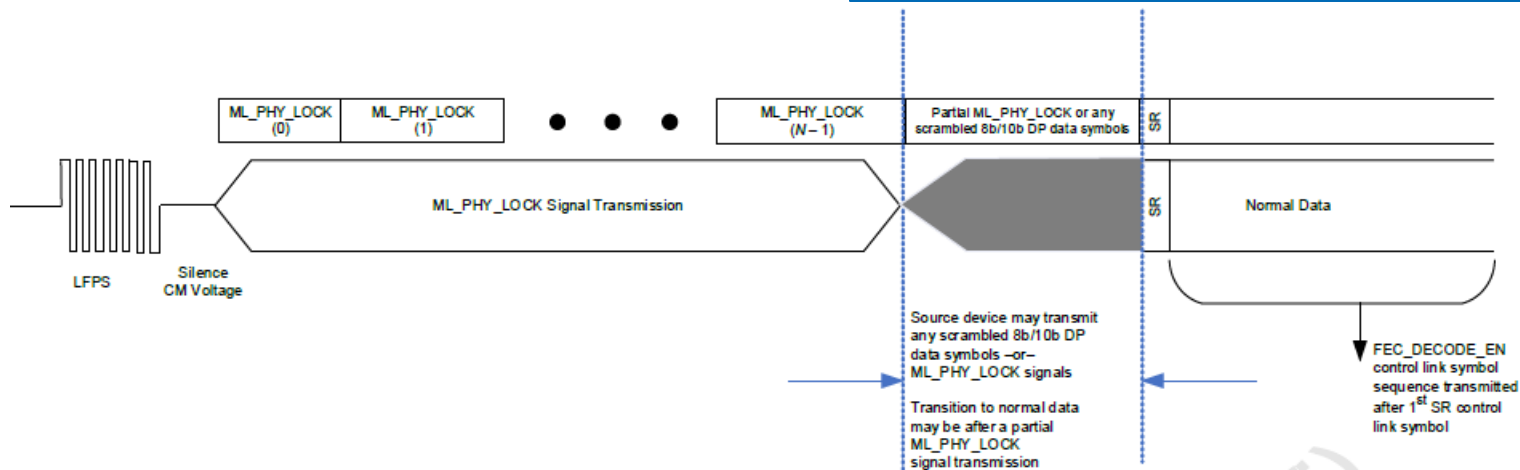
ALPM: Main Link Power-on (cont.)



8b/10b FEC support

- In 8b/10b mode, FEC is not mandatory for ALPM. However, it is mandatory for Panel Replay.
- FEC block structure is maintained during the power-off sequence
- On the Sink side, FEC is considered disabled after power-off. Source must re-enable it by transmitting the FEC_DECODE_EN sequence after ML_PHY_LOCK pattern.

- The FEC block containing the final part of power-off sequence's scrambled 0s may be left incomplete. Sink must handle this situation correctly.
- The Sink cannot disable its FEC Decoder right when ML_PHY_SLEEP is detected but needs to wait for the last FEC block data to be decoded, since it could contain e.g. the tale of the last video frame transmitted.

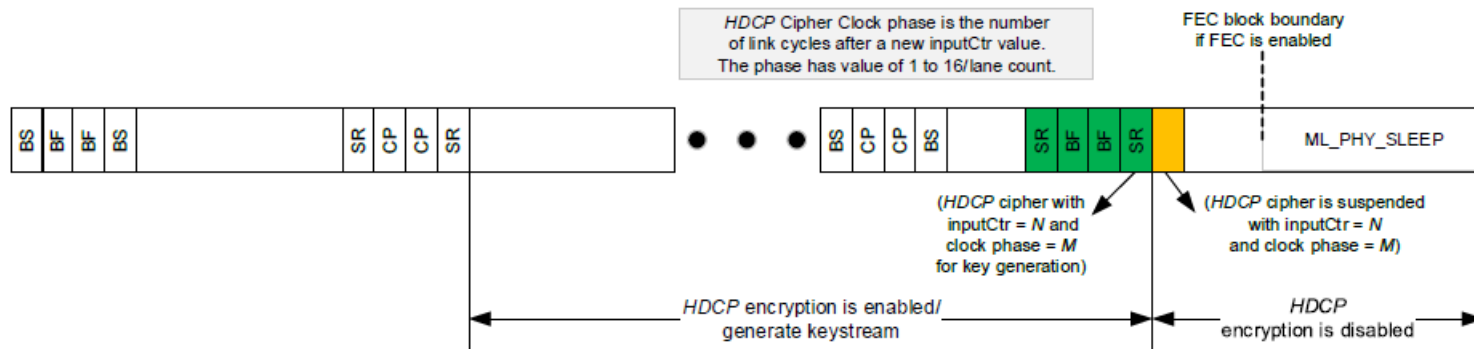


MST support

- During power-off sequence, ML_PHY_SLEEP is transmitted using all time slots.
- Source must be careful not to overwrite important data such as BS and VBID with ML_PHY_SLEEP in allocated slots.
- After power-on sequence, MST is started after the ML_PHY_LOCK pattern with an MST SR symbol.

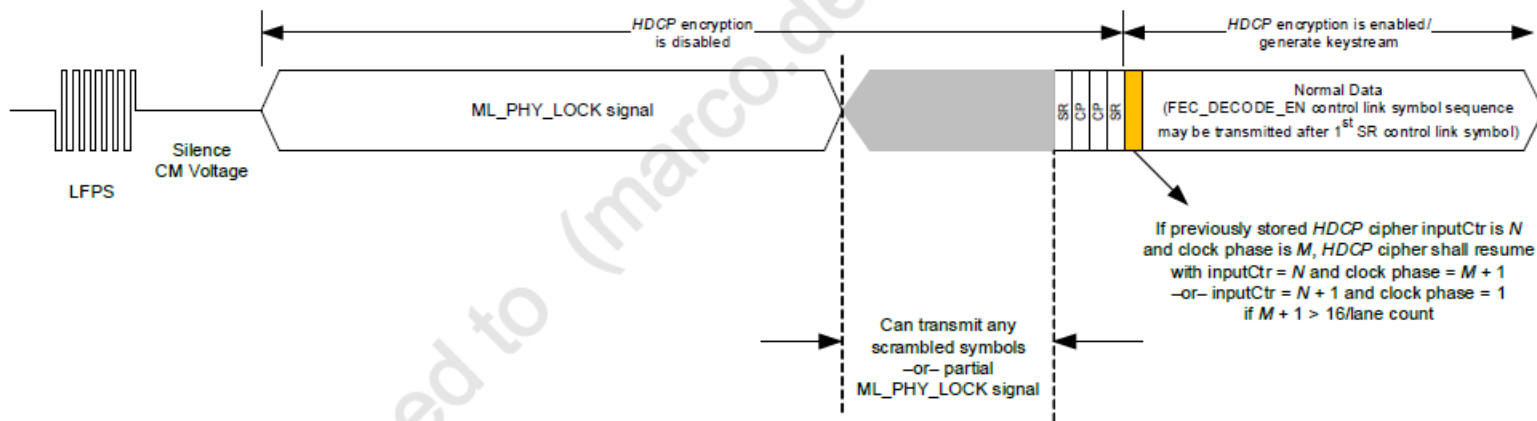
HDCP support

- Only HDCP r2.3 (or higher) is supported with AUX-less ALPM.
- HDCP is suspended before ML_PHY_SLEEP, HDCP cypher is frozen.



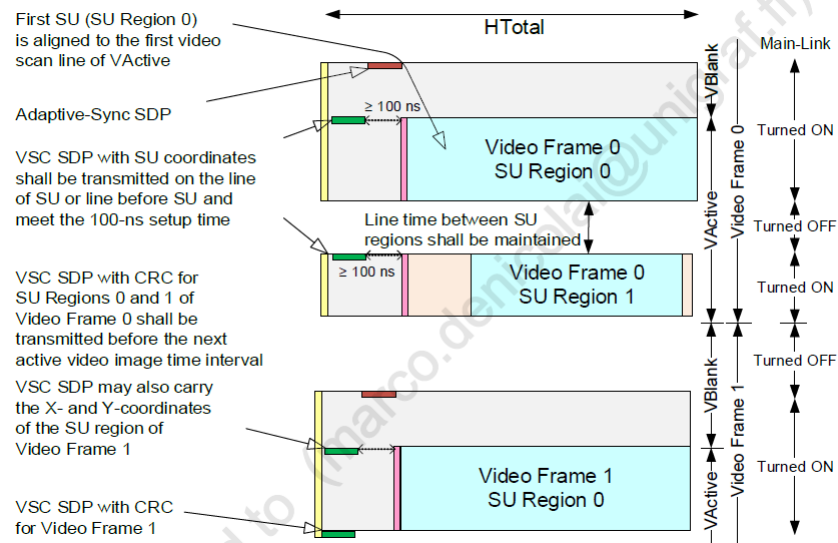
HDCP support (cont.)

- After power-on, HDCP is resumed and decryption continues from the previously frozen state, without the need for re-authentication.
- For 8b/10b SST and 128b/132b, encryption suspend and resume procedure is straightforward. For 8b/10b MST it is more complicated.



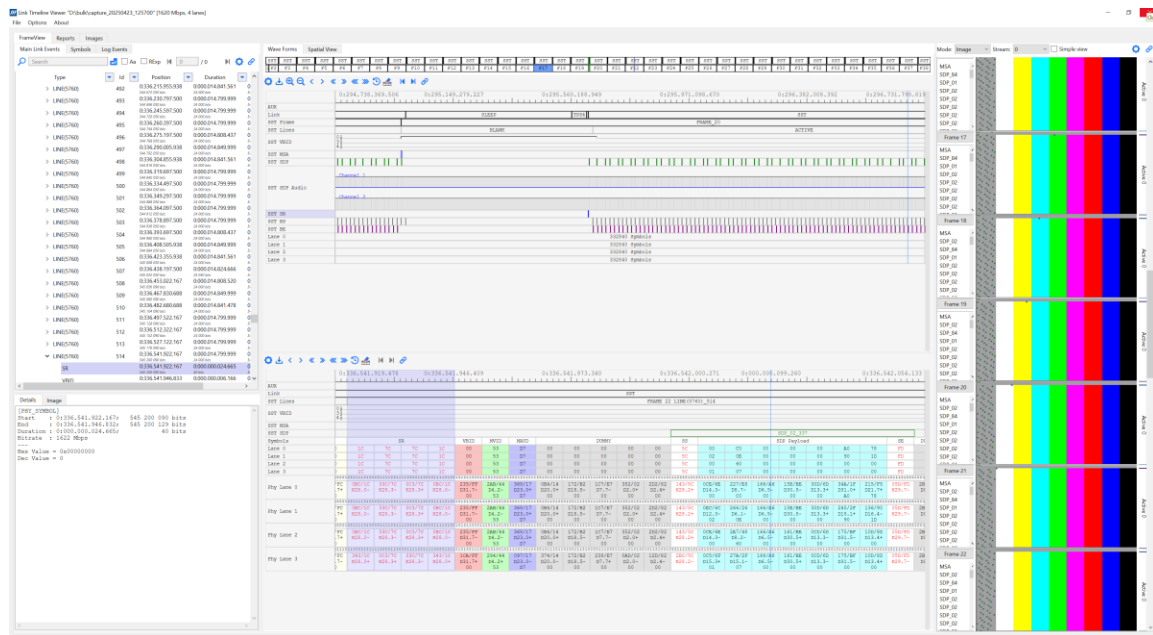
Panel Replay with ALPM

- When PR is in Active state, the Main Link can stay powered (option 1-A) or can be powered-off (option 1-C) using ALPM
- When ALPM is used, Sink and Source video timing synchronization is maintained using Adaptive-Sync SDPs, for each frame and at the same position.
- When ALPM is used, Early Transport is mandatory.
- Power-off is possible between SU regions, but the line interval still must be maintained.



DP Link Analyzer

A Unigraf tool for capturing Main-link Data Events and AUX Transactions. Within each frame, users can have a deep view of the events and metadata that occurs in each line. Measure distances in nanoseconds and symbol size to identify the length of problems in between events. Observe descrambled and scrambled symbols in hexadecimal format in each of the active lanes.



Demo Tables

Teledyne LeCroy Test Solutions for DisplayPort v2.1



M42de 80G Video Analyzer/ Generator



Teledyne LeCroy
7F., No. 667, Bannan Rd
Zhonghe Dist, New Taipei City 235
Taiwan
Phone: +886-2-8228-6100

protocolsales@teledynelecroy.com

Teledyne LeCroy DisplayPort Test Platforms

■ Quantumdata M42de Analyzer / Generator

- DisplayPort 1.4 & 2.1 (UHBR) Lane Rates
- DP80 and USB Type-C[®] connectors
- Deep Capture / Analysis
- T.A.P.4[™] Passive Monitoring
- Comprehensive DP 1.4 & 2.1 Compliance Coverage
 - Link, DSC, LTTPR, EDID & MST
- qdPrime[™] Automated Test Suite

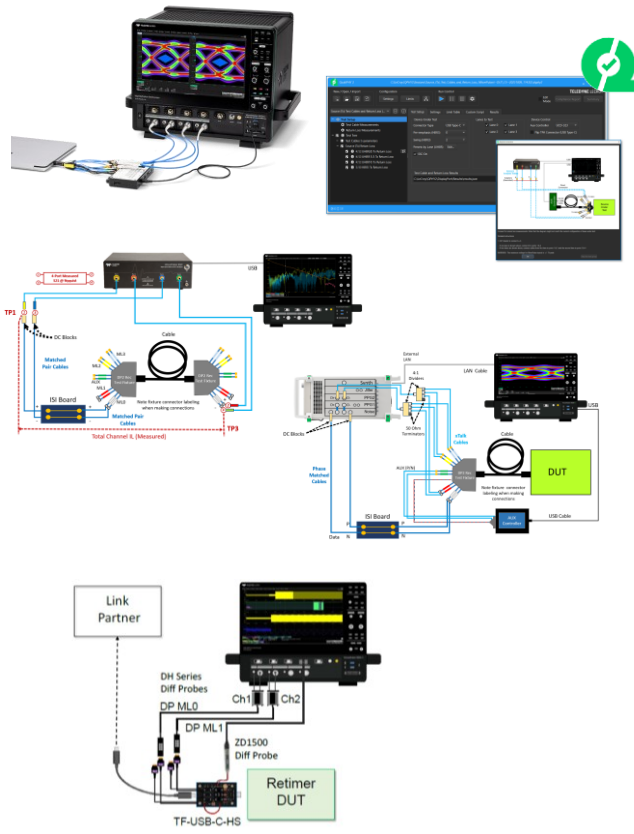


■ Quantumdata M21 Analyzer

- Portable DP Analyzer & HDMI Analyzer / Generator
- DisplayPort Source Testing only (up to UHBR 13.5Gb/s)
- AUX Channel Monitoring



DisplayPort 2.1 PHY Compliance and PHY-Logic Debug



- DisplayPort 2.1 Source (Tx) Compliance
 - WaveMaster/SDA 8000HD with QualiPHY® 2 software
 - SDAX-DP expert analysis – Find Best CTLE/DFE
 - Reduced test times with QPHY2-PC
 - Automated Return Loss with WavePulser 40iX
- DisplayPort 2.1 Sink (Rx) Compliance
 - WaveMaster/SDA 8000HD with QualiPHY 2 software
 - SSG Cal and BER testing using Anritsu MP1900 SQA
 - Automated Channel Cal with WavePulser 40iX
- PHY-Logic (Interop) Debug
 - AUX Triggered + Main Link capture
 - TF-USB-C-HS – probing access
 - DP-AUX, USB-PD TDMP software
 - Clock switch testing on live link



Unigraf DisplayPort and USB-C Test Solutions

UCD-500 Gen2



16K DP 2.1 Generator & Analyzer

- DP 2.1 Link Layer CTS Tool
- DP 2.1 Sinks and Sources up to 8K@60Hz (UHBR 20Gbps / Lane) and 16K@60Hz with DSC
- Featuring Link Analyzer, Panel Replay and eDP test functions

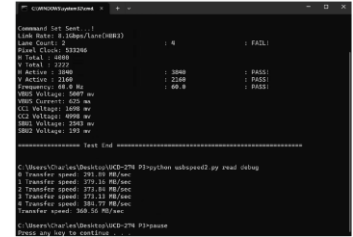


UTC-274



USB-C Test Automation Tool

- Test DP Alt Mode, Power Delivery and USB Speed
- Support EPR function up to 240W Source and Sink
- Test USB-C connector pins soldering and assembly quality with a single cable insertion





DisplayPort Alt Mode Compliance Testing and Analysis solutions

Ellisys USB/DPAM Test and Analysis Solutions

USB Explorer™ 350



Multi-function USB Type-C®, USB 3.2,
and Power Delivery Protocol Test Platform

VESA-Approved Tester for DisplayPort ALT Mode



Type-C Tracker™



Protocol and Electrical Analysis Tool
for USB Type-C® Standards

Includes DP AUX and DP ALT Support



GRL DisplayPort

DP2.1 Tx PHY Test Solution

DP2.1 Rx PHY Test Solution

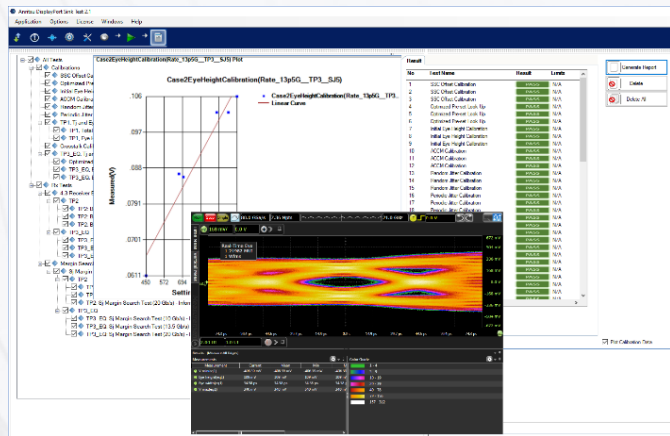
DPAM Test Solution



GRL Test Solution

GRL Solutions

DisplayPort 2.1 Tx/Rx Test Automation Solution



USB Type-C® Power Delivery Tester & Analyzer - EPR



- USB Power Delivery Specification 3.2
- Type-C® Functional Specification
- IEC Functional Safety (IEC 62368-1)
- **DisplayPort™ Alternate Mode Tests**
- Thunderbolt 3/4/5 Alternate Mode Tests
- Thunderbolt 3/4/5 Power Tests
- Qualcomm® Quick Charge 2™
- Qualcomm® Quick Charge 3™ and 3+™
- Qualcomm® Quick Charge 4™ and 4+™
- Qualcomm® Quick Charge 5™
- BC 1.2 for QC Sink products
- IEC 63680-1-2

The only instrument you need for validating compliance, interoperability, and reliability of your designs

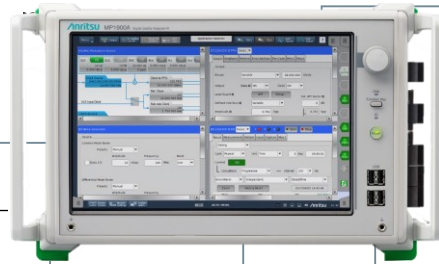


MP1900A Signal Quality Analyzer

High Speed Bus SINK Compliance Solution

MP1900A Standalone

Multi-channel BER Measurement
High-quality PPG
High-input-sensitivity ED
PAM3/4 BER Measurements



Thunderbolt
4/5&DP1.4/2.1 Rx Test
Stressed Signal Calibration and
Stressed Signal Input Test

USB Link Sequence Generation
Transition to Loopback mode

Jitter Tolerance Test
SJ/RJ/BUJ Injection
Low-rate estimated BER measurement

Stressed Signal Calibration
PCI Express Link Sequence Generation
Transition to Loopback Mode
Pass/Fail evaluation using BER measurement

Calibration of stressed signal*

Transition DUT state to Loopback

Stressed Receiver Testing

MX183000A Software

Stressed Signal Calibration*

USB Link Sequence Generation Function

PCI Express Link Sequence Generation Function

Stressed Signal Input Test Function

Jitter Tolerance Test

Auto-receiver Test Function

MP1800A Hardware

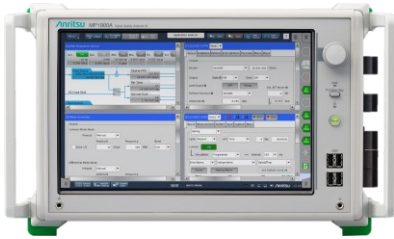
Up to 32 Gbit/s, 8ch

High Quality Signal

Jitter
Emphasis

MP1900A Signal Quality Analyzer

DP1.4/2.1 SINK Compliance Test Structure



MP1900A Standalone

- Multi-channel BER Measurement
- High-quality PPG
- High-input-sensitivity ED
- PAM3/4 BER Measurements
- DP1.4/2.1 and USB4v1&v2 Compliance test Support

Lunch

Wordly AI

Scan the QR Code for real-time captions & translation



VESA DisplayHDR Overview and Test Method

Do Kyun Kim (keneth.kim@lge.com)

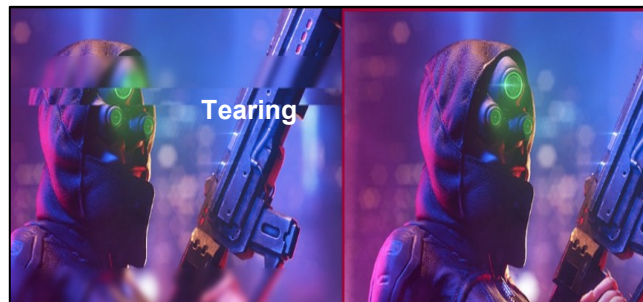
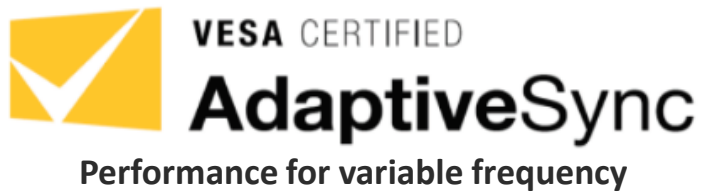
LG Electronics, Inc.

31 Oct 2025

Agenda

- HDR Technology
- DisplayHDR CTS1.2 Overview
- DisplayHDR CTS1.2 Test

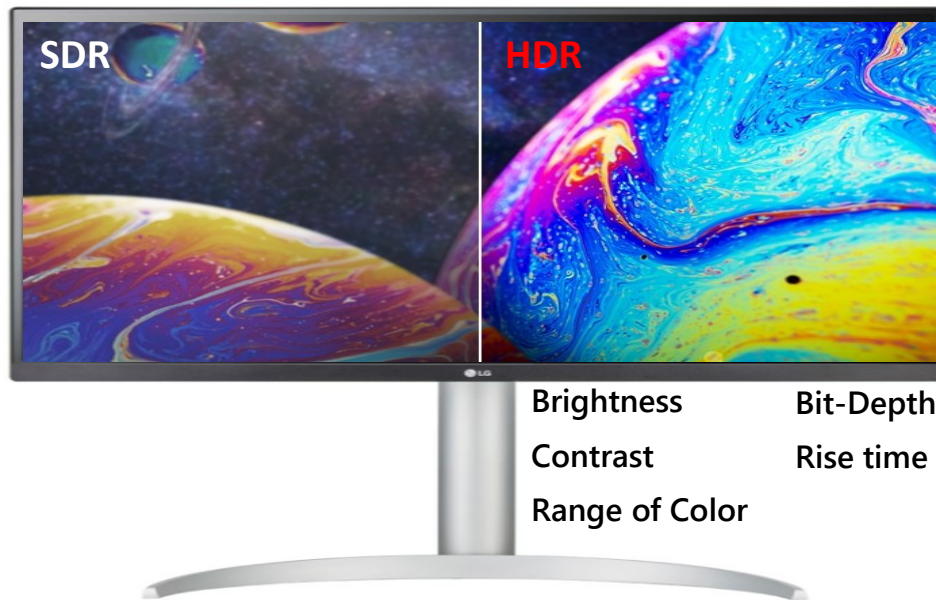
VESA Display Logo



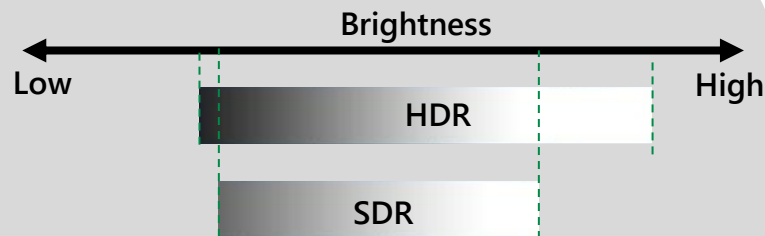
DisplayHDR

High Dynamic Range

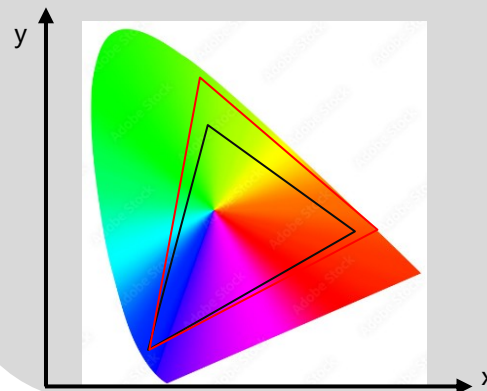
- Display Performance Measurement Standard for HDR (Industry)



1. Brightness & Contrast & Bit-Depth



2. Range of Color & Bit-Depth



HDR Main Parameter

Data Byte number	Contents	Group
Data Byte 3	display primaries x[0], LSB	1
Data Byte 4	display primaries x[0], MSB	
Data Byte 5	display primaries y[0], LSB	
Data Byte 6	display primaries y[0], MSB	
Data Byte 7	display primaries x[1], LSB	
Data Byte 8	display primaries x[1], MSB	
Data Byte 9	display primaries y[1], LSB	
Data Byte 10	display primaries y[1], MSB	
Data Byte 11	display primaries x[2], LSB	
Data Byte 12	display primaries x[2], MSB	
Data Byte 13	display primaries y[2], LSB	
Data Byte 14	display primaries y[2], MSB	
Data Byte 15	white_point x, LSB	2
Data Byte 16	white_point x, MSB	
Data Byte 17	white_point y, LSB	
Data Byte 18	white_point y, MSB	
Data Byte 19	max_display_mastering_luminance, LSB	3
Data Byte 20	max_display_mastering_luminance, MSB	4
Data Byte 21	min_display_mastering_luminance, LSB	
Data Byte 22	min_display_mastering_luminance, MSB	5
Data Byte 23	Maximum Content Light Level, LSB	
Data Byte 24	Maximum Content Light Level, MSB	6
Data Byte 25	Maximum Frame-average Light Level, LSB	
Data Byte 26	Maximum Frame-average Light Level, MSB	

HDR Static Metadata Descriptor Type 1(CTA-861)

ST.2086 Container(HDR10)

4. Corner test for Total Contrast
Measure in the center box
Nits: 270.00 HDR10: 625
Press SPACE to hide this text.



Displayed HDR Test Tool

MaxCLL: 270 MaxFALL: 27 MinCLL: 0.000000 Gamut: Native

Mastering Luminance

: Maximum and Minimum Luminance of a 10% Patch
Used in Mastering Display

MaxCLL

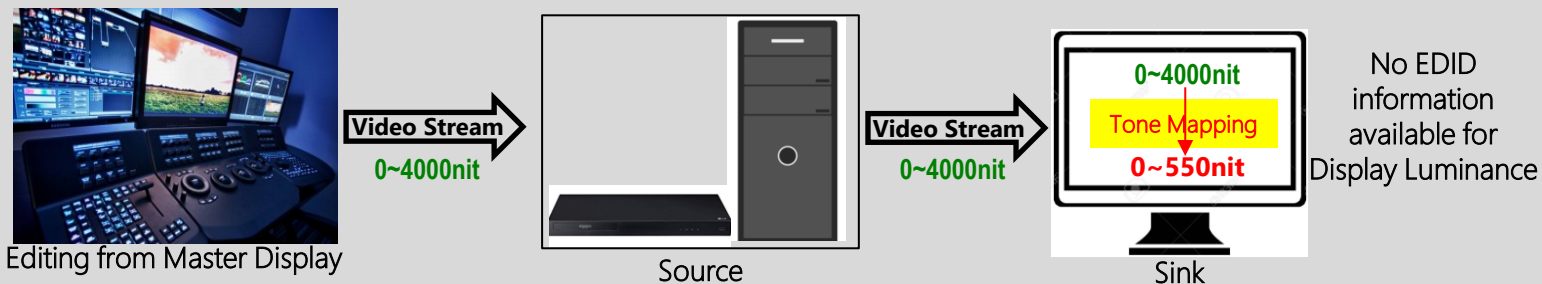
: Maximum Luminance Level per Single Pixel

MaxFall

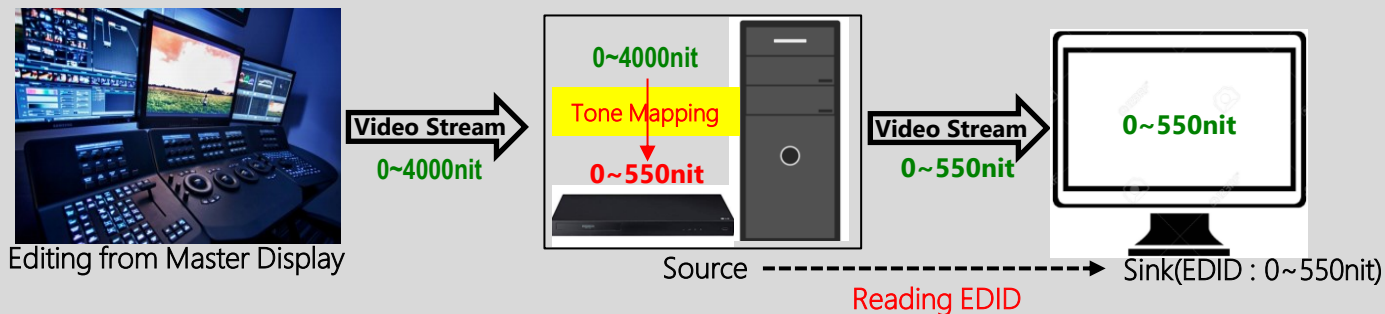
: Average Luminance of All Pixels in a Single Frame

HDR Tone Mapping

Tone Mapping *by the Sink*



Tone Mapping *by the Source*



HDR Rendering

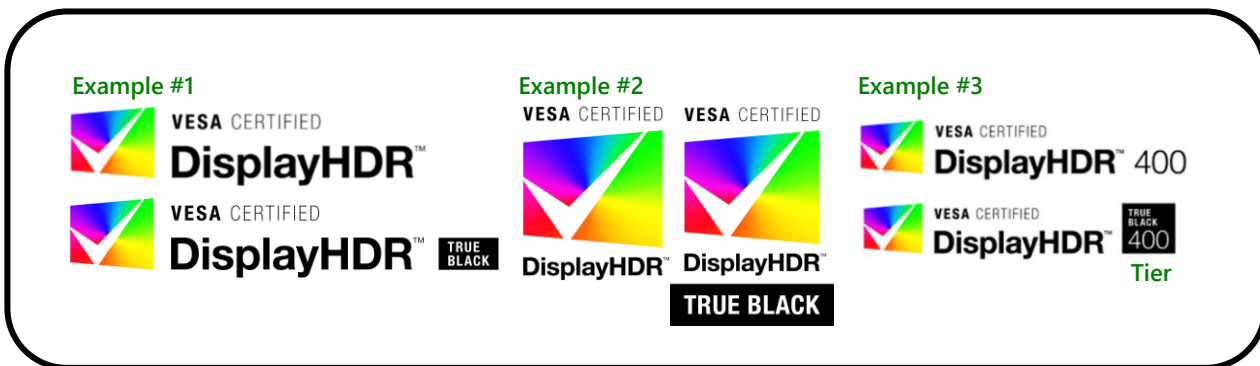
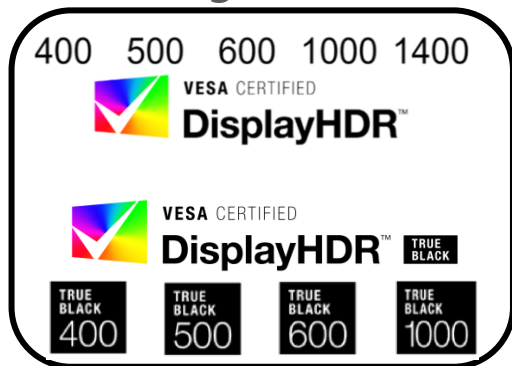


- **Movies & Dramas:** Color tones and master luminance are defined by the creator using a master display.
- **Games & PC OS:** Metadata is generated directly from the source content.

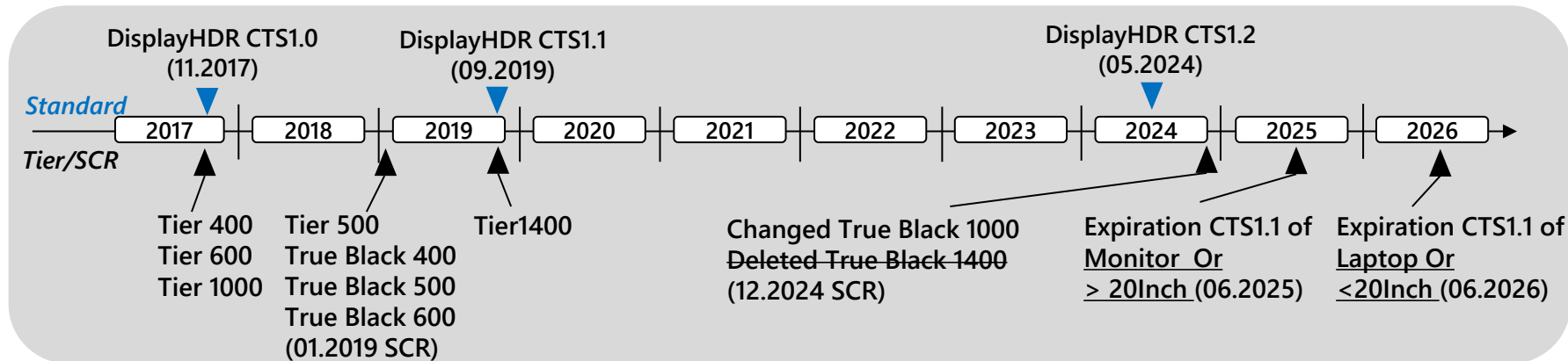


DisplayHDR CTS

- Tier/Logo



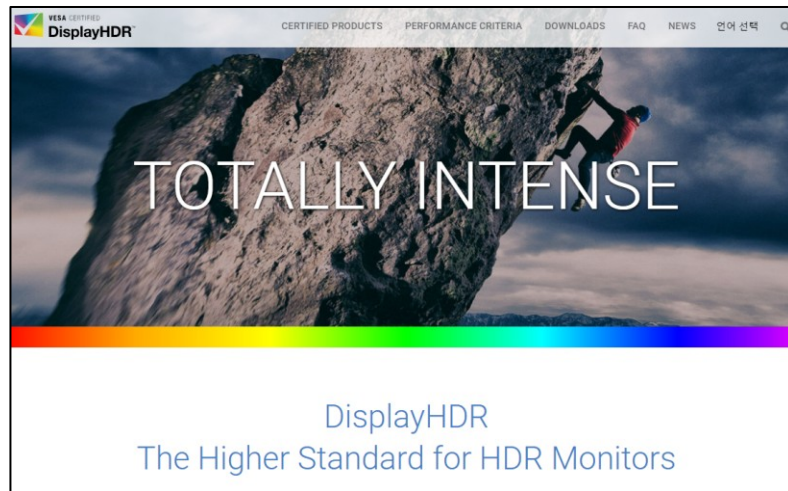
- History



Certificated Products

Tier	2024.10	2025.10	Growth Rate
DisplayHDR 400	714	885(+171)	23.95%
DisplayHDR 500	18	31(+13)	72.22%
DisplayHDR 600	101	132(+31)	30.69%
DisplayHDR 1000	126	164(+38)	30.16%
DisplayHDR 1400	12	22(+10)	83.33%
DisplayHDR True Black 400	89	167(+78)	87.64%
DisplayHDR True Black 500	194	282(+88)	45.36%
DisplayHDR True Black 600	65	123(+58)	89.23%
DisplayHDR True Black 1000	0	33(+33)	N/A
SUM	1319	1839(+520)	39.42%

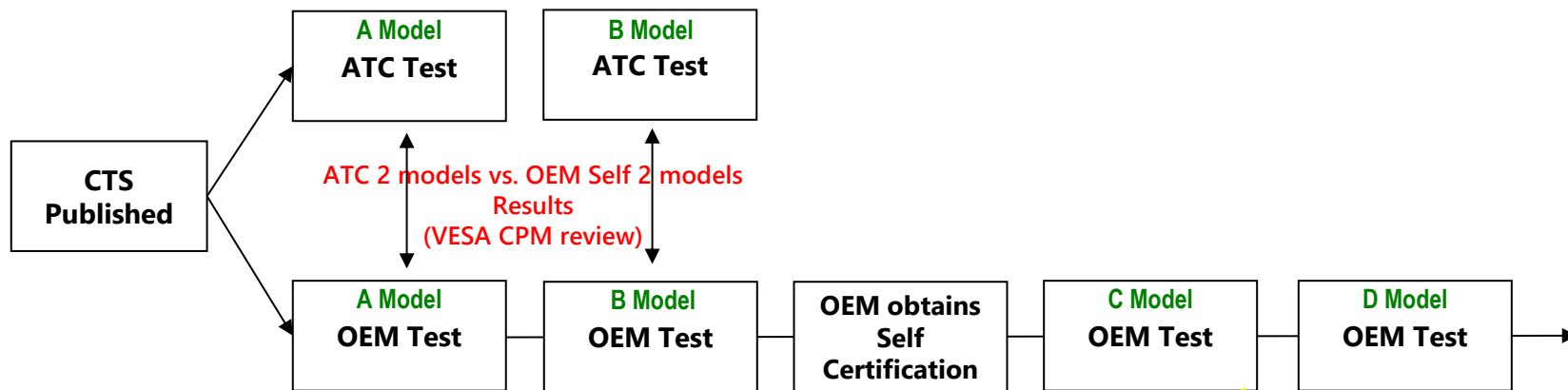
Excluding Family models



<https://displayhdr.org/>

Self Certification

- If the OEM self-test results for both models match the ATC results, the OEM is eligible for self-certification from the VESA Compliance Project Manager (CPM)



OEM can apply for official logo
via VESA Compliance Manager

Agenda

- HDR Technology
- DisplayHDR CTS1.2 Overview
- DisplayHDR CTS1.2 Test

DisplayHDR CTS1.2 Spec

Red : Changed to

Test/Specification			DisplayHDR					DisplayHDR TrueBlack			
			400	500	600	1000	1400	400	500	600	1000
Minimum White Luminance	8% Center Patch	Min (cd/m ²)	400	500	600	1000	1400	400	500	600	1000
		Min –Max 편차	10%	10%	10%	10%	10%	10%	10%	10%	10%
	Full screen Flash Test	Min (cd/m ²)	400	500	600	1000	1400	250	300	350	400 →500
	Full screen Long duration	Min (cd/m ²)	320	320	350	600	900	250	300	350	600 →500
Dual Corner Box	Screen Center	Max (cd/m ²)	0.4	0.1	0.1	0.05	0.02	0.0005	0.0005	0.0005	0.0005
	Both White Corners	Min (cd/m ²)	300	375	450	750	1050	300	375	450	750
Active dimming - <u>CheckerBoard</u>	Log ₁₀ (8%patch white/ 5nit Black)/Log ₁₀ 2		11	11.6	12	13	13.5	N/A	N/A	N/A	N/A
	Log ₁₀ (8%patch white/ 50nit Black)/Log ₁₀ 2		12	12.6	13	14	14.5	N/A	N/A	N/A	N/A
	Checkerboard black level at maximum EDID white luminance (or when white luminance is less than 500 cd/m ²)		N/A	N/A	N/A	N/A	N/A	0.0005	0.0005	0.0005	0.0005
Color Gamut	ITU-R BT.709 - 8% and Full screen		95 →99%	99%	99%	99%	99%	99%	99%	99%	99%
	DCI-P3 CIE D65 - 8% and Full screen		N/A → 90%	90 →95%	90 →95%	90 →95%	90 →95%	90 →95%	90 →95%	90 →95%	90 →95%
	RGB Combined Color Luminance - 8%		400	500	600	1000	1400	400	500	600	1000
	RGB Combined Color Luminance – Full screen		320	320	350	600	900	250	300	350	600 →500
Minimum Bit-depth	10-bit Video Signal, per Channel		✓	✓	✓	✓	✓	✓	✓	✓	✓
	Temporal or Spatial Dithering		8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC
	Minimum 8-bit Digital-to-analog		✓	✓	✓	✓	✓	✓	✓	✓	✓
	Backlight Control 8-bit Accuracy		✓	✓	✓	✓	✓	N/A	N/A	N/A	N/A
Rise-time	60Hz에서 Luminance 10%→90% 시간		8 Frame	8 Frame	8 Frame	8 Frame	8 Frame	2 Frame	2 Frame	2 Frame	2 Frame

DisplayHDR CTS1.2 Spec

Red : Changed to CTS1.2

Test/Specification			DisplayHDR					DisplayHDR TrueBlack			
			400	500	600	1000	1400	400	500	600	1000
White Point Accuracy (Addition Noise Pattern)	Delta-ITP Error	≤ 5cd/m2	20	20	20	20	20	20	20	20	20
		15 cd/m2	10→15	10→15	10→15	10→15	10→15	10→15	10→15	10→15	10→15
		50,100, 200 cd/m2 50%, 100% tier level	10	10	10	10	10	10	10	10	10
Static Contrast Ratio	1D Test Pattern		1300:1	7000:1	8000:1	N/A	N/A	N/A	N/A	N/A	N/A
	2D Test Pattern		N/A	N/A	N/A	30K:1	50K:1	N/A	N/A	N/A	N/A
Black HDR vs SDR	HDR Contrast Ratio > SDR Contrast Ratio × 0.9 (Pass if SDR C/R > Static C/R)		>90%	>90%	>90%	>90%	>90%	>90%	>90%	>90%	>90%
Black Level Crush	Required number of distinct shadow levels		5	5	5	5	5	5	5	5	5
Subtitle Flicker	10 cd/m ² Box Brightness vs. Subtitle Presence		13%	13%	13%	10%	10%	10%	10%	10%	10%
X-Rite Color 96 Delta-TP	50 cd/m2		8	8	8	6	6	8	8	8	6
	100 cd/m2		8	8	8	6	6	8	8	8	6
	50% of DisplayHDR Logo		8	8	8	6	6	8	8	8	6

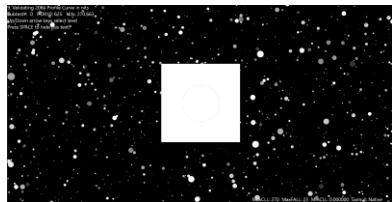
DisplayHDR CTS1.2 Overview

- Luminance Performance Test

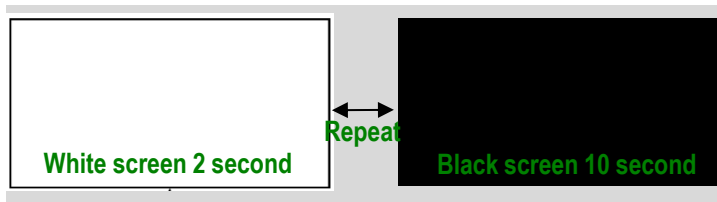
Red : Added patterns in CTS 1.2



8% Patch



White Delta accuracy

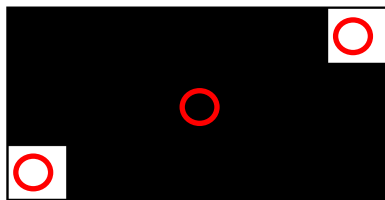


Full-screen Flash

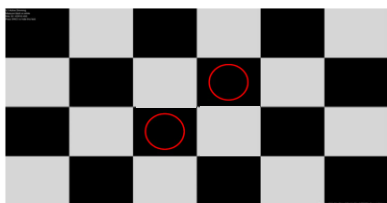


Full-screen Long-duration

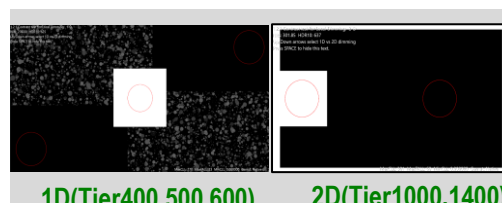
- Black Level/Contrast Ratio Test



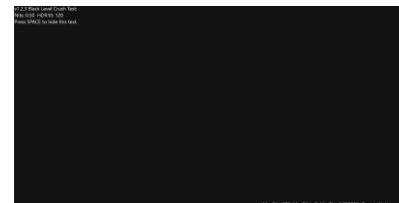
Dual Corner Box



Checker board



Static Contrast Ratio

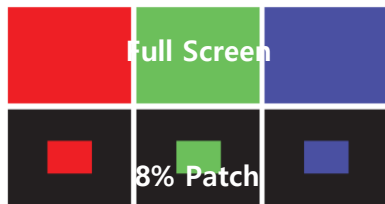


Black Level Crush

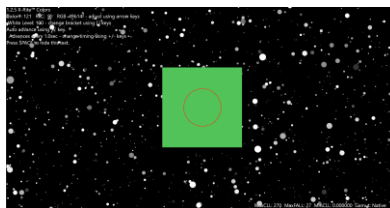
DisplayHDR CTS1.2 Overview

- Color Test

Red : Added patterns in CTS 1.2

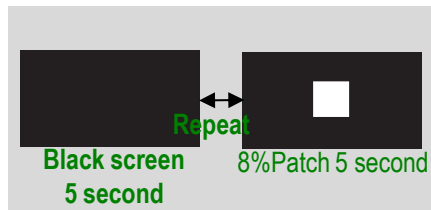


Color Gamut
sRGB, DCI-P3

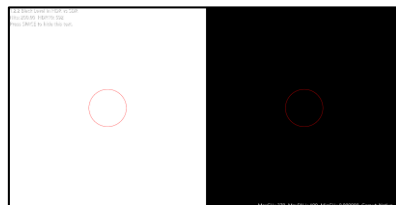


Xrite 96color

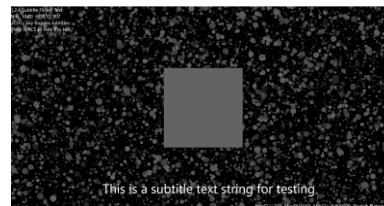
- HDR Performance Test



Rise-time Sequence



HDR vs. SDR Black Level Test



Subtitle Flicker

Agenda

- HDR Technology
- DisplayHDR CTS1.2 Overview
- DisplayHDR CTS1.2 Test

- Colormeter
 - Black Level Luminance Range
 - DisplayHDR → 0.05 to 4 cd/m² ± 4%
 - DisplayHDR True Black → 0.0005 to 4 cd/m² ± 4%
 - White Level Luminance Range → 400 to 1,400+ cd/m² ± 2%
 - Color accuracy – 0.003 x, y

Certification Level	Manufacturer (Family)	Model Numbers
DisplayHDR	Konica-Minolta™	CA-310 ^a , CA-410 family of products, CA-P427, CA-VP427, and CS-2000
	Photo Research SpectraDuo®	PR-670 and PR-680
	Gamma Scientific	GS-1220
	Topcon TechnoHouse	SR-UL1R
DisplayHDR True Black ^b	Konica-Minolta	CS-2000A, CS-3000, and CS-3000HDR
	Photo Research SpectraDuo®	PR-680 and PR-680L
	Photo Research SpectraScan®	PR-740, PR-745, PR-788, and PR-1050
	Topcon TechnoHouse	SR-UL2



CA-VP427



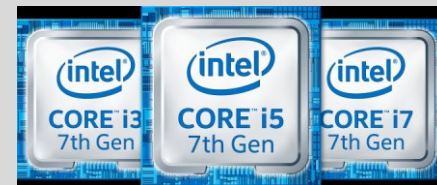
CA-2000A

Test Environment

- CTS Test Tool for H/W,S/W requirement
 - Hardware(Minimum requirements)
 - Intel®
 - 7th Generation Core™ processors or later, with 620 graphics or higher
 - AMD®
 - Radeon Rx 5xx series and Radeon Rx Vega or later
 - NVIDIA®
 - GeForce GTX 10-Series graphics cards or later
 - Software
 - Windows 11
 - Changed in the CTS1.2



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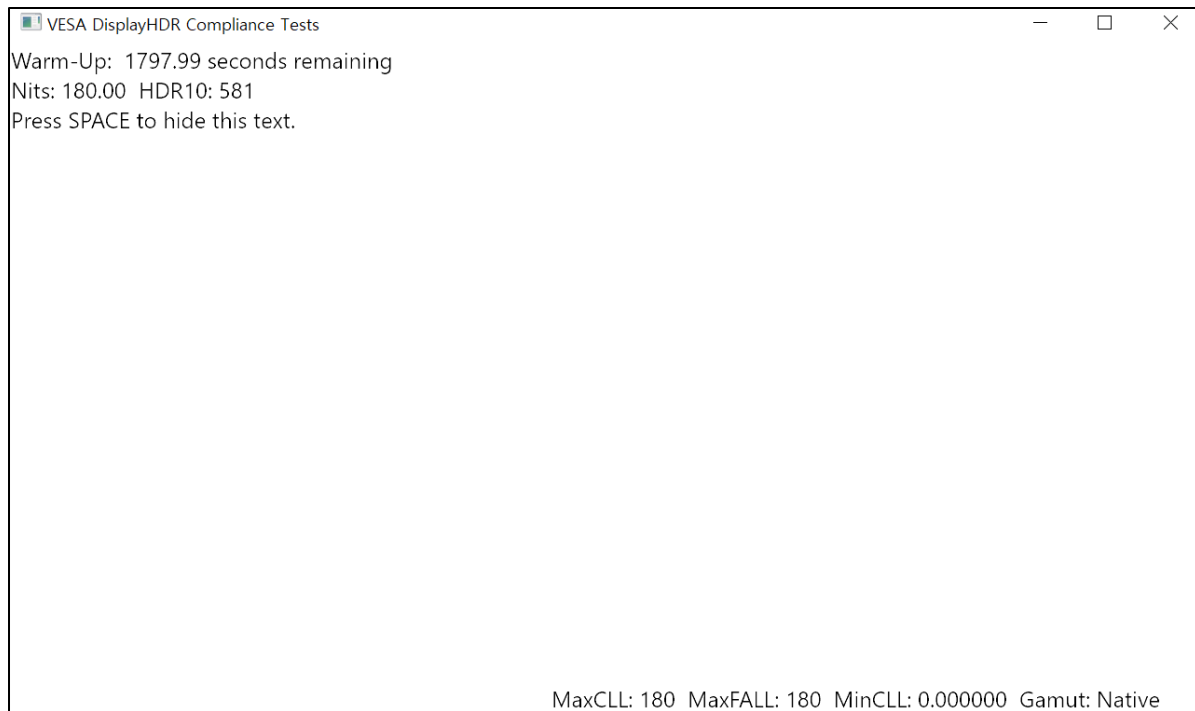
ADD TO CART

Free Shipping
Estimated Ship Date: 1 week
Limit 2 per customer

NVIDIA® GeForce GTX 10-Series

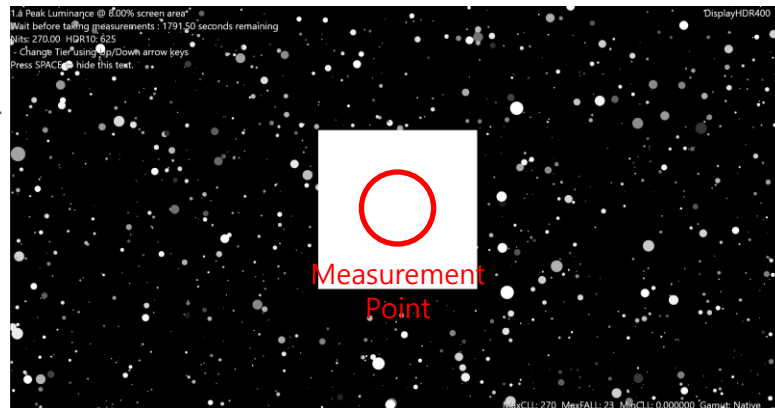
Measurement setting

- Warm-Up 30minutes
 - Luminance : 180nit (PQ-Code value : 581)



8% Center Patch Noise Pattern

- Test Pattern Information
 - White : 8% APL¹⁾ center square at MaxLuminance pixel value.
 - Background: 2% APL, based on the DisplayHDR performance tier
 - Maximum luminance of noise patterns: 100 cd/m²
- How to Measure
 - Black screen for a 1-minute cool-down reset(C key)
 - Luminance is measured at the screen's center once per minute for 30 minutes
 - First measurement shall be obtained within 5 seconds



8% Center Patch

Specifications

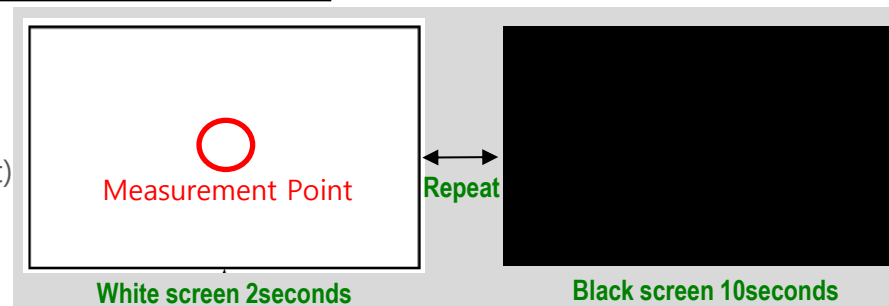
Test/Specification			DisplayHDR					DisplayHDR TrueBlack			
			400	500	600	1000	1400	400	500	600	1000
Minimum White Luminance	8% Center Patch	Min (cd/m2)	400	500	600	1000	1400	400	500	600	1000
		Min-Max Deviation	10%	10%	10%	10%	10%	10%	10%	10%	10%

1) APL : Average Picture Level

Full-screen Flash Test

- Test Pattern Information
 - White : EDID Max Luminance value
 - White Screen 2seconds → Black Screen 10seconds (Repeat)

- How to Measure
 - Black screen for a 1-minute cool-down reset (C key)
 - Luminance is measured at the screen's center once per iteration, for five iterations



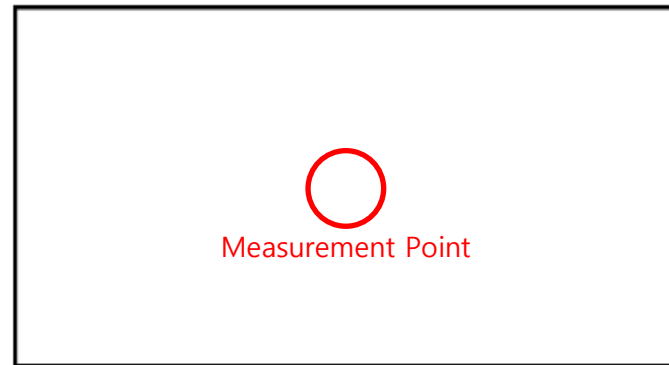
Full-screen Flash Test

- Specifications

Test/Specification			DisplayHDR					DisplayHDR TrueBlack			
			400	500	600	1000	1400	400	500	600	1000
Minimum White Luminance	Full screen Flash	Min (cd/m2)	400	500	600	1000	1400	250	300	350	500

Full-screen Long-duration Test

- Test Pattern Information
 - White : EDID Max Luminance value
- How to Measure
 - Black screen for a 1-minute cool-down reset(C key)
 - Luminance is measured at the screen's center once per minute for 30 minutes
 - First measurement shall be obtained within 5 seconds
- Specifications

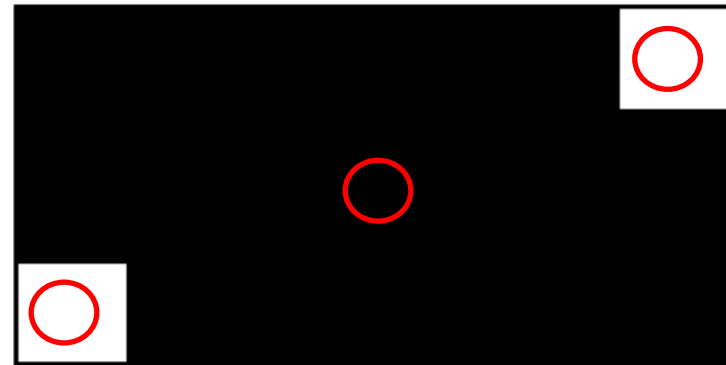


Full screen Long duration

Test/Specification			DisplayHDR					DisplayHDR TrueBlack			
			400	500	600	1000	1400	400	500	600	1000
Minimum White Luminance	Full screen Long duration	Min (cd/m2)	320	320	350	600	900	250	300	350	500

Dual Corner Box

- Test Pattern Information
 - White : 5% corner squares use the MaxLuminance value
- How to Measure
 - Black screen for a 1-minute cool-down reset(C key)
 - Luminance is measured at the screen's center and both white corner squares
 - Measurements shall be obtained within 10 seconds
- Specifications



Dual Corner Box  Measurement Point

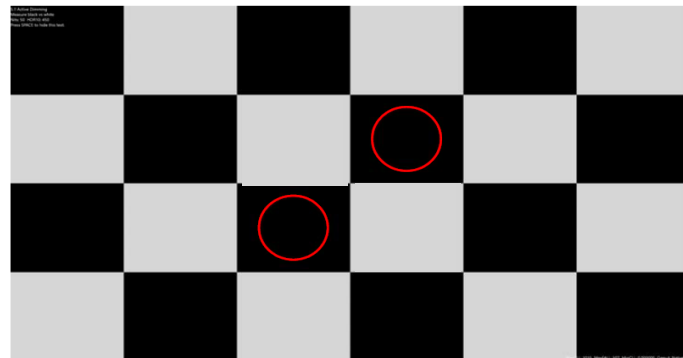
Test/Specification			DisplayHDR					DisplayHDR TrueBlack			
			400	500	600	1000	1400	400	500	600	1000
Dual Corner Box	Screen Center	Max (cd/m2)	0.4	0.1	0.1	0.05	0.02	0.0005	0.0005	0.0005	0.0005
	Both White Corners	Min (cd/m2)	300	375	450	750	1050	300	375	450	750

Checkerboard(1/2)

• Test Pattern Information

- DisplayHDR
 - White : 5cd/m² – EOTF code value : 253
 - White : 50cd/m² – EOTF code value : 450
- DisplayHDR True Black
 - EDID Max Luminance white Or White Luminance < 500 cd/m²
If found to exceed 500 cd/m², the applied digital code value shall be reduced until the luminance is just above 500 cd/m²

Continue to Adjust the input code values until the average of the white center squares greater than or equal to 5 cd/m², 50 cd/m²

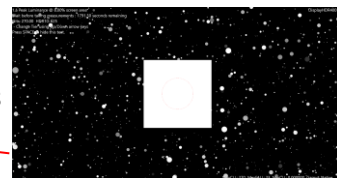


Checker board

 Measurement Point

• How to Measure

- Black screen for a 1-minute cool-down reset(C key)
- Luminance is measured at the screen's average of two center black squares
 - Each of the four measurements on each Checkerboard luminance test shall be measured within 10 seconds



8% Center patch

• Specifications

White 8% patch 30 times measured average value

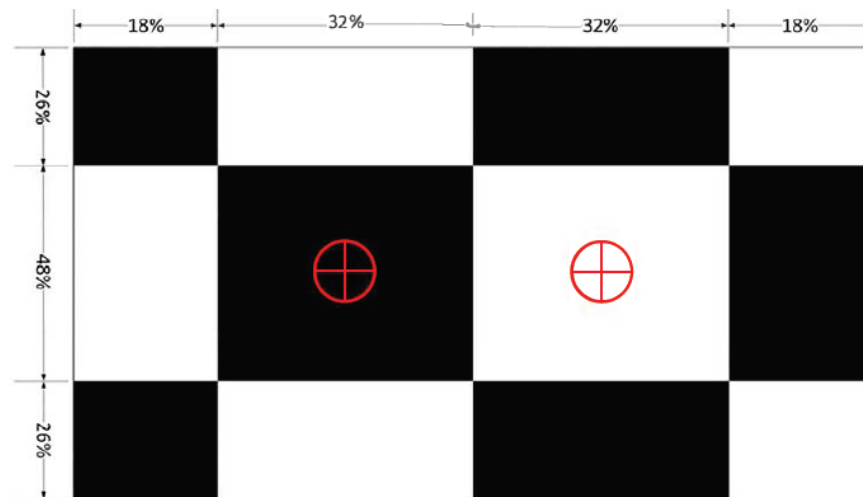
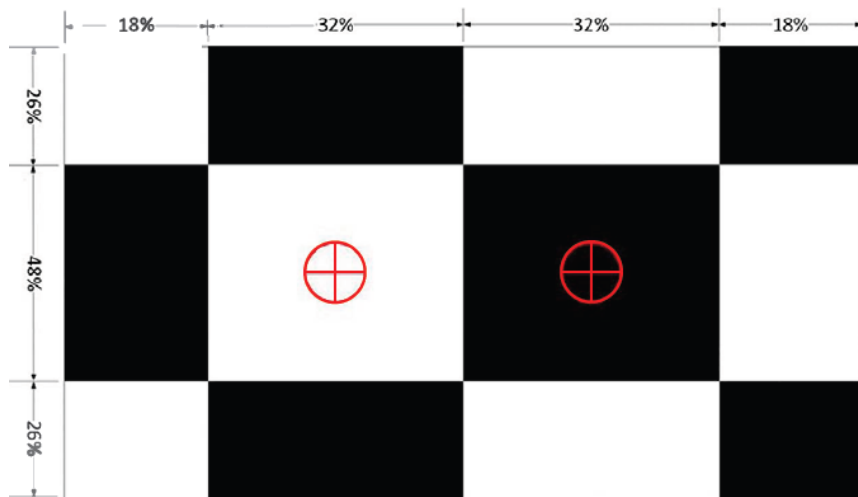
Test/Specification		DisplayHDR					DisplayHDR TrueBlack			
		400	500	600	1000	1400	400	500	600	1000
Active dimming - Checker Board	$\text{Log}_{10}(\text{8\% patch white} / 5\text{nit Black}) / \text{Log}_{10}2$	11	11.6	12	13	13.5	N/A	N/A	N/A	N/A
	$\text{Log}_{10}(\text{8\% patch white} / 50\text{nit Black}) / \text{Log}_{10}2$	12	12.6	13	14	14.5	N/A	N/A	N/A	N/A
	Checkerboard black level at maximum EDID white luminance (or when white luminance is less than 500 cd/m ²)	N/A	N/A	N/A	N/A	N/A	0.0005	0.0005	0.0005	0.0005

Checkerboard(2/2)

- In case of Panel Size < 20Inch, Possible to test the 4 × 3 checkerboard

- For the 4×3 checkerboard test, this specification requires measuring the black and white luminance of the check near the center for both patterns.

For more details, Please see
DisplayHDR1.2 Spec.



- Test Result Form

5.2.2	5.x	Checkerboard tests			Top White	Bottom White	Top Black	Bottom Black	Screen Size	Test Type
	N/A	N/A - No 50cd/m2 or 5 cd/m2 test for TrueBlack							10	4x3 Pattern
		N/A - No 50cd/m2 or 5 cd/m2 Test for TrueBlack	N/A	N/A	N/A					6x4 Pattern
	5.2	Full Luminance Checkerboard or >=500 for TrueBlack			0	0	0	0		4x3 Pattern

Measurement Point

Measurement Point

Color Gamut(1/2)

• Test Pattern Information

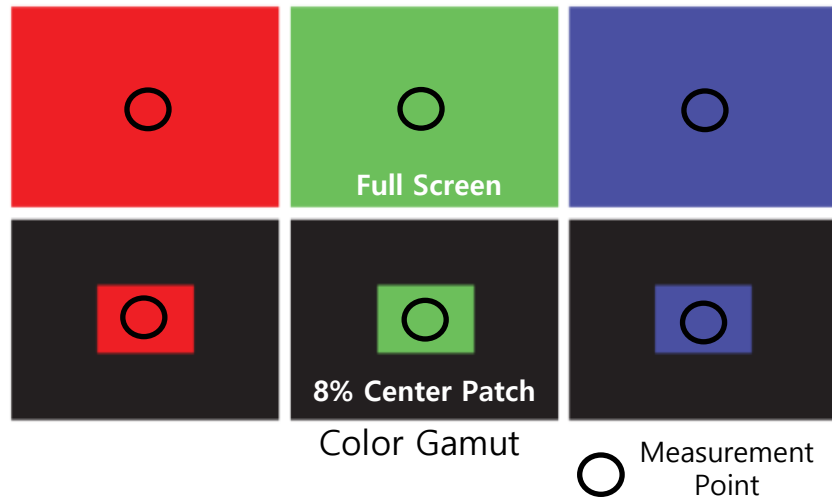
- MaxLuminance and RGB primary color values in the DisplayID (or legacy EDID)
- Six separate tests(Red, Green, and Blue)
 - Full-screen
 - 8% center square

• How to Measure

- CIE 1931 x, y, Y values are measured at the screen's center

• Specifications

- Color gamut shall be calculated for actual coverage of the target gamut
- The Red, Green, and Blue luminance sum for each 8% center square and full-screen color test shall meet or exceed the white-level luminance specifications



Test/Specification		DisplayHDR					DisplayHDR TrueBlack			
		400	500	600	1000	1400	400	500	600	1000
Color Gamut	ITU-R BT.709 - 8% and Full screen	99%	99%	99%	99%	99%	99%	99%	99%	99%
	DCI-P3 CIE D65 - 8% and Full screen	90%	95%	95%	95%	95%	95%	95%	95%	95%
	RGB Combined Color Luminance - 8%	400	500	600	1000	1400	400	500	600	1000
	RGB Combined Color Luminance – Full screen	320	320	350	600	900	250	300	350	500

Color Gamut(2/2)

- Test Result Form(e.g. DisplayHDR400)

6.1	6a & 6b	Color Gamut & Luminance Test		①Enter measurement data					
		Patch Test Size 8% and Full Screen		Luminance			Luminance		
		Red		x			x		
		Green		y			y		
		Blue		8% Patch Size Color Test			Full Screen Patch Size Color Test		
		Calculated EDID Color, u'v'		Luminance	x	y	Luminance	x	y
		Red		100	0.7	0.3	100	0.7	0.3
		Green		350	0.25	0.65	350	0.25	0.65
		Blue		32	0.15	0.05	32	0.15	0.05
		8% Patch Color Luminance Sum Requirement		Luminance	u	v	Luminance	u	v
		sRGB Coverage u'v' for the 8% Patch		482	0.53846	0.51923	482	0.53846	0.51923
		DCI-P3 Coverage u'v' for the 8% Patch			0.09709	0.56796		0.09709	0.56796
		Full Screen Color Luminance Sum Requirement			0.18182	0.13636		0.18182	0.13636
		sRGB Coverage u'v' for Full Screen		400	Pass				
		DCI-P3 Coverage u'v' for Full Screen		99%	Pass	100.00%			
				90%	Pass	97.40%			
				320	Pass				
				99%	Pass	100.00%			
				90%	Pass	97.32%			

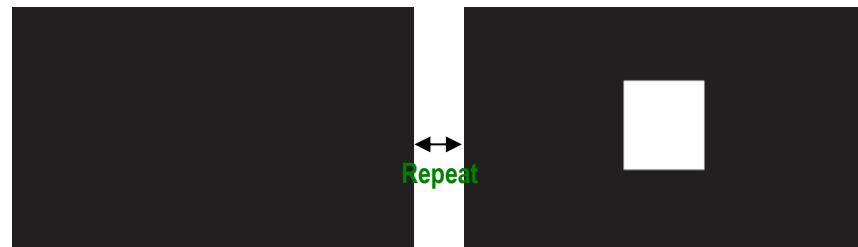


Press this button to calculate the color gamut

- ②Click the Press Button included in the template to check the result.

Rise-time

- Test Pattern Information
 - White : 8% APL center square at MaxLuminance pixel value
- How to Measure
 - Rise time is measured from the 10 to 90% luminance levels
- Specifications

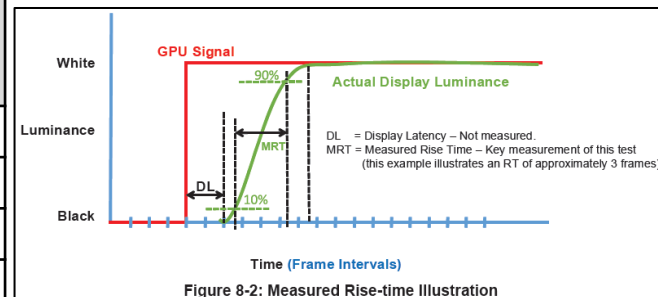


Black Screen 5seconds

8%Patch 5seconds

Bit Depth

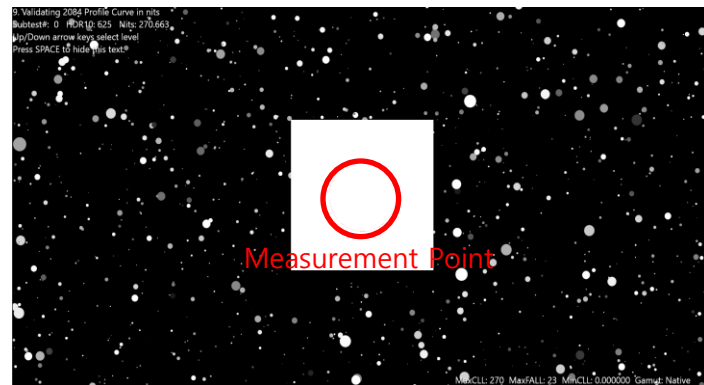
Panel Type	Display Refresh Rate	Maximum Number of Frames for Rise from Black to Maximum Luminance		Time (ms)	
LCD	24	8	Recommended	333	Recommended
	60	8	Mandatory	133	Mandatory
	144	8	Recommended	56	Recommended
	200	8	Recommended	40	Recommended
OLED TrueBlack	60	2	Mandatory	33	Mandatory



Section9

- **White** : Center square comprising 8% of the screen's area
 - Possible to change the 8% of the screen's luminance area
 - 1.0509, 5.172, 14.958, 50.825, 100.23, 199.15 cd/m²
 - 50% of DisplayHDR Tier
 - 100% of DisplayHDR Tier - Least three 10-bit code values below the tier
- **Background** : Max Luminance of Noise Patterns is 100 cd/m²
 - Limiting 2% APL of the DisplayHDR performance tier

- CIE 1931 x, y, Y values are measured at the screen's center
 - Measurement shall be initiated at the screen's center within 5 seconds
 - The tests shall be measured in sequentially increasing luminance levels

[illegible]

White Accuracy Pattern

Luminance and White Point Accuracy

- Test Result Form(e.g. DisplayHDR400)

① Enter measurement data
(Automatically calculate Delta-ITP)

		Maximum of any sample (8 frames i.e. 133ms at 60Hz)	133	Pass	16	Measured		
9		Delta-ITP			Delta-ITP	x	y	Y
9.3	9.10	Delta-ITP at 1.0509 cd/m ²	20	Pass	1.83	0.31271	0.32902	1
	9.11	Delta-ITP at 5.172 cd/m ²	20	Pass	1.73	0.31271	0.32902	5
	9.12	Delta-ITP at 14.958 cd/m ²	15	Pass	0.17	0.31271	0.32902	15
	9.14	Delta-ITP at 50.825 cd/m ²	10	Pass	1.12	0.31271	0.32902	50
	9.16	Delta-ITP at 100.23 cd/m ²	10	Pass	0.17	0.31271	0.32902	100
	9.17	Delta-ITP at 199.15 cd/m ²	10	Pass	0.32	0.31271	0.32902	200
	9.18/19/24/28	Delta-ITP 50% of Tier: 199.15 cd/m ²	10					
	9.21/23/26/32/37	Delta-ITP near Tier: 387.13 cd/m ²	10	Pass	0.03	0.31271	0.32902	387

② Check the results

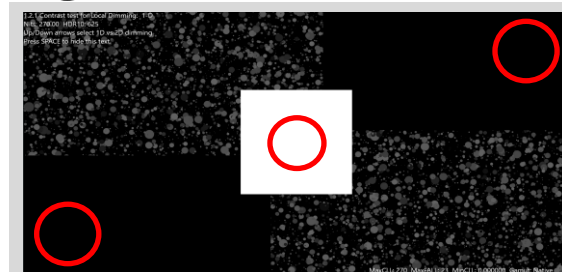
1D and 2D Local Dimming

• Test Pattern Information

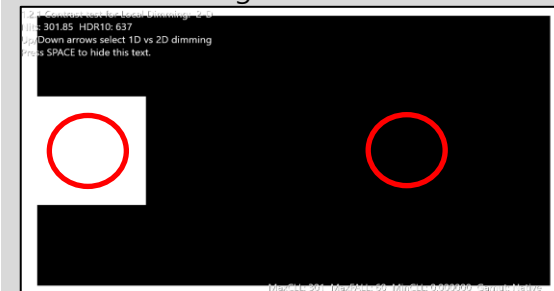
- 1D : DisplayHDR 400, 500, 600 tier(Including True black tier)
 - White : 8% APL center square at MaxLuminance pixel value
 - Background : Upper left, Lower right corners: 30% of Screen size and <10nit Star
- 2D : DisplayHDR 1000, 1400 tier
 - White : 8% APL left square at MaxLuminance pixel value
 - Background : MaxLuminance on all four sides of the image, 3% of width each

• How to Measure

- Luminance is measured at the screen's ○ Points →



1D Local Dimming Pattern



2D Local Dimming Pattern

○ Measurement Point

• Specifications

Test/Specification		DisplayHDR					DisplayHDR TrueBlack			
		400	500	600	1000	1400	400	500	600	1000
Static Contrast Ratio	1D Test Pattern	1300:1	7000:1	8000:1	N/A	N/A	N/A	N/A	N/A	N/A
	2D Test Pattern	N/A	N/A	N/A	30K:1	50K:1	N/A	N/A	N/A	N/A

[illegible]

- White

- APL 8% gray square at 10 cd/m²
- Subtitle : 100 cd/m²

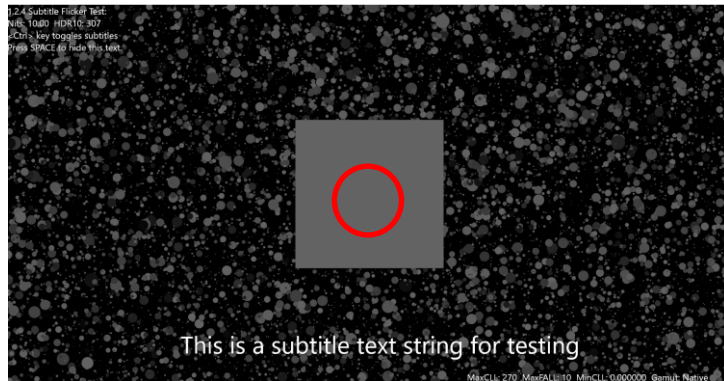
- Background : <10 nit Stars

- How to Measure

- Luminance is measured the gray square's minimum and maximum range as the subtitles ON/OFF
 - The CTRL button can control the subtitles ON/OFF

- Specifications

- Maximum Luminance/ minimum Luminance x100



Subtitle Luminance
Flicker Pattern

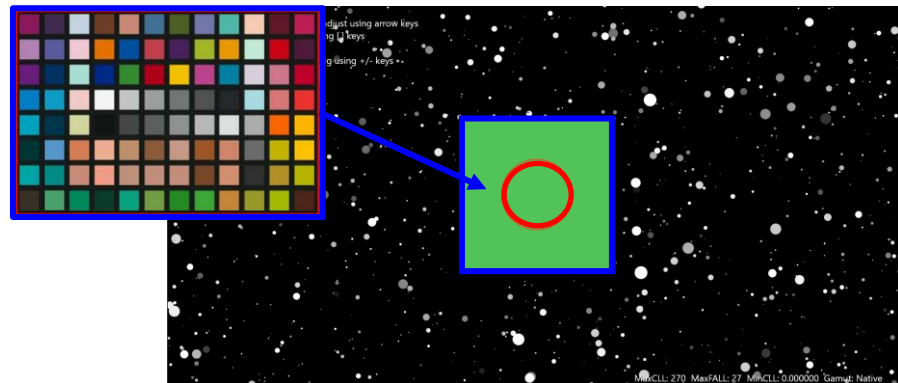
Measurement Point

Test/Specification		DisplayHDR					DisplayHDR TrueBlack			
		400	500	600	1000	1400	400	500	600	1000
Subtitle Flicker	10 cd/m² Box Brightness vs. Subtitle Presence	13%	13%	13%	10%	10%	10%	10%	10%	10%

X-Rite Color Square Test

• Test Pattern Information

- X-Rite Color 96types of 8% center square
 - The colors are tested at three different luminance levels
 - 50 cd/m2
 - 100 cd/m2
 - 50% of DisplayHDR Compliance Logo level
- Background : <100nit Stars



• How to Measure

- 96 Delta-TP color values are measured at the screen's O point. Three tests are conducted at different luminance levels, each using 96 color patches. This test focuses on color accuracy, using Delta-TP instead of Delta-ITP.

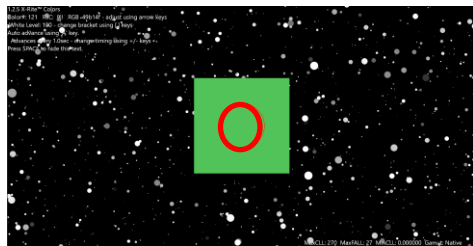
X-Rite Color Square Pattern  Measurement Point

• Specifications

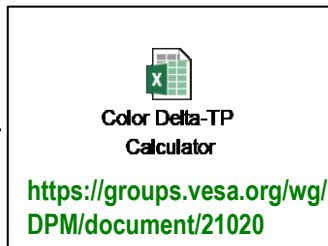
Test/Specification		DisplayHDR					DisplayHDR TrueBlack			
		400	500	600	1000	1400	400	500	600	1000
X-Rite Color 96 Delta-TP	50 cd/m2	8	8	8	6	6	8	8	8	6
	100 cd/m2	8	8	8	6	6	8	8	8	6
	50% of DisplayHDR Logo	8	8	8	6	6	8	8	8	6

XRite Color Square Test

• Test procedure



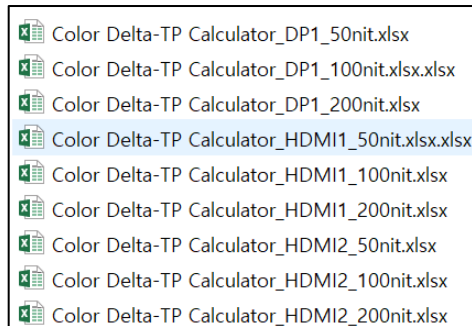
① Set the luminance levels and Measure the 96 color Delta-TP



② Download and Open the Delta-TP Color Patch Calculator

RGB for Lum Target: 50		
R	G	B
0.4315341	0.4322815	0.4301258
0.306711	0.3068675	0.3071609
0.1951589	0.1949144	0.1944453
0.3016082	0.2196962	0.2770536
0.2334271	0.2140811	0.2542263

③ Input the RGB Luminance



⑥ Save the data according to luminance and submit it to the VESA Compliance Manager with Test Result

11.88	11.39	4.0919	20.62	3.09	4.7
9.6269	11.872	3.6052	20.78	1.54	4.9
12.171	16.248	3.32	21.40	1.66	6.7
2.4935	2.3018	1.5514	18.71	5.27	1.1
			Delta-ITP	Delta-TP	Lum Error
			Average	15.77	2.92
			Maximum	24.18	9.48

⑤ Check the Delta TP

Measured Values			Delta-ITP	Delta-TP	Luminance
X	Y	Z	Error		
86.172	91.763	98.4	0.99	0.96	-0.3
19.565	20.513	22.632	3.93	0.27	1.3
3.4797	3.6113	4.0109	10.76	1.57	0.9
11.56	7.5736	12.083	20.84	7.52	3.1
6.1162	5.2144	9.9653	15.10	4.24	1.7
57.238	61.038	78.14	6.33	2.47	5.3
8.5755	7.6934	5.019	18.08	0.25	2.9
29.896	27.448	19.722	15.40	1.33	7.3
14.263	14.993	28.79	14.26	1.97	4.0
7.9662	10.23	5.1425	17.19	0.85	3.5
20.756	19.458	38.389	11.44	2.88	3.8
25.899	35.159	38.02	12.90	1.00	7.5
58.248	58.207	46.465	10.05	1.31	8.9
6.7257	5.0673	4.7988	17.95	0.95	2.1
17.223	10.556	9.9451	22.50	6.84	4.6
31.336	26.162	43.964	13.37	3.50	5.9
14.271	12.067	31.279	16.77	3.92	3.9
64.24	61.355	67.237	6.05	1.27	5.5
26.753	21.709	4.5928	23.49	3.76	9.4
10.5	8.6996	31.231	20.04	2.94	3.7
19.87	13.603	9.751	20.62	5.20	5.3
6.3774	4.8422	11.754	18.50	5.37	2.0
24.971	33.479	8.6296	19.62	2.25	11.3
31.476	29.92	5.3272	22.55	1.96	12.1
58.316	69.296	66.575	6.80	1.69	6.7
18.195	10.992	3.9527	23.76	6.54	5.2
5.8153	4.4966	6.8859	17.49	5.26	1.8
10.371	6.4744	20.876	21.82	6.79	3.0
4.9269	4.7471	13.109	19.11	1.83	2.1
49.336	59.235	66	8.94	2.65	7.7
6.016	4.5097	20.759	20.27	2.34	2.2
11.217	17.922	7.6543	17.79	1.68	5.9
14.001	8.3427	3.883	23.23	7.61	3.9
39.034	42.076	6.3153	23.03	1.50	16.8
22.064	14.587	23.892	19.63	5.31	5.3
11.222	14.57	30.392	21.05	3.24	6.0
62.971	64.227	79.454	3.73	2.44	2.7
31.12	25.02	26.447	14.68	2.89	6.2
15.869	9.4934	5.2344	23.73	6.61	4.6
14.889	15.939	46.294	20.64	2.47	6.4
21.398	24.427	49.652	17.56	2.60	7.7
62.238	60.972	58.039	7.07	1.46	6.3
53.973	56.739	62.505	1.68	0.66	1.3
33.789	35.623	39.664	2.74	0.52	1.5
10.219	10.681	11.971	7.65	1.41	1.5
4.6133	4.8259	5.5722	9.06	1.17	0.9
50.718	58.036	74.526	9.37	2.42	8.1

④ Measure each of the 96 colors and Input the X, Y, and Z values

VESA Adaptive-Sync Display CTS Overview and Test

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Seung Hyun Yoo (Seunghyun.yoo@lge.com)

LG Electronics, Inc.

31 Oct 2025

Agenda

- Adaptive-Sync Display CTS1.1a Overview
- Adaptive-Sync Display CTS1.1a Test



Adaptive-Sync Display



VESA CERTIFIED

DisplayHDR™

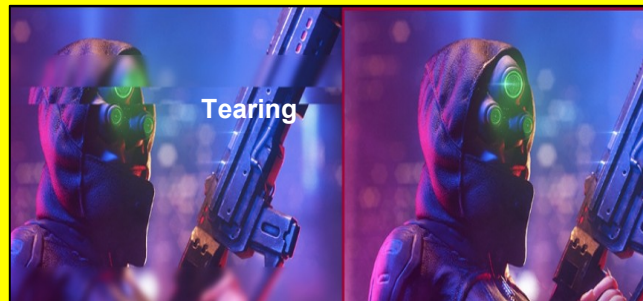
Performance for HDR



VESA CERTIFIED

AdaptiveSync

Performance for variable frequency



VESA CERTIFIED

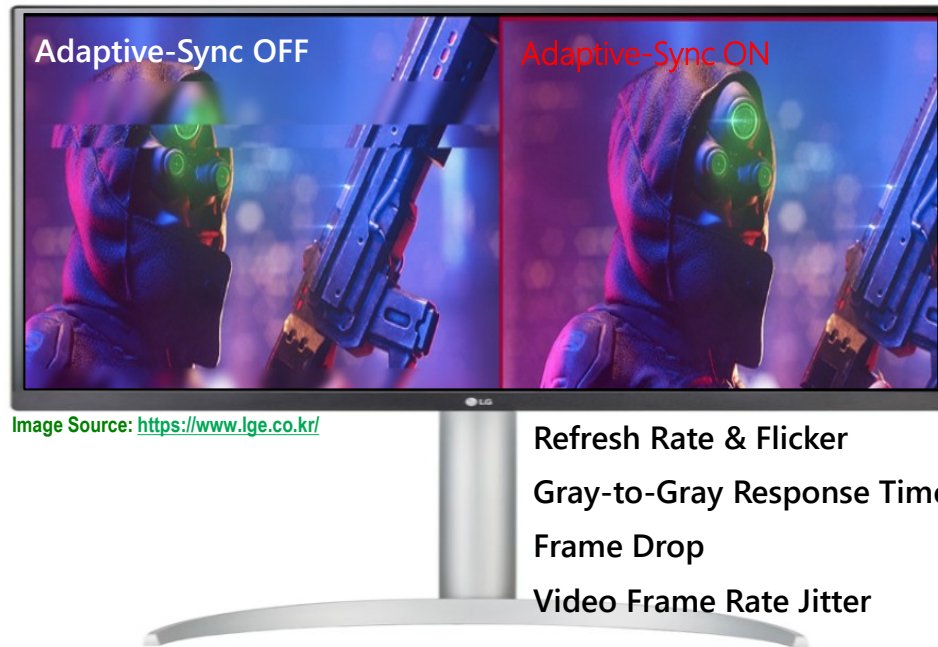
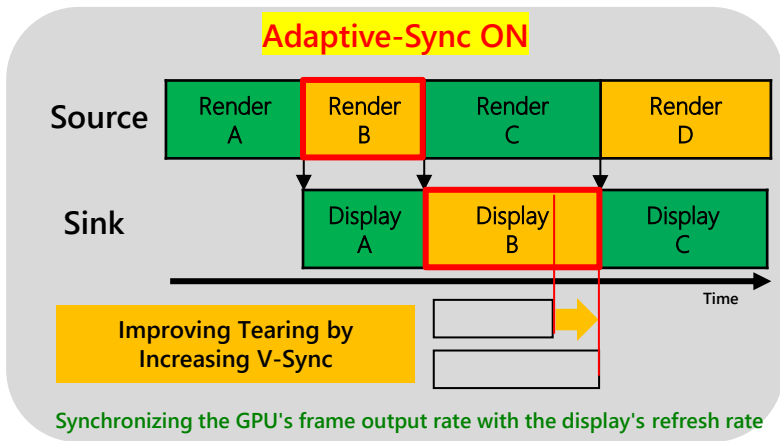
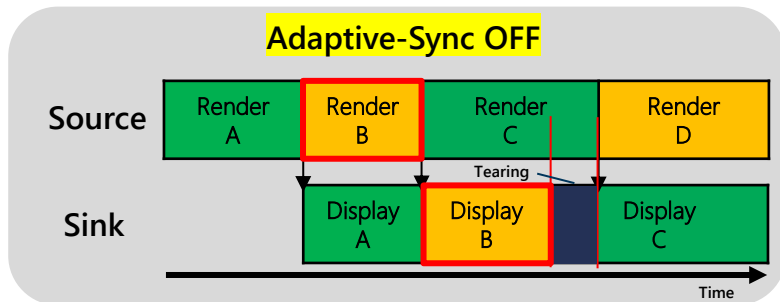
ClearMR

Performance for Motion



Adaptive-Sync Display

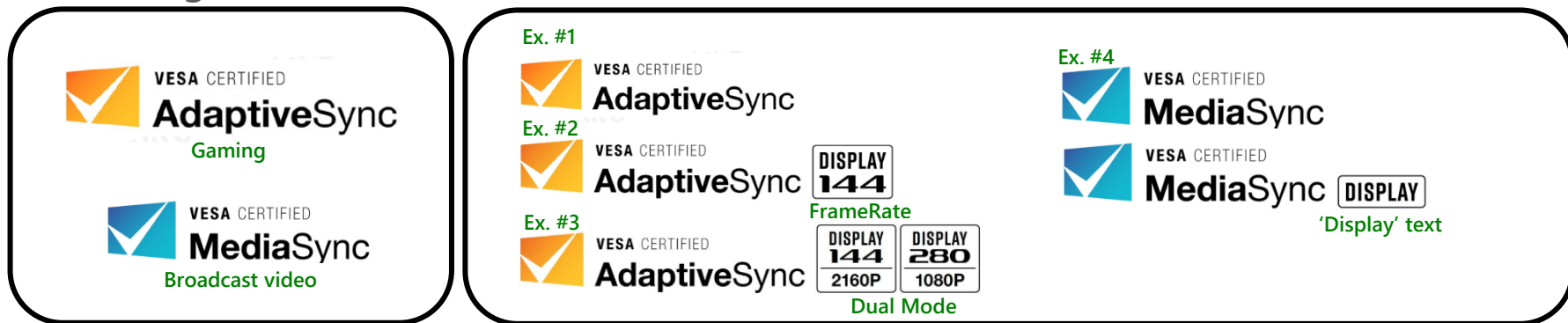
- Industry Standards for Variable Refresh Rate Display Performance
 - Screen Tearing Prevention through V-Sync Control
 An issue caused by a lack of synchronization between the monitor and GPU



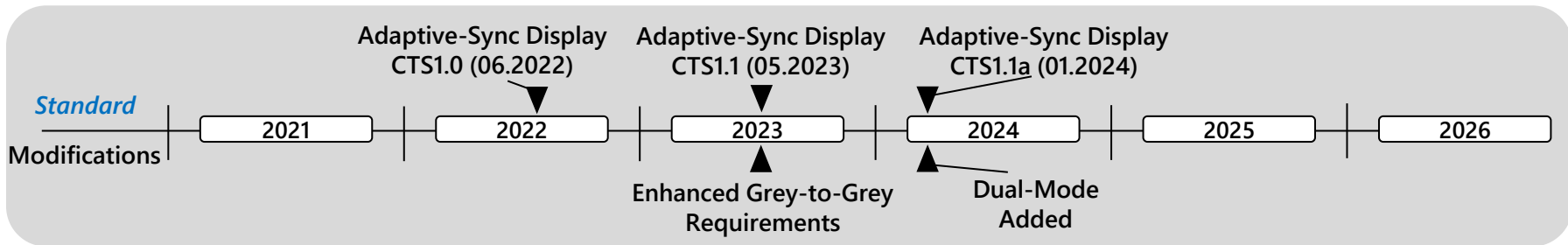


Adaptive-Sync Display

- Tier/Logo



- History

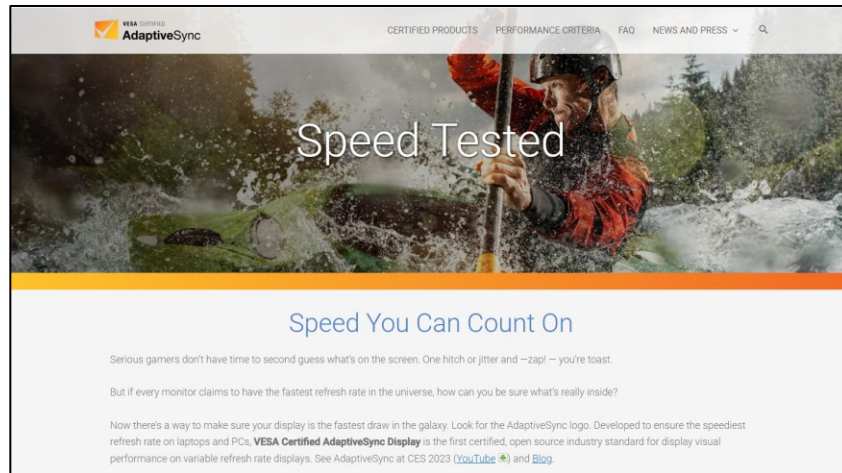


Adaptive-Sync Display

- Adaptive-Sync Display Certification Status

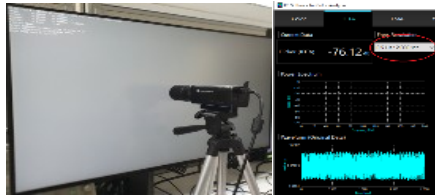
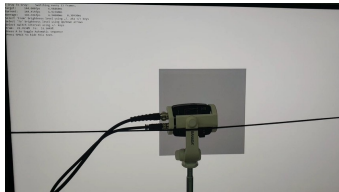
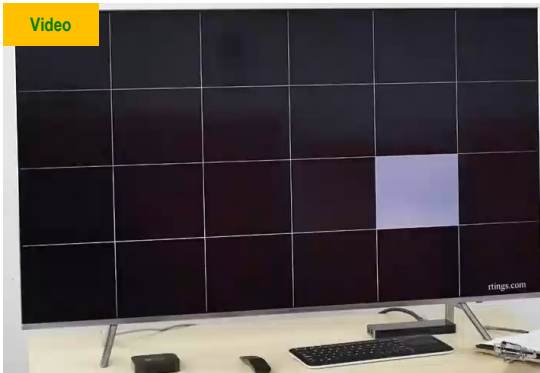
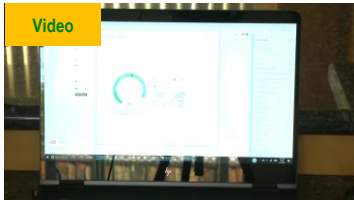
Tier	2024.10	2025.10	Growth rate
Adaptive-Sync Logo	117	210(+93)	79.49%
MediaSync Logo	20	25(+5)	25.00%

Excluding family models



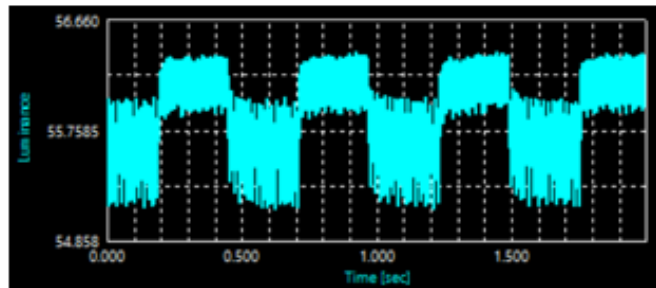
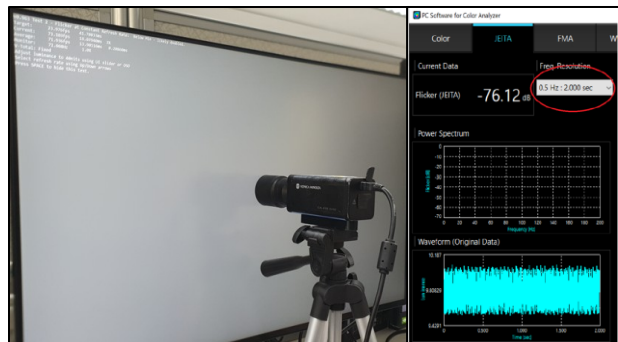
<https://www.adaptivesync.org/>

Adaptive-Sync Display

Test	Phenomenon	Measurement
Flicker		
Grey to Grey (G2G)		
Frame Drop		
Jitter		

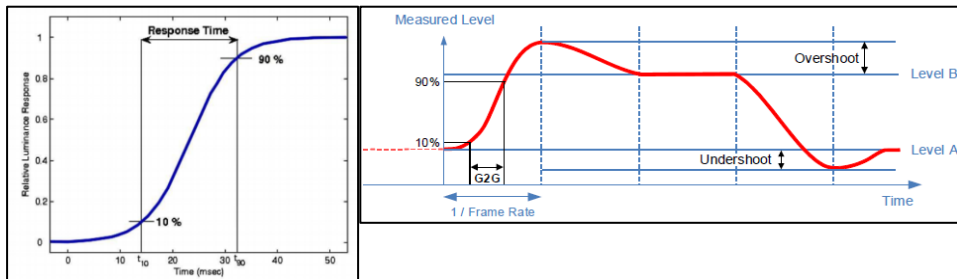
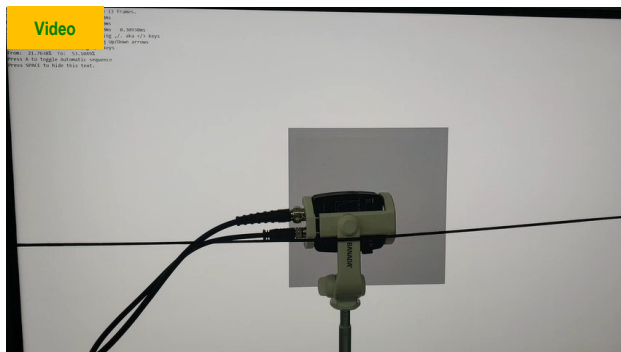
Adaptive-Sync Display

- Flicker Test



Verification of Luminance Flicker under Static and Variable Refresh Rates

- Grey to Grey Test



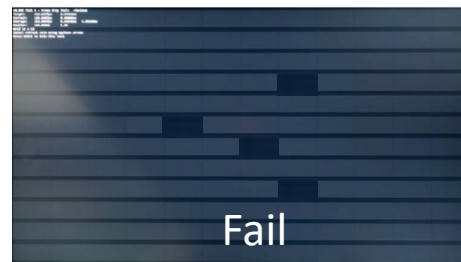
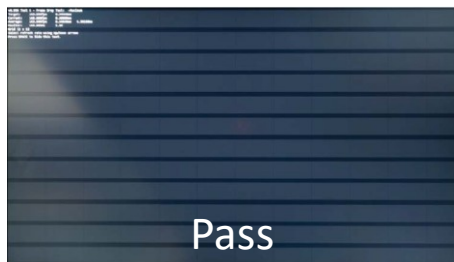
Verification of Response Time and Over/Undershoot in G2G Transitions

Adaptive-Sync Display

- Frame Drop Test



Shutter Speed 1s

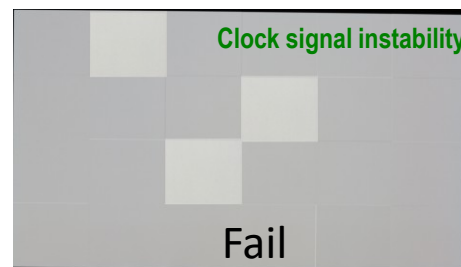
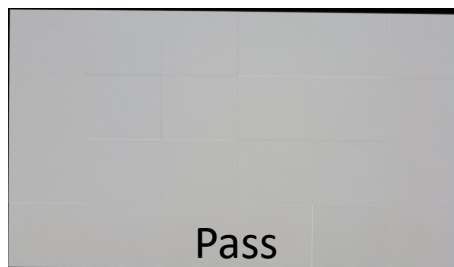


Verification of Dropped Frames under Static and Variable Refresh Rates

- Jitter Test



Shutter Speed 1s



Verification of Block Luminance Variation under Static Frequency

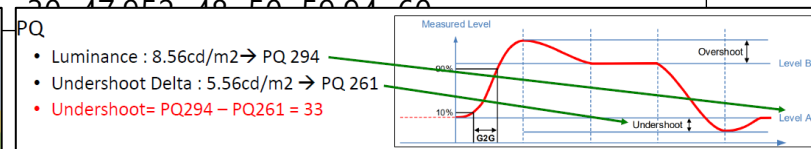
Adaptive-Sync Display Spec

		Tier	
		AdaptiveSync	MediaSync
Maximum Refresh Rate		≥144Hz	≥60Hz
Minimum Refresh Rate		≤60Hz	≤48Hz
Flicker	Low variability refresh	≤-50dB	≤-50dB
	High variability refresh	≤-50dB	N/A
G2G (Max Frame Rate)	Response Time(Avg)	≤5ms	-
	Overshoot(Max)	≤ Delta-PQ Tolerance of each section (#Attachment1)	≤ Delta-PQ Tolerance of each section (#Attachment1)
	Undershoot(Max)		
Frame Drop		0	
Frame-to-frame jitter duration for 23.976- to 60-Hz video		±0.5ms	±0.5ms
The 10 Static frequency video frame rates #Attachment1		23.976, 24, 25, 29.9 30, 47.052, 48, 50, 50.04, 60	

Allowed overshoot/undershoot beyond the target luminance level, measured in Delta-PQ at 10bit

To/End:
(8-bit SDR, Gamma 2.2 code value)

	0	31	63	95	127	159	191	223	255
From/Start: (8-bit SDR, Gamma 2.2 code value)									
0			18	18	18	18	18	18	15
31			15	15	18	18	18	18	10
63				13	15	15	15	18	10
95			20		10	15	15	15	10
127			20	20		10	10	10	10
159			20	20	15		8	10	10
191			30	20	20	13		8	10
223			30	20	20	20	12		5
255			30	30	20	20	10	10	



Substitute Luminance with PQ Values to Compute Differences in Over/Undershoot and Saturation Regions

Agenda

- Adaptive-Sync Display CTS1.1a Overview
- Adaptive-Sync Display CTS1.1a Test

Test Sequence

- <1000nit Display
 1. Warm-up phase(40nit) -1hour
 2. Static Flicker tests
 3. Variable Flicker tests
 4. G2G tests
 5. Frame Drop tests
 6. Jitter tests
 7. If the display supports HDR, then also the HDR tests
- >1000nit Display
 1. Warm-up phase(40nit) -1hour
 2. Static Flicker tests
 3. Variable Flicker tests
 4. Frame Drop tests
 5. Jitter tests
 6. Warm-up phase(185nit)- 20 minutes
 7. High-luminance G2G Tests
 8. If the display supports HDR, then also the HDR tests

Tests must be performed in sequence to prevent DC Offset

Section6 - Flicker Tests

- Purpose : To Verify flicker caused by frame rate changes

Pixel charging/discharging time varies by frame rate, leading to luminance differences

- Test Pattern : SDR Static Full-Screen pattern

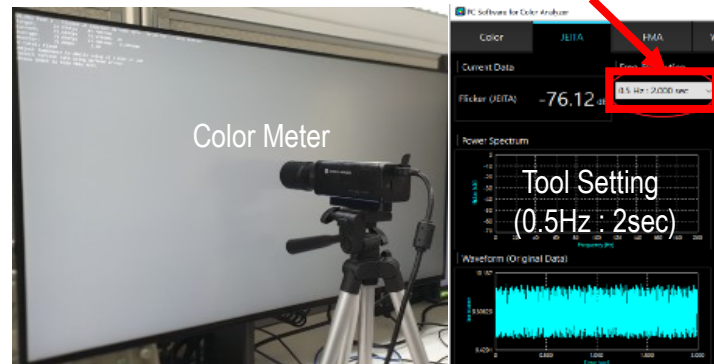
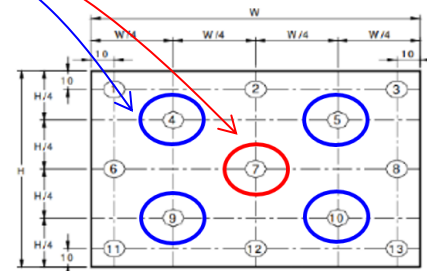
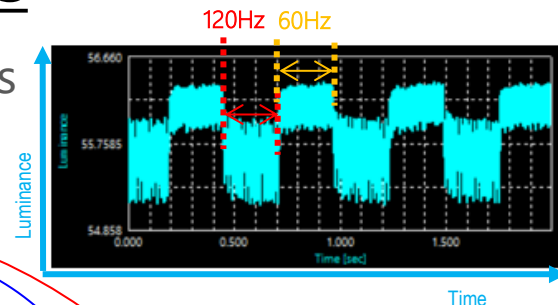
- 40 cd/m² $\pm$ 5% at center
- If center > -60 dB, measure 4 corners additionally.

- Test Refresh Rates

- Static : 23.976, 24, 25, 29.9, 30, 47.952, 48, 50, 59.94, 60Hz
- Variable
- Low variability refresh :
 - Zigzag Sweep (integer multiple per frame)
 - Sine Wave Sweep (frame rate follows sine curve)
- High variability refresh :
 - Square Wave (Min $\leftrightarrow$ Max every 250 ms)
 - Random frame rate.

- Requirement : ≤ -50 dB.

- Perform 10 measurements and record the average
- MediaSync Tier testing does not include high variability refresh



Section7 - G2G tests

- Purpose : For evaluating response time and image quality
- Test Pattern : SDR 8-bit Gamma 2.2 Code Values

- 9 x 9 Matrix Usage(10% patch in 90% grey surround)

Table 7-1: SDR G2G Test Levels – 8-bit Gamma 2.2 Code Values, Displays with MaxLuminance < 1,000 cd/m ²			Table 7-2: SDR High-Luminance G2G Test Levels – 8-bit Gamma 2.2 Code Values, Displays with MaxLuminance ≥ 1,000 cd/m ²		
9 × 9 Matrix Test Patch Values	SDR 10% Test Patch	SDR 90% Gray Surround	9 × 9 Matrix Test Patch Values	SDR 10% Test Patch	SDR 90% White Surround
Test 1 (Black)	0	127	Test 1 (Black)	0	255
Test 2 (Very Dark Gray)	31	127	Test 2 (Very Dark Gray)	31	255
Test 3 (Dark Gray)	63	127	Test 3 (Dark Gray)	63	255
Test 4 (Dark-Mid Gray)	91	127	Test 4 (Dark-Mid Gray)	91	255
Test 5 (Mid Gray)	127	127	Test 5 (Mid Gray)	127	255
Test 6 (Light Mid Gray)	159	127	Test 6 (Light Mid Gray)	159	255
Test 7 (Light Gray)	191	127	Test 7 (Light Gray)	191	255
Test 8 (Bright Gray)	223	127	Test 8 (Bright Gray)	223	255
Test 9 (White)	255	127	Test 9 (White)	255	255

90% surround Grey



Measurement Point

- For each matrix, the G2G response, overshoot, and undershoot are measured 20 times and the average values are reported

Requirement

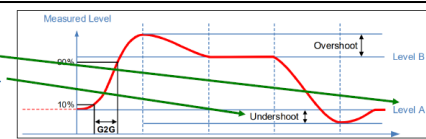
- Response time
 - AdaptiveSync : ≤ 5-ms average over the 64 tests
 - MediaSync : N/A

- Overshoot/Undershoot

Allowed overshoot/undershoot beyond the target luminance level, measured in Delta-PQ at 10bit										
To/End: (8-bit SDR, Gamma 2.2 code value)		0	31	63	95	127	159	191	223	255
From/Start: (8-bit SDR, Gamma 2.2 code value)	0			18	18	18	18	18	18	15
	31			15	15	18	18	18	18	10
	63				13	15	15	15	18	10
	95			20		10	15	15	15	10
	127			20	20		10	10	10	10
	159			20	20	15		8	10	10
	191			30	20	20	13		8	10
	223			30	20	20	20	12		5
255			30	30	20	20	10	10		

PQ

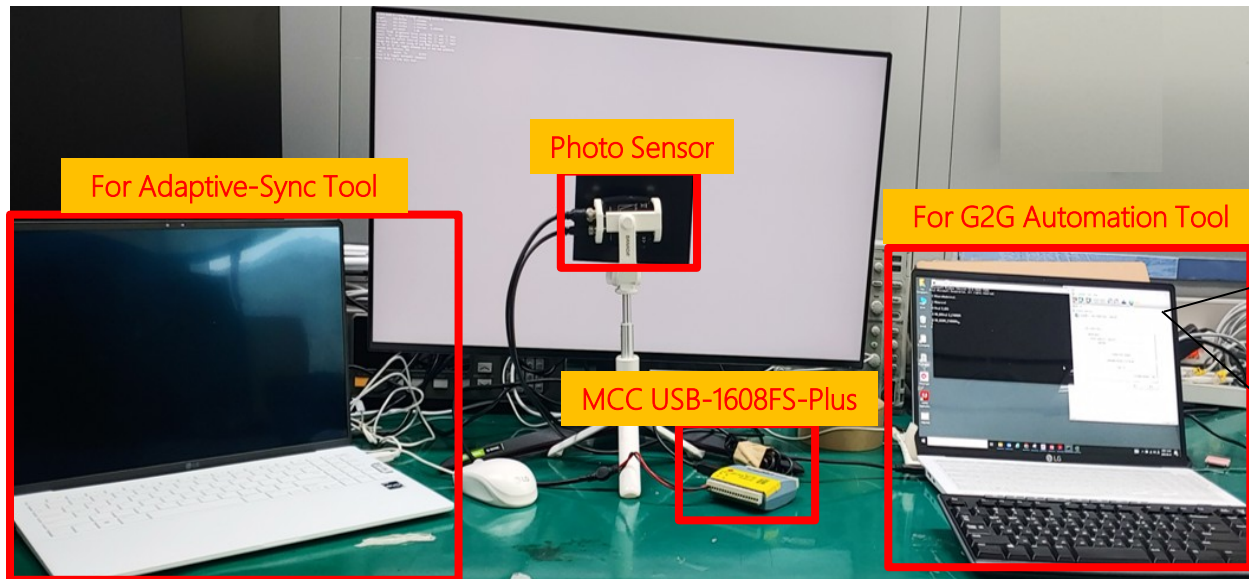
- Luminance : 8.56cd/m² → PQ 294
- Undershoot Delta : 5.56cd/m² → PQ 261
- Undershoot = PQ294 – PQ261 = 33



Substitute Luminance with PQ Values to Compute Differences in Over/Undershoot and Saturation Regions

Section7 - G2G tests

- VESA provides an automated test tool for G2G measurements.
 - Tool Setting : MCC USB-1608FS-Plus(DAQ) + Photo Sensor + Laptop 2ea



	0	31	63	95	127	159	191	223	255
0	0	0	4.5	4.2	4.3	4	4.7	4.4	4.1
31	2.9	0	4.2	4.1	4.2	4	4.1	4.3	4
63	3.1	0	0	3.8	3.8	3.8	3.8	4	3.8
95	3.1	0	3.3	0	3.3	3.5	3.7	3.8	3.7
127	3.1	0	3.7	3.2	0	3.3	3.4	3.5	3.7
159	3.2	0	3.9	3.7	2.8	0	3	3.1	3.6
191	3.3	0	4.1	4	3.3	2.5	0	2.7	3.6
223	3.4	0	4.2	4	3.5	2.8	2.4	0	3.6
255	3.6	0	4.4	4.4	3.9	3.2	3.3	2.4	0
Average G2G	3.7								
Max G2G: (m)	4.7	Start Level	0	End Level	191				

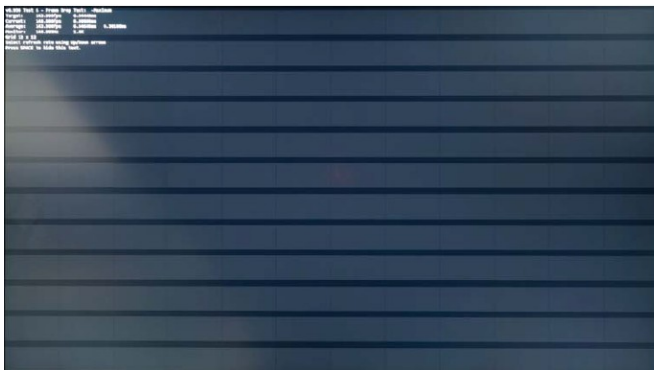
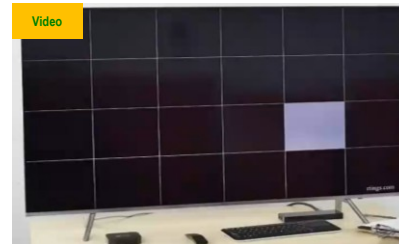
Response time

	0	31	63	95	127	159	191	223	255
0	0	0	4	8	6	8	0	0	0
31	0	0	4	7	7	7	3	0	0
63	0	0	0	5	7	7	4	0	0
95	0	0	9	0	6	6	4	1	0
127	0	0	8	8	0	3	4	2	0
159	0	0	1	7	9	0	3	3	0
191	0	0	0	3	12	10	0	3	0
223	0	0	0	1	15	19	9	0	0
255	0	0	0	0	8	21	8	7	0
Maximum CV	8	Start Level	0	End Level	95				
Maximum Un	21	Start Level	255	End Level	159				

Over/Undershoot Delta PQ

Section8 - Frame Drop Testing

- Purpose: To verify frame drop
- Test Pattern: A single white block moves one cell per frame
 - Testing frequency : Max refresh rate/ Random refresh rate
- Requirement : The camera shutter speed was set to 1 second to capture the screen. No dropped boxes were observed in the captured image.



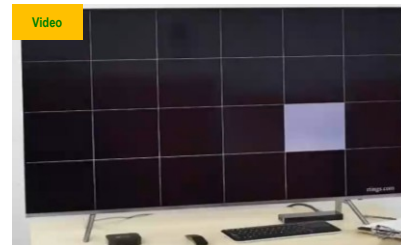
Pass



Fail

Section9 - Jitter Testing

- Purpose: To verify video signal output errors
- Test Pattern: Same as the Frame Drop Testing pattern
 - Testing Frequency: 23.976, 24, 25, 29.97, 30, 47.952, 48, 50, 59.94, 60 Hz
- Requirement : Capture the moving block twice over a 1-second exposure using a camera. Check for luminance variation in each block
 - Use Photoshop to check the Code Value Delta for each block (refer to CTS requirements for acceptable thresholds)



Ignore one or two unusually bright or dark frames



Capture 1

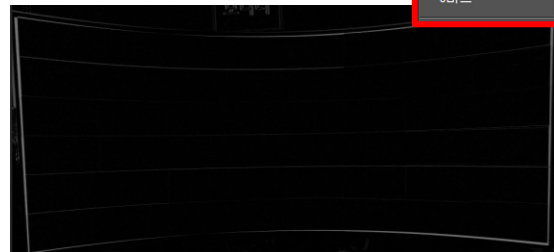
+



Capture 2



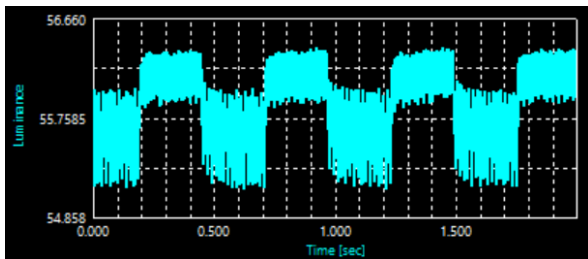
Photoshop
compositing



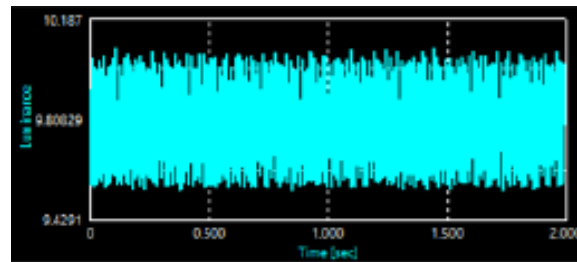
Pass

Section10 - HDR Testing

- Purpose: To verify whether Adaptive-Sync operates correctly under HDR On conditions
- Test Pattern: Square wave signal used in flicker testing
 - Min $\leftrightarrow$ Max every 250 ms
- Requirement : Check if luminance variation patterns remain consistent across different frame rates, indicating proper Adaptive-Sync operation



Pass



Fail



ClearMR™ v1.1

: Specifications and Compliance Testing Overview

Yongwoo Yi

Samsung Display Co. Ltd.

Oct. 31. 2025

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Introduction

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화면 잔상과 번짐을 줄여 디테일까지 선명하게 세계 최초 VESA ClearMR 21000 인증

화면 전환이 빠른 영상 재생 시 꼬림 현상을 수치화하는
VESA ClearMR(Clear Motion Ratio) 인증에서
가장 높은 21000 등급 인증을 세계 최초로 획득해 게임 잔상과
번짐 없이 작은 디테일까지 부드럽고 선명하게 표현합니다.



* 소비자의 이해를 돕기 위해 연출된 영상으로, 실제와 차이가 있을 수 있습니다.

* VESA ClearMR 21000 인증 관련

- ① 인증대상(부품여부, 모델명 등) : 27GX790A
 - ② 인증기관 : VESA
 - ③ 인증내용 : VESA certified ClearMR
 - ④ 인증조건(인증기준 등) : 공식 사이트 참조(<https://www.clearmr.org/performance-criteria/>)
 - ⑤ 인증증빙번호(특허인 경우, 특허등록번호) : 공식 사이트 참조(<https://www.clearmr.org/certified-products/>)
- * 2025년 1월 1일 기준 VESA ClearMR 인증 중 가장 높은 등급은 21000 등급으로 27GX790A만 획득 하였습니다.
(2024년까지는 13000 등급이 가장 높은 등급임)

AORUS FO27Q5P

주요 특징 상세 정보 지원 뉴스/수상 내역 사진 갤러리



게이밍 강점

QD-OLED 기술로 게임의 최대 강점을 얻을 수 있습니다. 빠른 반응과 확실한 영료함으로 게임 플레이를 새로운 차원으로 끌어 올립니다.

10배 빠른 반응시간

0.03ms
반응시간

고스트 이미지 없음

590Hz
재샘플

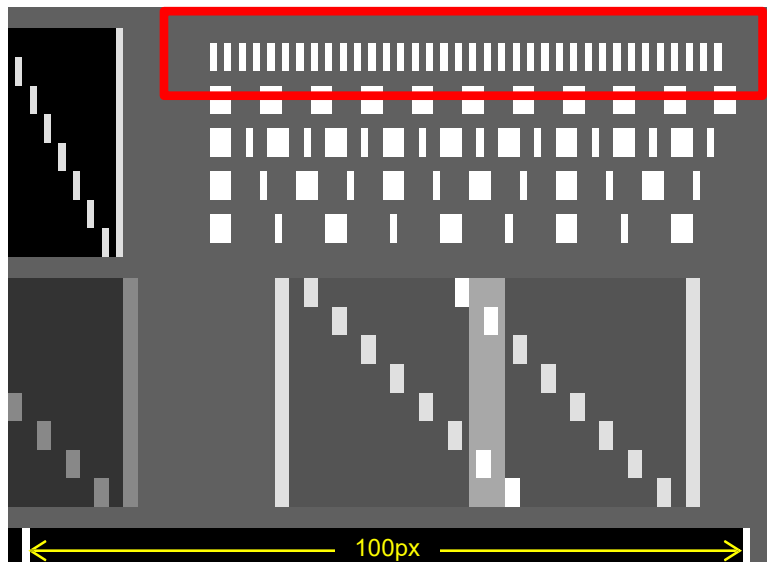
테어링 및 스테리링 없음

 **NVIDIA
G-SYNC**

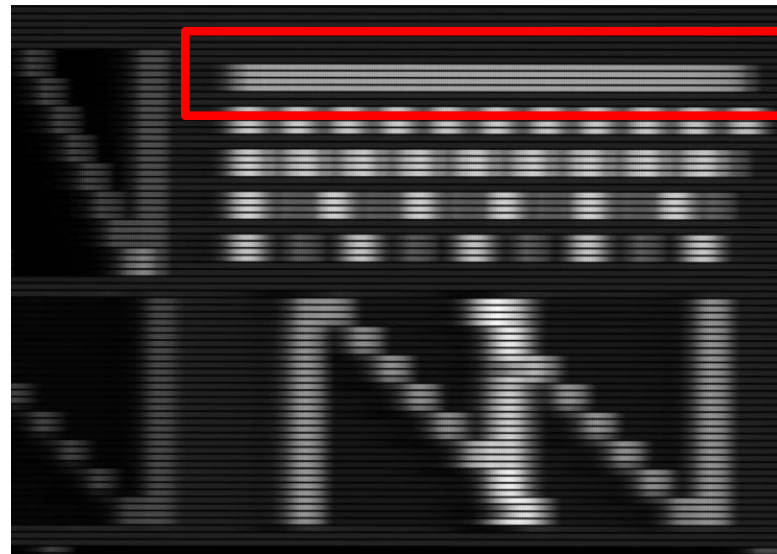
최고 수준의 모션 명확도

 **VESA CERTIFIED
ClearMR 21000**

Blur beyond recognition

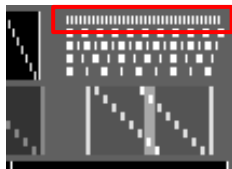


still frame of the actual pattern

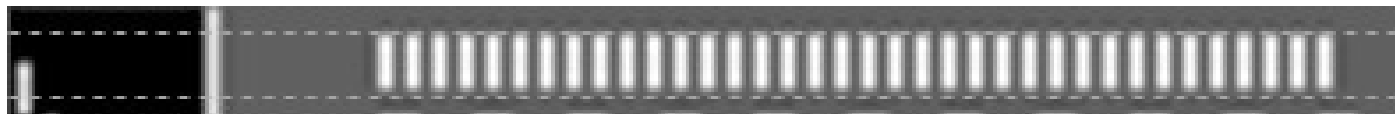


motion composite showing blur similar to what humans might see

Blur beyond recognition



Actually, vertical lines 2 pixels wide, 2 pixels apart

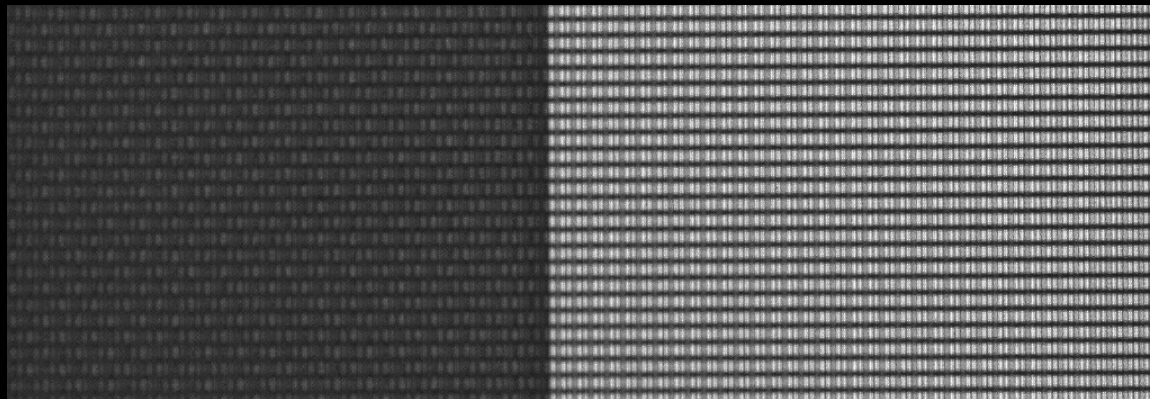


Horizontal lines?



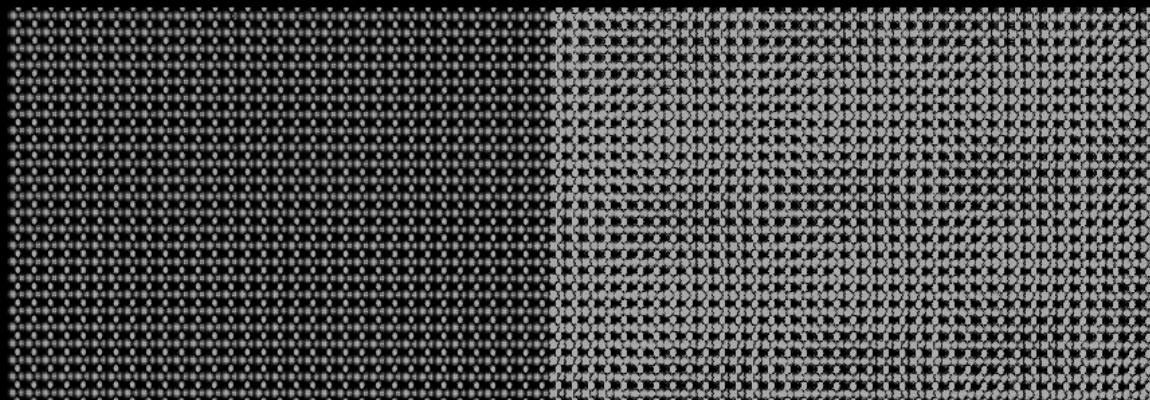
Product A 240Hz

$$10000 / 240 = 41.67$$



Product B 175Hz

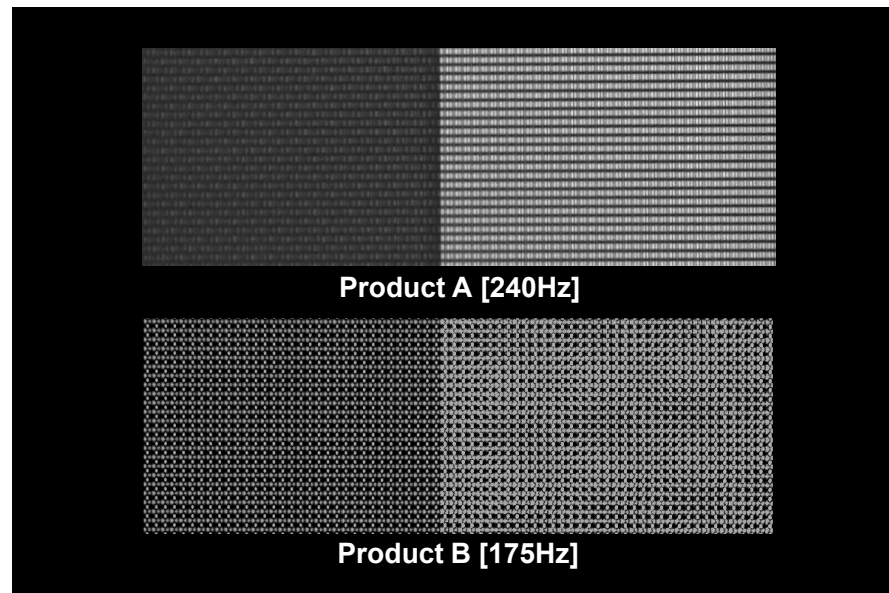
$$10000 / 175 = 57.14$$



* 1 frame Captured by High-Speed Camera(10,000 fps)

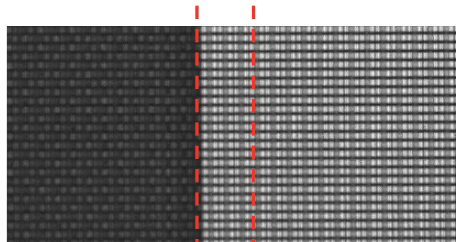
The problem statement

- **How blurry is the picture**
- Is blur by Product A the same as blur by Product B?
- What metric/method is best for quantifying blur?
 - Hertz (Hz)
 - milliseconds (ms)
 - G2G? MPRT?

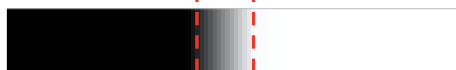


Blur profile

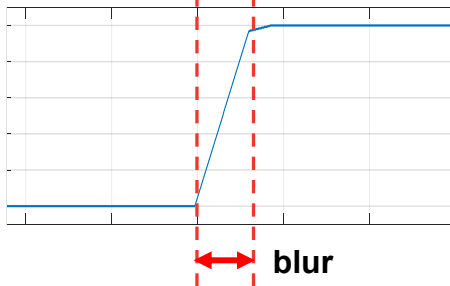
Motion picture



Blur image



Blur profile

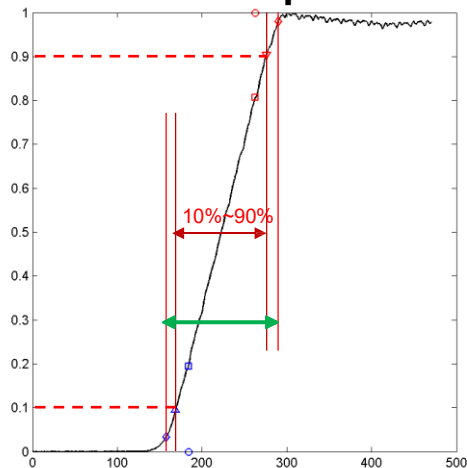


Blur vs. MPRT(Moving Picture Response Time)

• MPRT [ms]

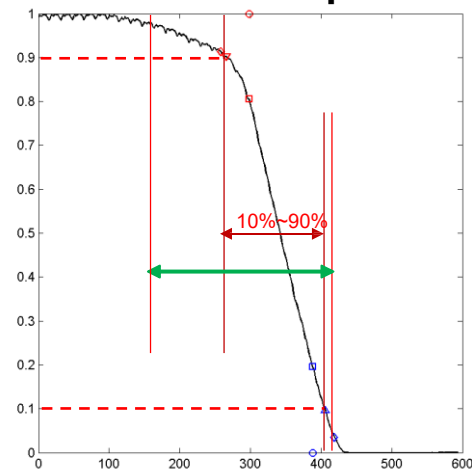
- only analyzes 80% of light
- Incorrectly assumes linearity outside of 10% and 90%

Linear blur profile



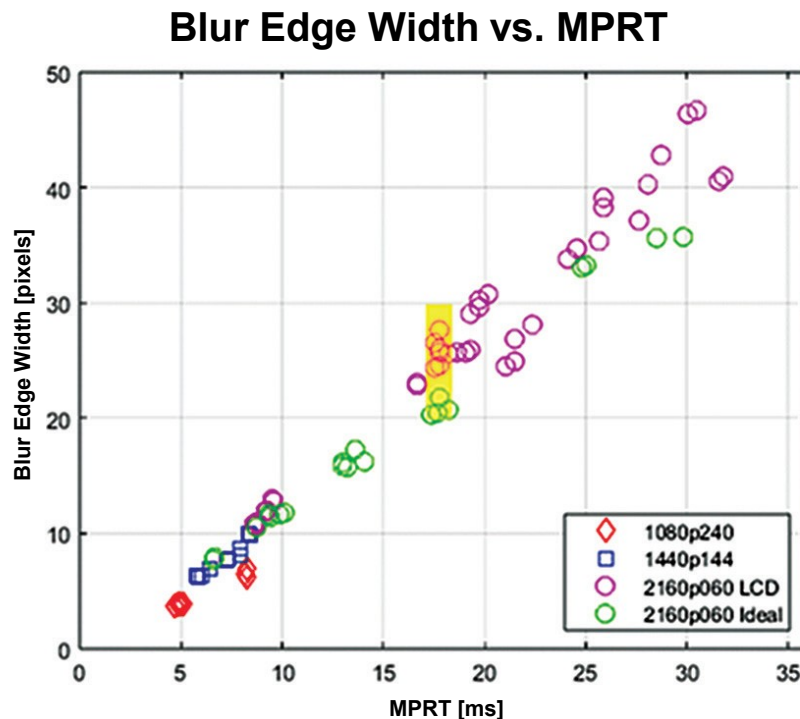
$$\text{blur profile} \sim k_{\text{scale}} \times \text{MPRT}$$

Non-linear blur profile



$$\text{blur profile} \neq k_{\text{scale}} \times \text{MPRT}$$

Blur vs. MPRT(Moving Picture Response Time)



A new metric : Clear Motion Ratio (CMR)

- **No objective blur description**
 - Gray-to-gray is a step response, do not explain the full picture
 - MPRT only analyzes 80% of light
- **A new metric must:**
 - Capture all the display light output
 - Be suitable for high density displays > 300 ppi
 - Be repeatable
 - Make fair points of comparison (eg. Limit overdrive to eliminate ghosts)

✓ ClearMR uses the new metric, Clear Motion Ratio (CMR) for a *better* and *fairer* measure of display blur.

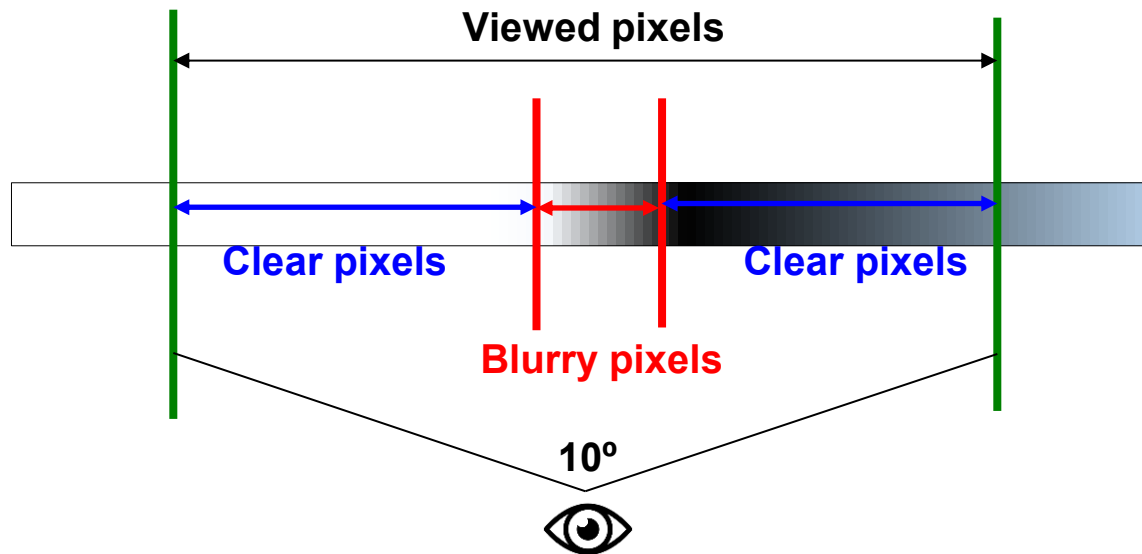
Methods

01 Problem statement

02 Clear Motion Ratio design

03 Seeing is believing

ClearMR index : CMR



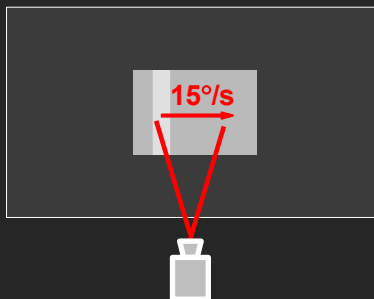
$$\text{CMR} = \frac{\text{Clear pixels}}{\text{Blurry pixels}}$$

ClearMR : Theory of Operation

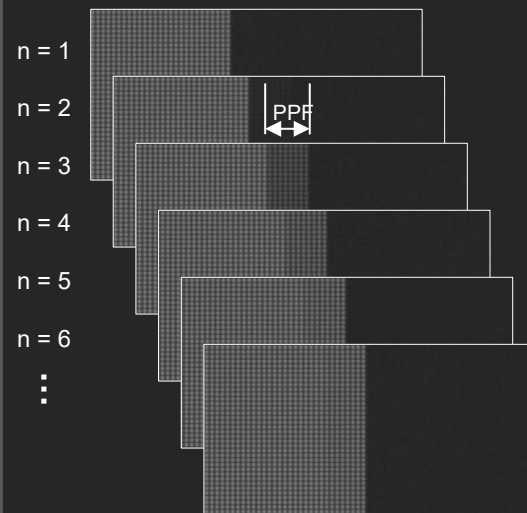
Concept



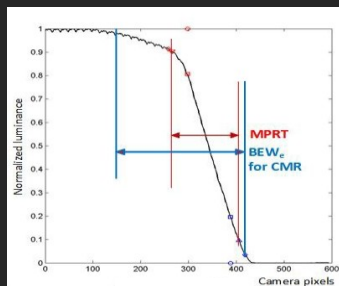
Test pattern and capture



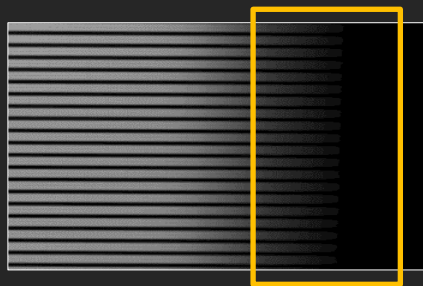
Frame stack



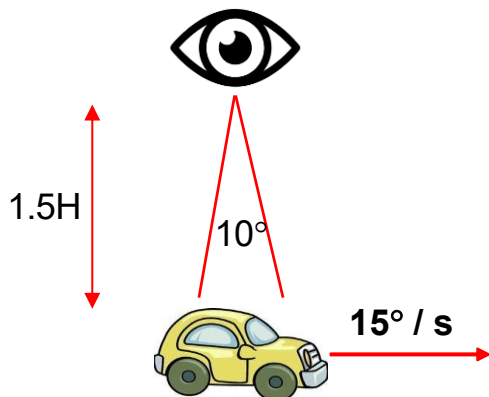
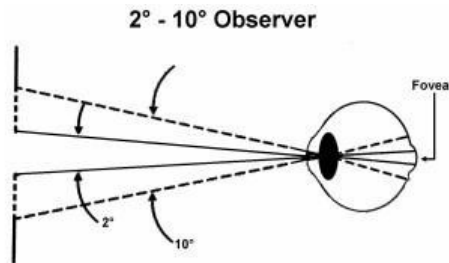
Blur profile



Blur image composition

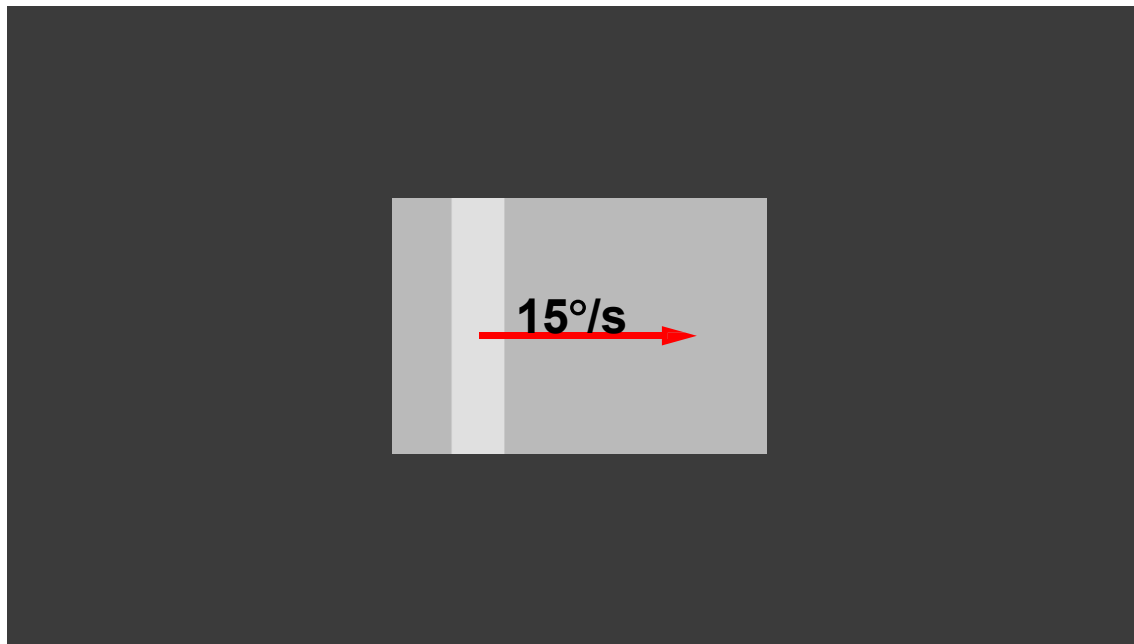


Concept

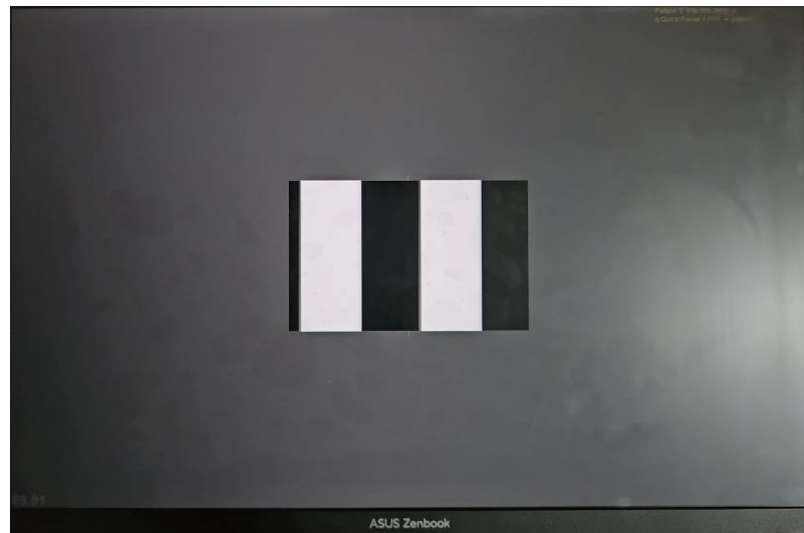
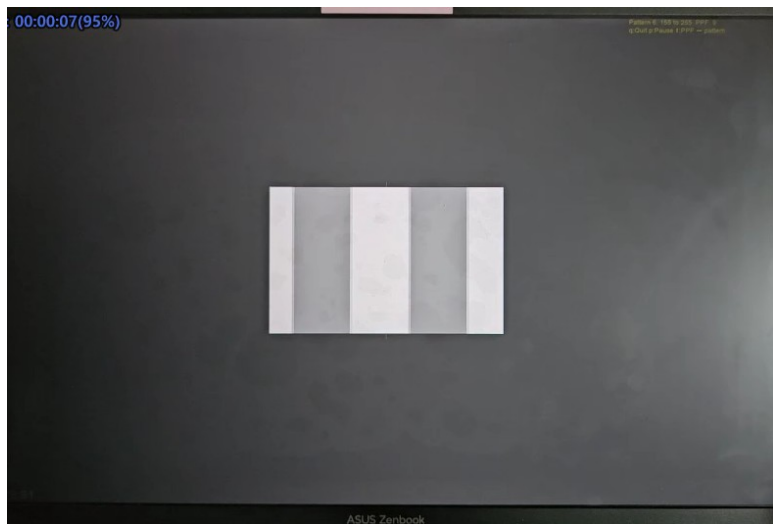


- **Determine pixels viewed when eye tracking**
 - Use a focus area similar to the CIE Standard Observer
 - **10°** field of view good for motion
 - 2° model would apply to fixed objects
 - Viewing distance at **$1.5H$** (height)
 - Fast motion but does not exceed human tracking capability
 - **$15^\circ/s$** angular velocity (v_θ)
 - $\sim 4s$ to cross a 16:9 screen (61.3°)

Test pattern

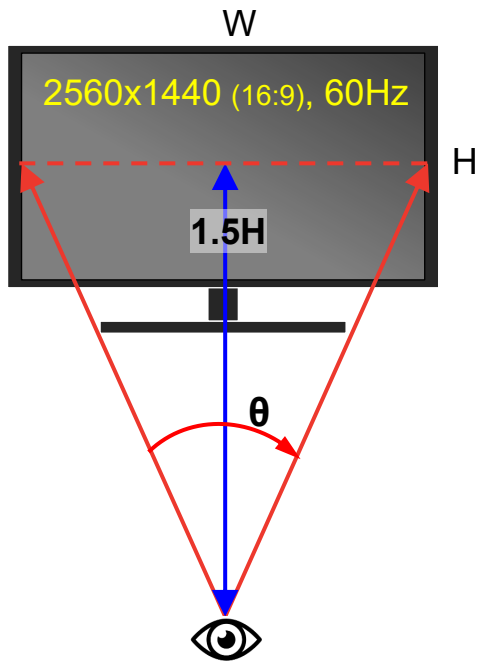


Test pattern



Pattern speed : PPF

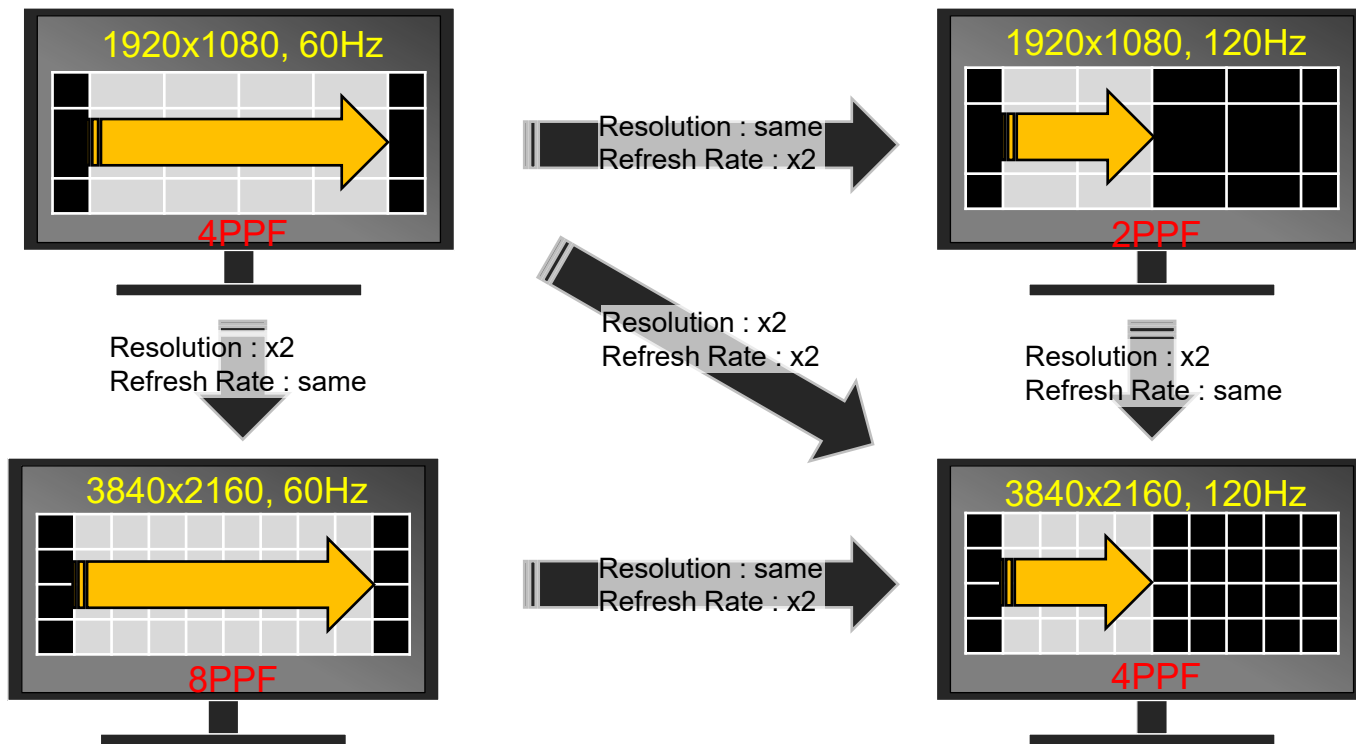
- $15^\circ/\text{s} \rightarrow \text{PPF}$ (pixel per frame)



$$\begin{aligned} \tan\left(\frac{\theta}{2}\right) &= \frac{W/2}{1.5H} = \frac{\frac{16}{9}H}{3H} = \frac{16}{27} \\ \rightarrow \tan^{-1}\left(\frac{16}{27}\right) &= \frac{\theta}{2} \\ \rightarrow \theta &= 2 \cdot \tan^{-1}\left(\frac{16}{27}\right) = 61.3^\circ \end{aligned}$$

$$\begin{aligned} \bullet \frac{\text{Horizontal pixels}}{\theta} &= \frac{2560_{px}}{61.3^\circ} = 41.76_{px/^\circ} \\ \bullet \frac{\text{Angular velocity}}{\text{FPS}} &= \frac{15^\circ/\text{s}}{60 \text{ frame/s}} = 0.25^\circ/\text{frame} \\ \bullet 41.76_{px/^\circ} \times 0.25^\circ/\text{frame} &= 10.44_{px/\text{frame}} \end{aligned}$$

Pattern speed : PPF



Pattern speed : PPF

<i>FPS</i> [Hz]	<i>hres</i> [pixels]	<i>vres</i> [pixels]	<i>PPF(REAL)</i> [pixels/frame]
60	1920	1080	7.830
60	3840	2160	15.660
120	1920	1080	3.915
120	3840	2160	7.830

1920x1080, 60Hz

4PPF

1920x1080, 120Hz

2PPF

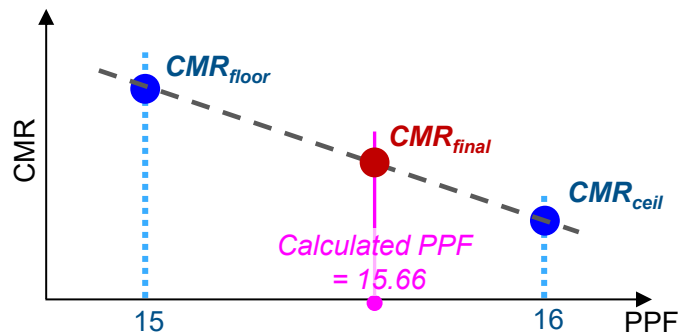
3840x2160, 60Hz

8PPF

3840x2160, 120Hz

4PPF

- Calculated PPF is Real number
- flooring & ceiling
- Logarithmic Interpolation



Pattern speed : scaled PPF (New in v1.1)

VESA ClearMR v1.1 (Build:07.31.2023)

Input

Base FPS: 240.000

Reduce by 1/1.001: ☒

Test Pattern: 1. 0 to 155

Visible Screen Diagonal(in): 32

Magnification: 12

Camera

Sensor Density(ppcm): 500

Camera shutter rate(fps): 10000

Output

hres x vres: 2560 x 1440

Target FPS: 239.760

PPF(real), PPF(test): 2.613, 2.613

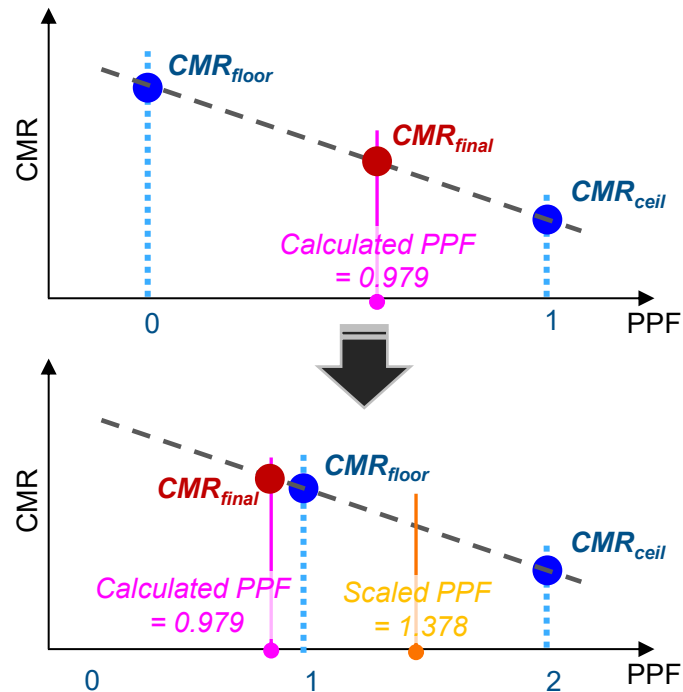
Floor(PPF), Ceil(PPF): 2, 3

Ideal Magnification: 11.761 - 13.836

f_cnt: 41

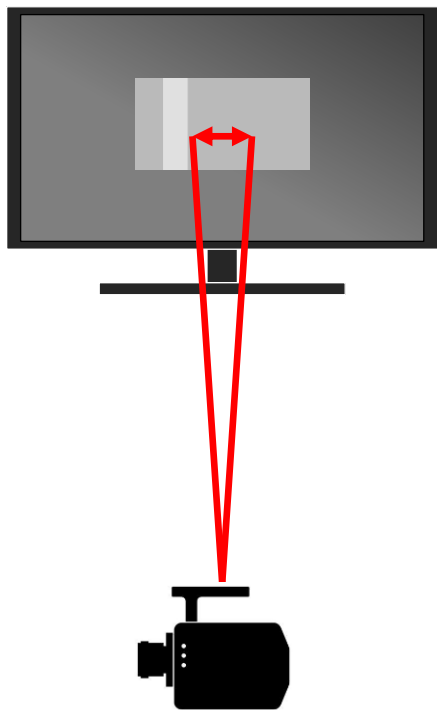
Go

(c) 2020-2023 Samsung Display Co., Ltd. All Rights Reserved.

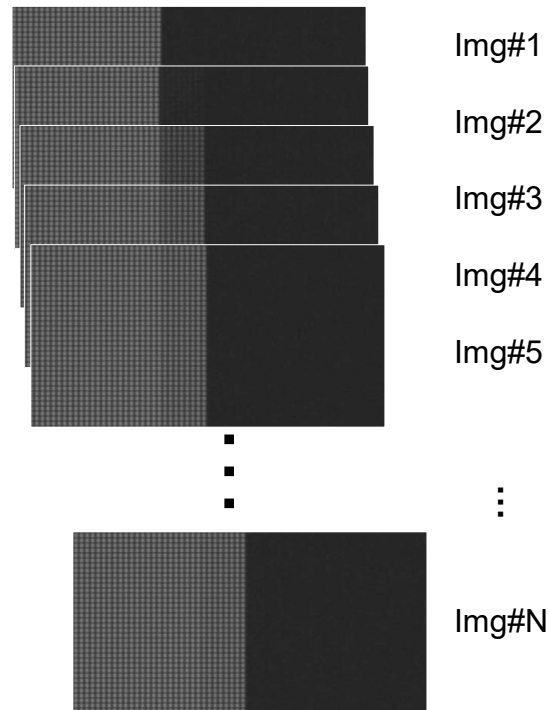


✓ Read [the Information Display article](#) for the update details

Image captured by high-speed camera



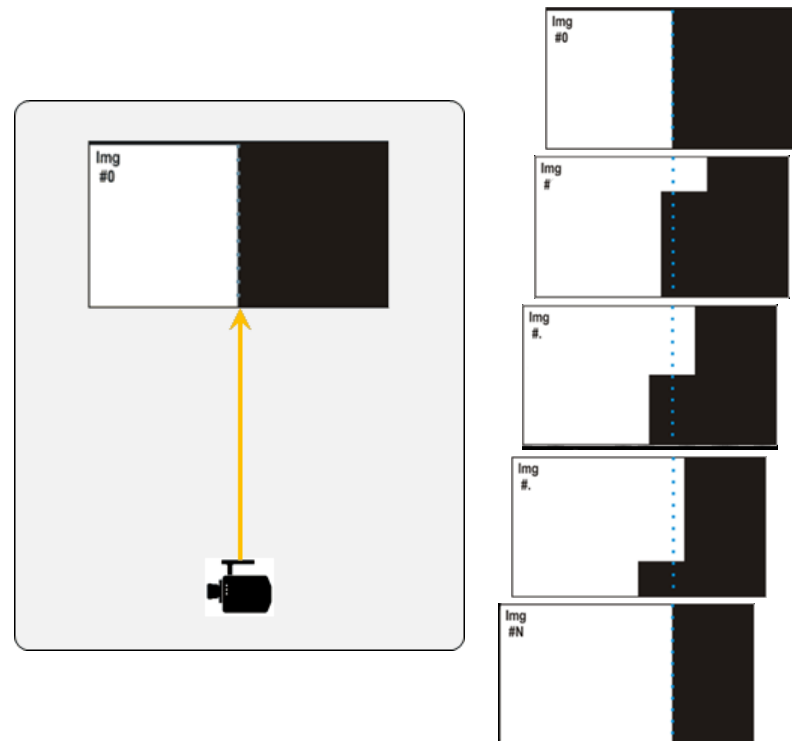
High-speed Camera



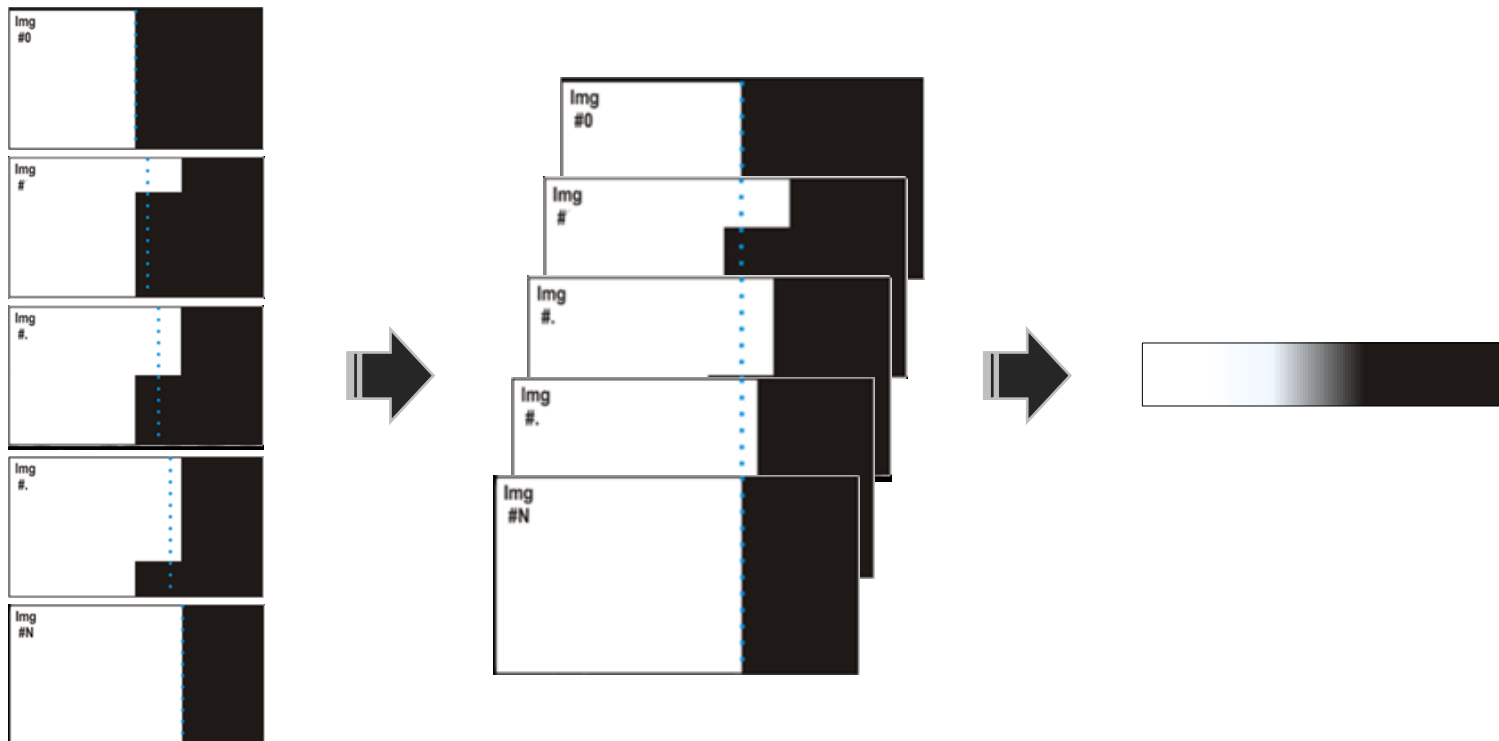
1 frame captured by high-speed camera

ex) 240Hz monitor with 10,000fps camera $\rightarrow N = 10000/240 = 41.67$

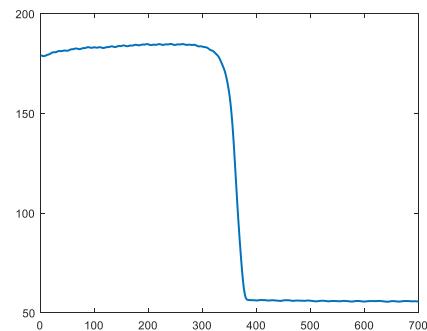
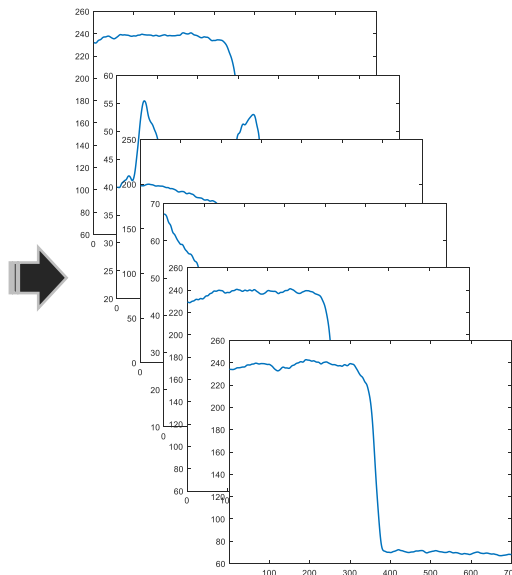
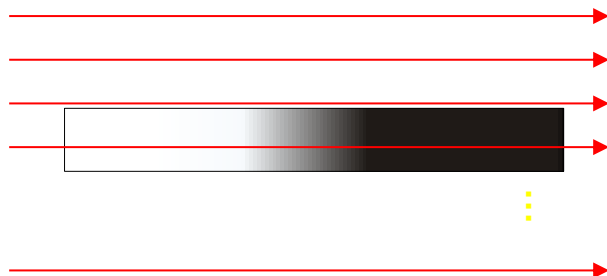
Blur image composition



Blur image composition

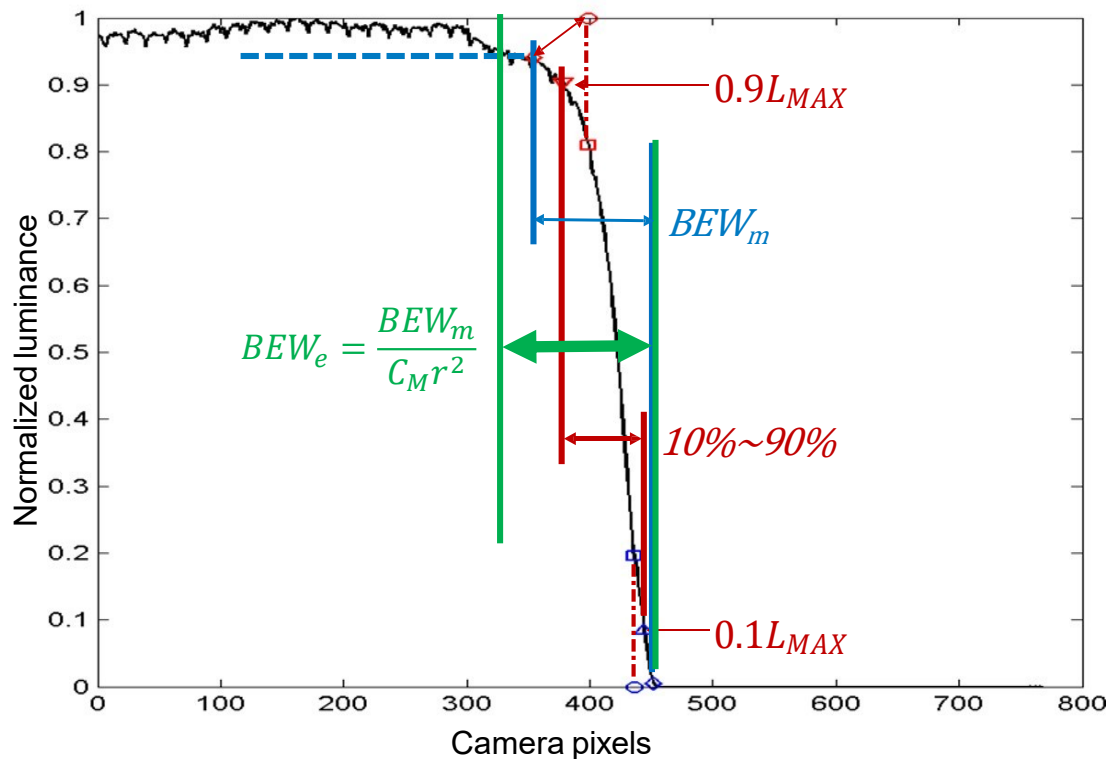


Blur profile



blur profile
= Vertically averaged blur image

Profile identifies the Blur Edge Width (BEW)



- Accounts for non-linearity
- Accounts for light outside of BEW_m
- Challenge: calculation should include all luminance change
- BEW_m is between the knees ($\diamond$) of the profile
- BEW_e corrects for non-linearity of the profile locus outside of BEW_m

* BEW_m : measured BEW

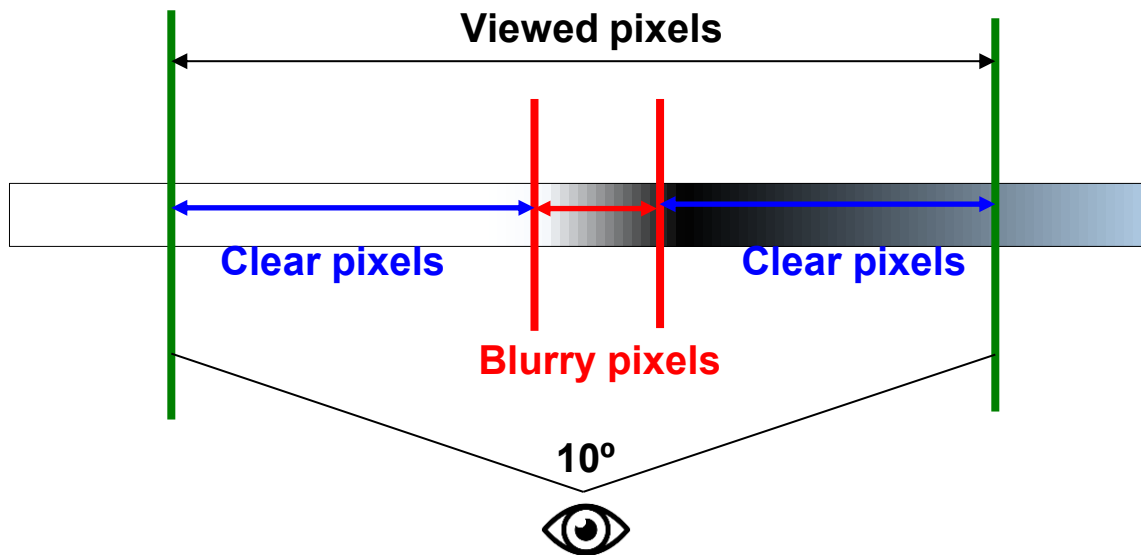
* BEW_e : effective BEW

* C_m : contrast modulation

* r^2 : coefficient of determination

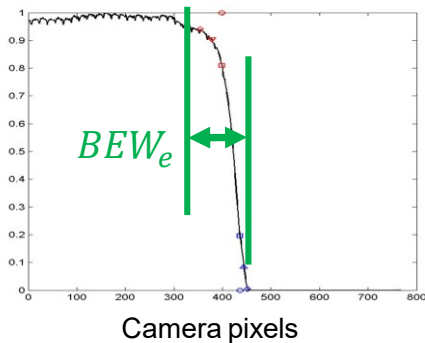
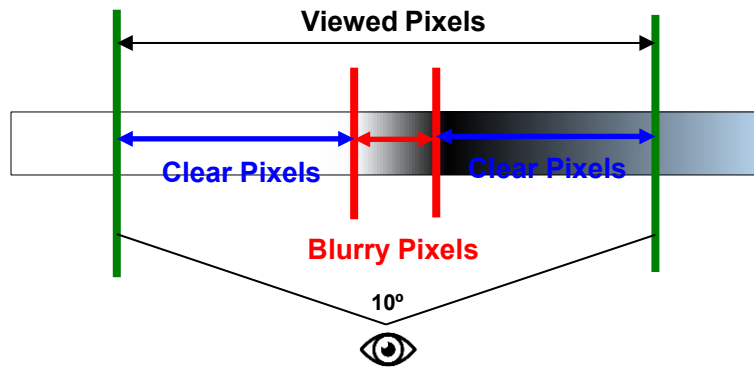
CMR(Clear Motion Ratio)

Clear Motion Ratio : Ratio of *Blurry pixels* and *Clear pixels* in a 10° FOV with Viewing distance at $1.5H$



$$\text{CMR} = \frac{\text{Clear pixels}}{\text{Blurry pixels}}$$

CMR(Clear Motion Ratio)



$$CMR = \frac{\text{Clear pixels}}{\text{Blurry pixels}}$$

$$\text{Viewed pixels} = 2d_v v_{res} \tan\left(\frac{arc}{2}\right)$$

$$d_v = 1.5H$$

$$v_{res} = \text{Display Vertical Resolution}$$

$$arc = 10^\circ$$

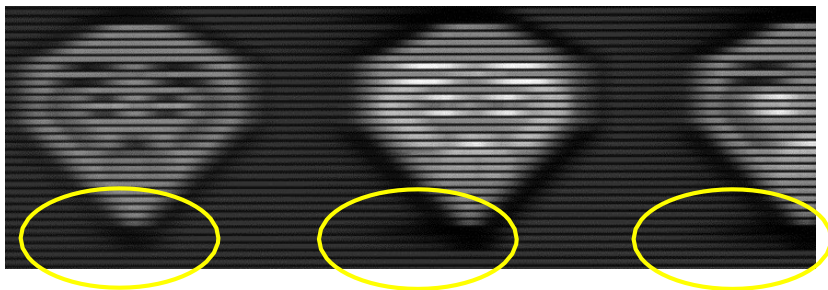
$$\text{Blurry Pixels} = BEW_e$$

$$\text{display pixels} = \text{camera pixels} \times \frac{\text{display pixel density}}{\text{camera pixel density}}$$

Ghosts and Coronas

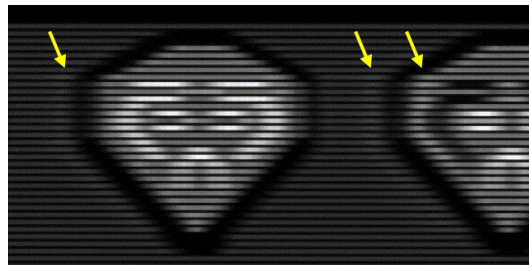
- **Ghosts**

- Uneven transitions
- Trailing artifact
- Usually, a dark trail



- **Coronas**

- Inverse of ghosts
- Over-shooting the final pixel value
- A trailing glow

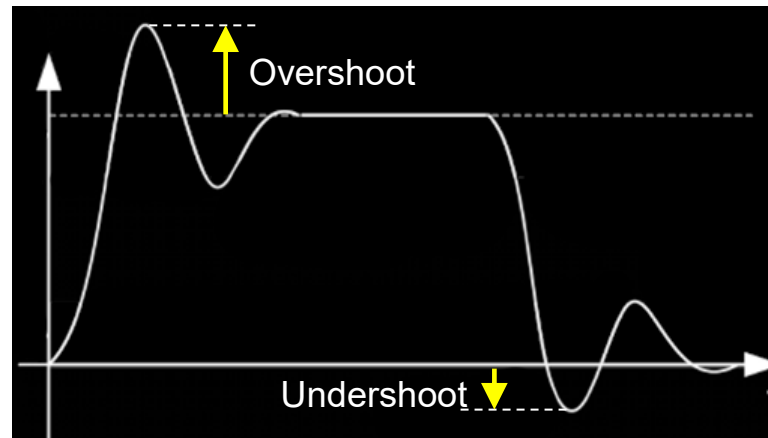
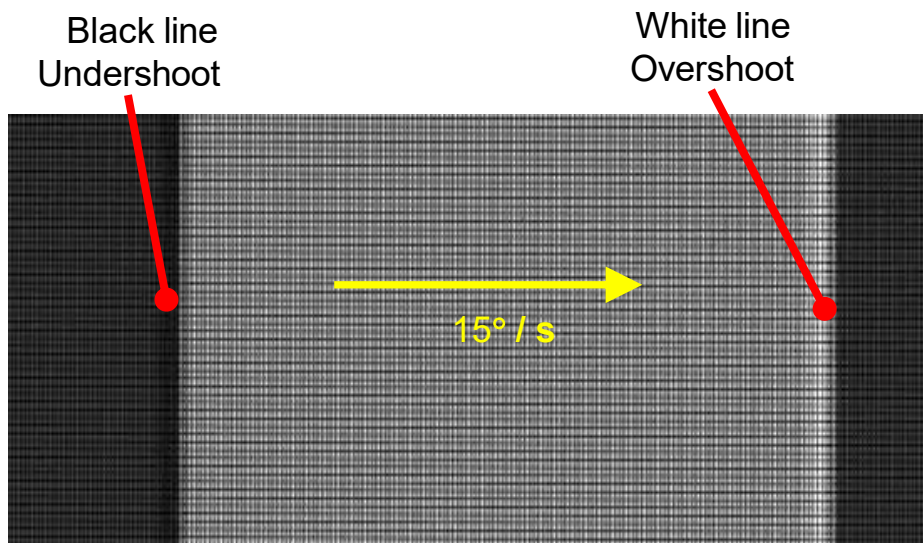


Working definitions by Mark Rejhon (2021)¹...

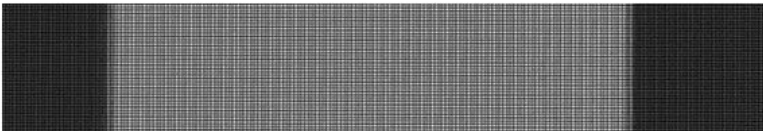
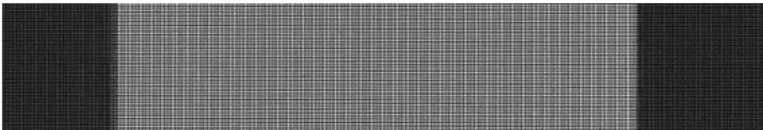
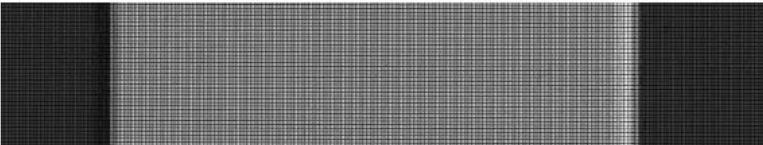
1. Accessed July 26, 2021. <https://blurbusters.com/faq/lcd-motion-artifacts>

2. Test patterns © 2021, Samsung Display Co., Ltd. right reserved.

Over/undershoot creates ghosts and coronas

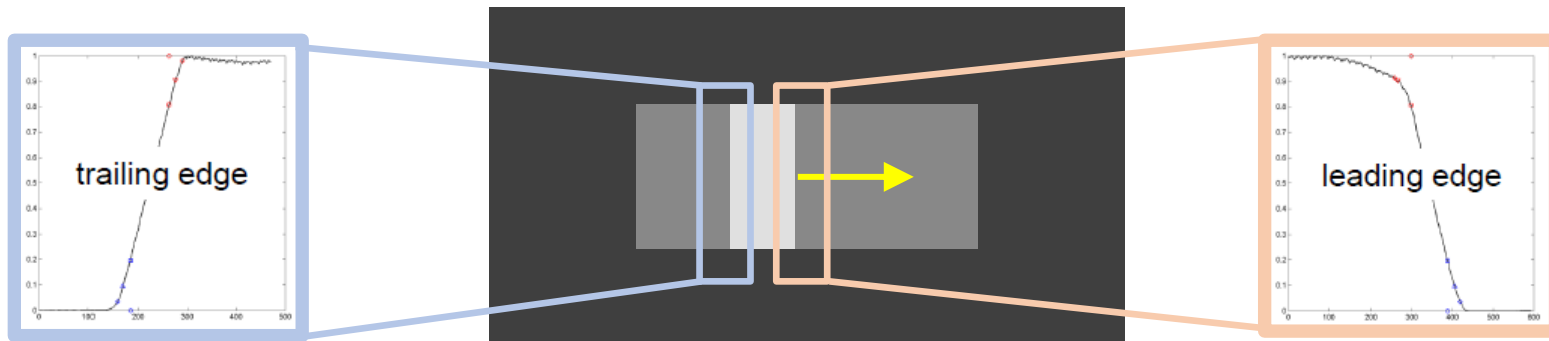


Moving bar subjective test

Picture		Views	Leading Edge seen	Trailing edge seen	Fractional response
		Test image	40		
		Default	8	0	0
		Increased overdrive	16	7	0.41
		Excessive overdrive	16	16	1.0

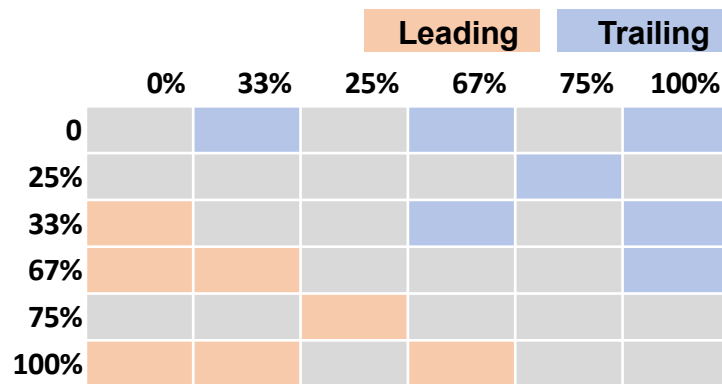
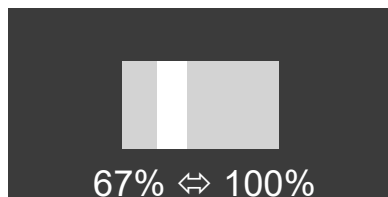
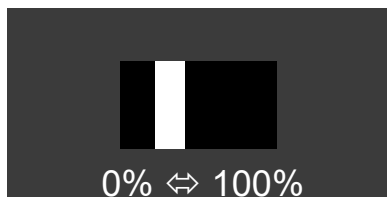
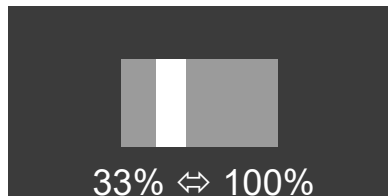
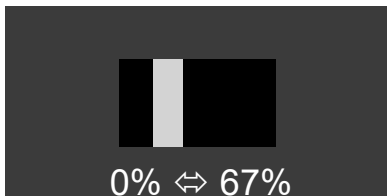
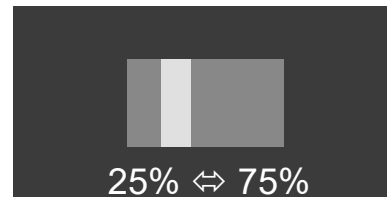
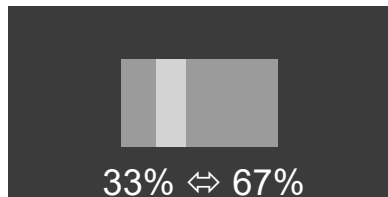
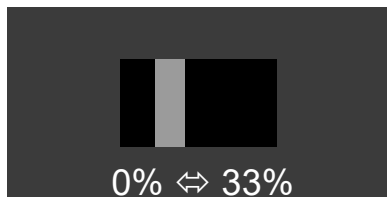
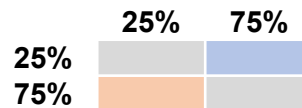
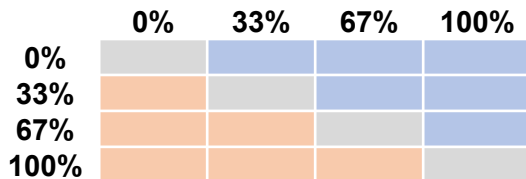
Overshoot < 20%, Undershoot < 10%

Rising and Falling (Leading and Trailing)



	Leading				Trailing	
	0%	33%	25%	67%	75%	100%
0						
25%						
33%						
67%						
75%						
100%						

Rising and Falling (Leading and Trailing)



Conclusion

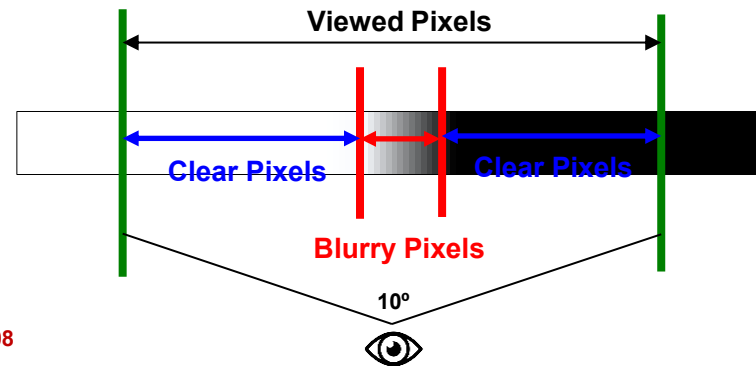
01 Problem statement

02 Clear Motion Ratio design

03 Seeing is believing

ClearMR Tiers

ClearMR TIER	CMR Range
3000	2500 ≤ CMR < 3500
4000	3500 ≤ CMR < 4500
5000	4500 ≤ CMR < 5500
6000	5500 ≤ CMR < 6500
7000	6500 ≤ CMR < 7500
8000	7500 ≤ CMR < 8500
9000	8500 ≤ CMR < 9500
10000	9500 ≤ CMR < 10500
11000	10500 ≤ CMR < 11500
12000	11500 ≤ CMR < 12500
13000	12500 ≤ CMR < 14000
15000	14000 ≤ CMR < 16500
18000	16500 ≤ CMR < 19500
21000	19500 ≤ CMR



$$\text{CMR} = \frac{\text{Clear pixels}}{\text{Blurry pixels}}$$

Mfr	Product/Model Number	Screen Size	Resolution	Frame Rate	ClearMR™ Tier
AOC	AG276QKD	27"	QHD	480Hz	13000
AOC	AG276QSD Series	27"	QHD	360Hz	18000
AOC	AG276QZD2	27"	QHD	240Hz	10000
AOC	AG276QZD Series	27"	QHD	240Hz	10000
AOC	AG276G4Z Series	27"	QHD	240Hz	10000
AOC	AG277QZ Series	27"	QHD	240Hz	10000
AOC	AG276QZD/P	27"	QHD	240Hz	10000
AOC	AG326UD Series	32"	4K	165Hz	10000
AOC	AG326UZD Series	32"	UHD	240Hz	10000
AOC	AG346UCD	34"	UWQHD	175Hz	10000
AOC	AG456UC7D	45"	UWQHD	144Hz	10000

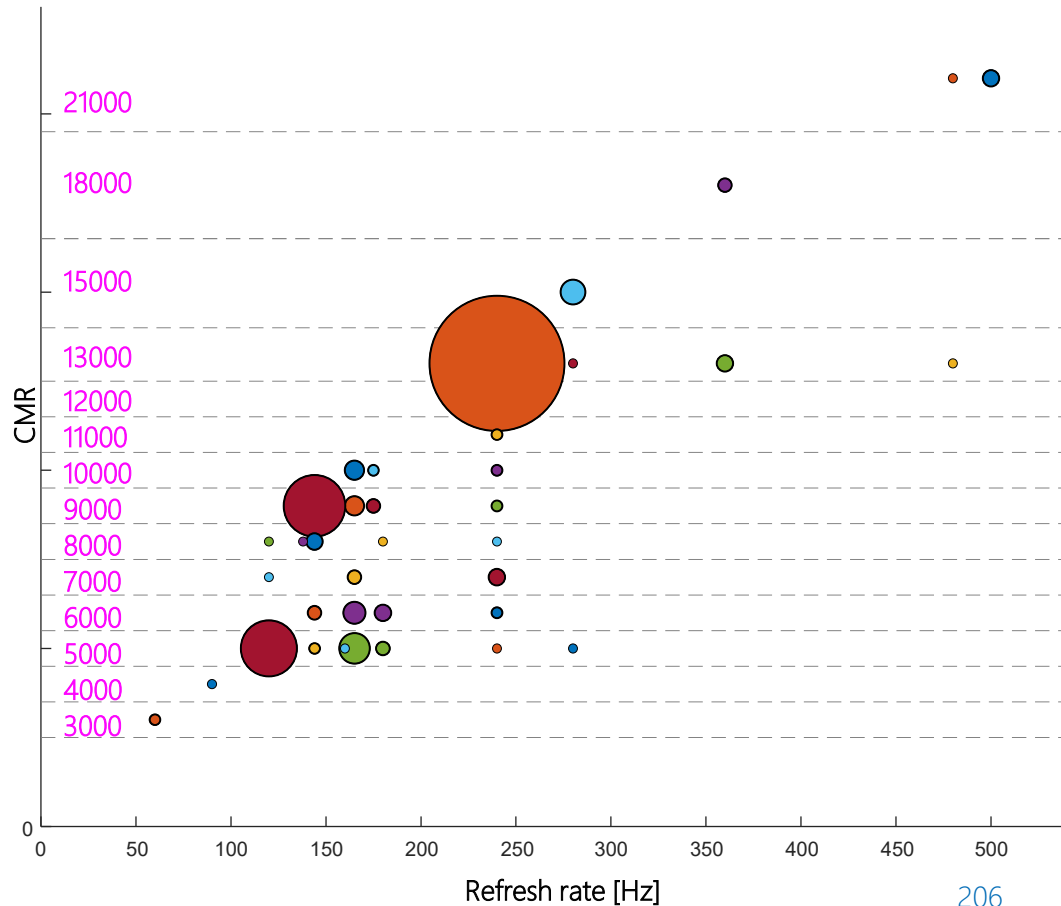
Category	Percentage
Monitor or Laptop	66%
TV	14%
Laptop or Tablet	20%

Refresh Rate	Percentage
240-280Hz	39%
160-180Hz	24%
144Hz	28%
>300Hz	7%
120-160Hz	2%

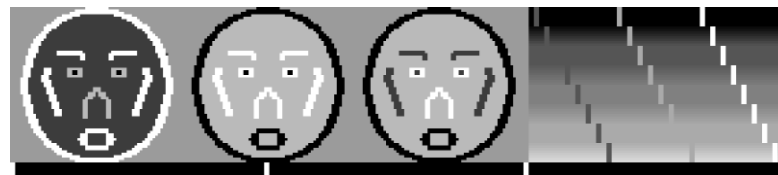
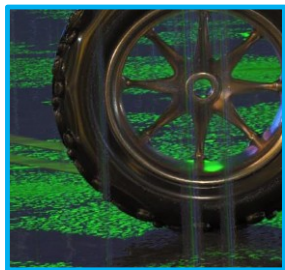
Resolution	Percentage
10K-13K	36%
6K-9K	34%
3K-5K	21%
480Hz	1%
360Hz	4%
500Hz	2%

ClearMR Tiers

ClearMR TIER	CMR Range
3000	$2500 \leq \text{CMR} < 3500$
4000	$3500 \leq \text{CMR} < 4500$
5000	$4500 \leq \text{CMR} < 5500$
6000	$5500 \leq \text{CMR} < 6500$
7000	$6500 \leq \text{CMR} < 7500$
8000	$7500 \leq \text{CMR} < 8500$
9000	$8500 \leq \text{CMR} < 9500$
10000	$9500 \leq \text{CMR} < 10500$
11000	$10500 \leq \text{CMR} < 11500$
12000	$11500 \leq \text{CMR} < 12500$
13000	$12500 \leq \text{CMR} < 14000$
15000	$14000 \leq \text{CMR} < 16500$
18000	$16500 \leq \text{CMR} < 19500$
21000	$19500 \leq \text{CMR}$



Simulated results : Seeing is believing

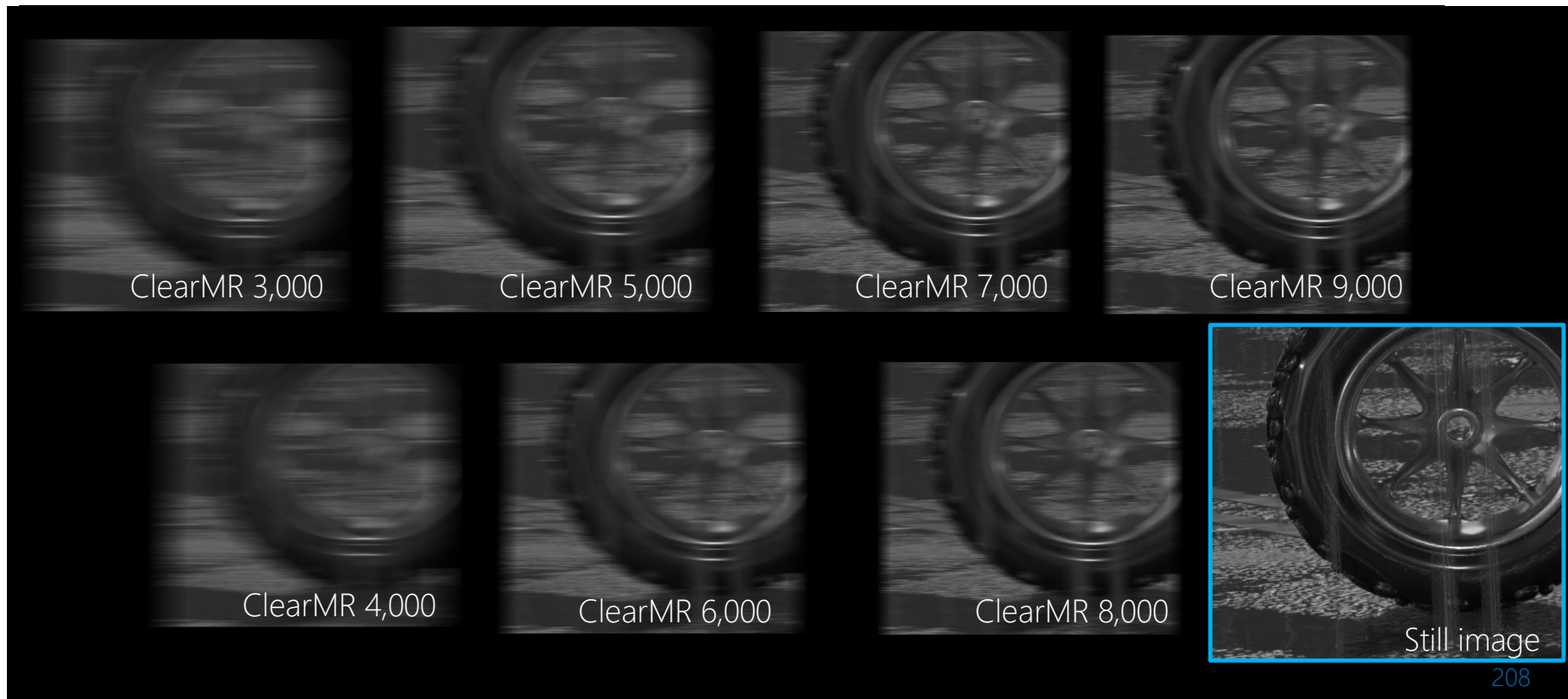


- Ideal edges, $C_M = 1$, $r^2 = 1$
- Show on 2560 x 1440 display

* ambientCG images are 400 x 400 from York University, licensed under a Creative Commons BY 4.0 license)

* Grayscale test pattern 300 x 70 © 2022 Samsung Display Co., Ltd. rights reserved.

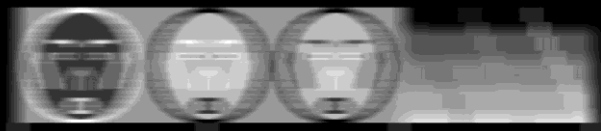
Animated tire



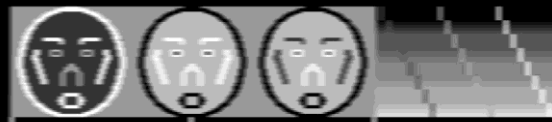
Animated tire



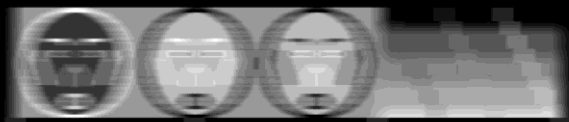
Grayscale cartoons and diagonal bars



ClearMR 3,000



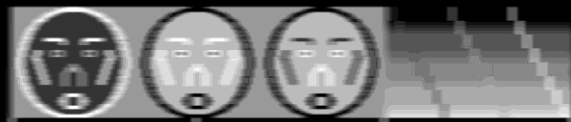
ClearMR 7,000



ClearMR 4,000



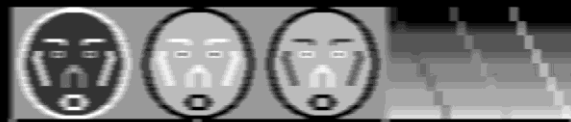
ClearMR 8,000



ClearMR 5,000



ClearMR 9,000

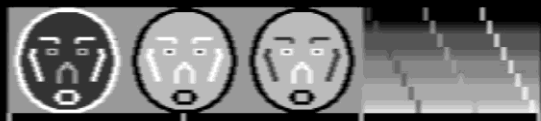


ClearMR 6,000



Still image

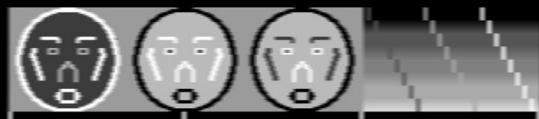
Grayscale cartoons and diagonal bars



ClearMR 9000



ClearMR 14000



ClearMR 11000



ClearMR 15000



ClearMR 12000



ClearMR 16000



ClearMR 13000



Still image



9K



13K



15K



15K



19K

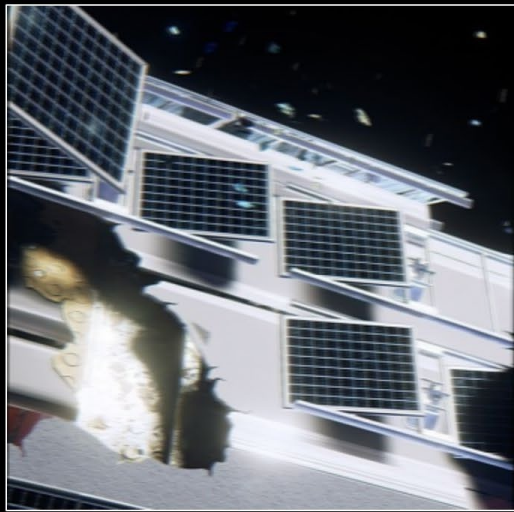


21K

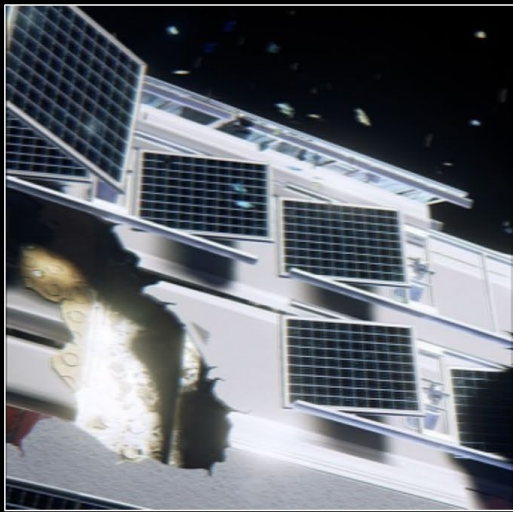




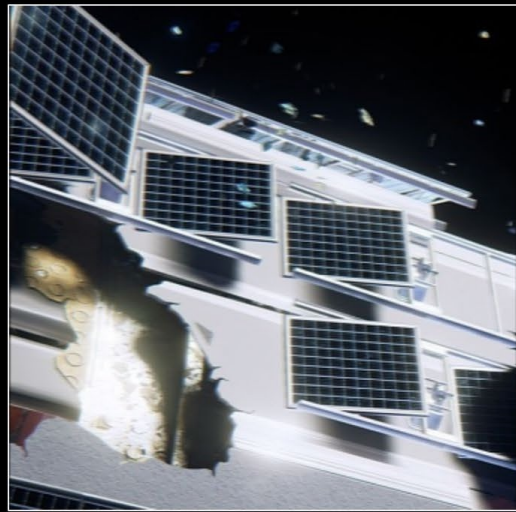
9K



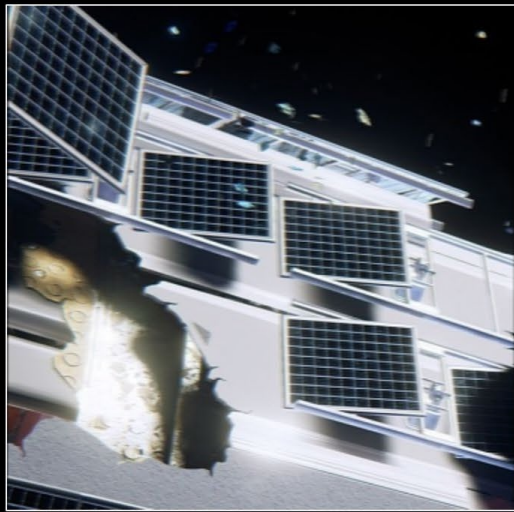
13K



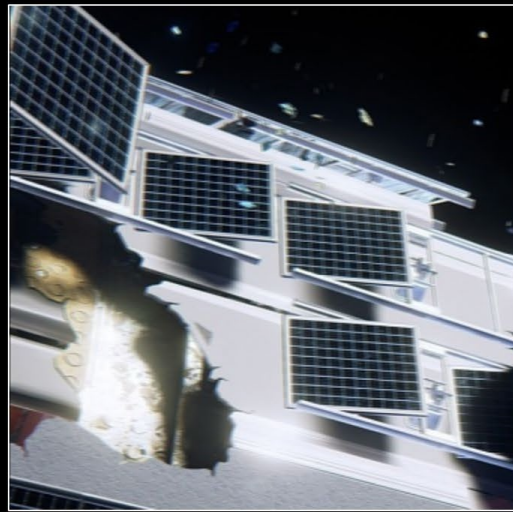
15K



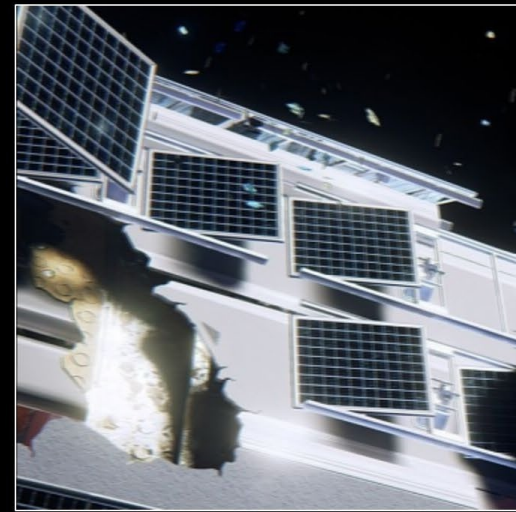
15K



19K



21K



Summary

- **ClearMR** can serve as an accurate metric of how clearly a display renders visual content.
- Since **ClearMR** first release in **August 2022**, more than 170 products have been certified to date, which has helped consumers compare motion blur among certified products using a true quality metric for motion performance
- As display driving technologies advance rapidly and the motion characteristics of displays evolve accordingly, **VESA** will continue to advance **ClearMR** in step with these developments.



Razor Sharp

Visit www.clearmr.org for the latest certifications and test details.

Thank you

Yongwoo Yi

yongwoo.yi@samsung.com

DP Alt Mode v 2.1a Overview and Updates

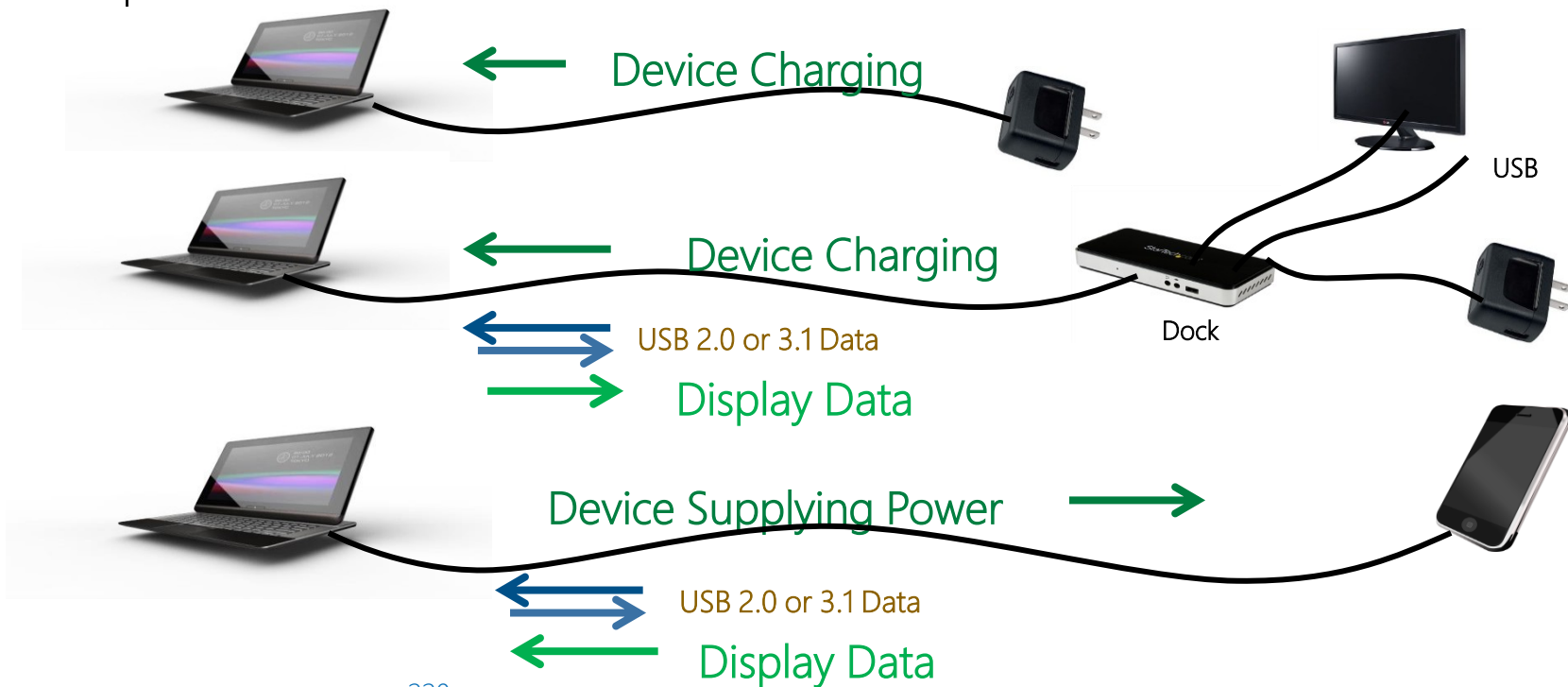
Tim Wei– Senior Application Engineer

Ellisys

Oct 31, 2025

Example USB Type-C Configurations

Either end can serve as USB Host, USB-PD Power Consumer, and DisplayPort Video Source (these services are independent of each other)



DP Alt Mode over USB-C Ecosystem is Mainstream



USB-C Tablets



USB-C Laptops



USB-C Displays



Multi Function Adapters

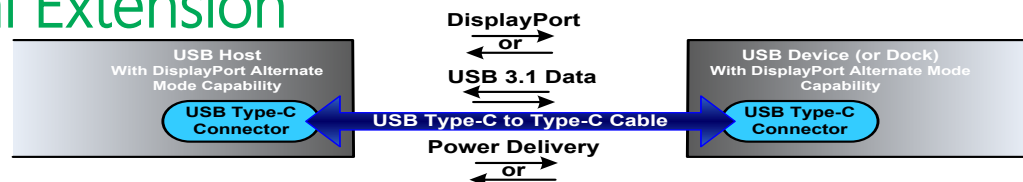
All types of certified adapters available

- C to DP adapters, Multifunction docks
- Type C protocol converters (HDMI, VGA, DVI) using DP Alt Mode

More are certified every week

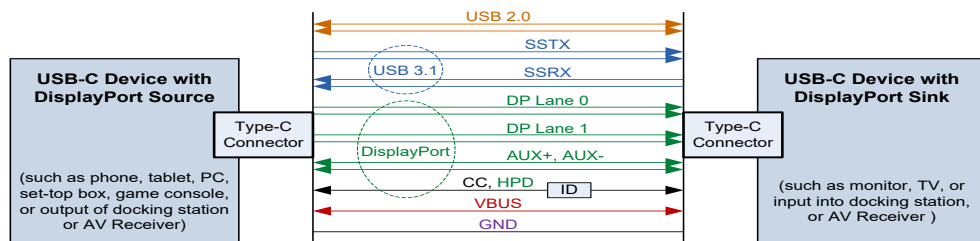
- Major PC OEMs continue to launch new products with DP Alt Mode over USB-C
- Major Display OEMs continue to add USB-C inputs to their products

USB-C Connector Functional Extension DP Alt Mode



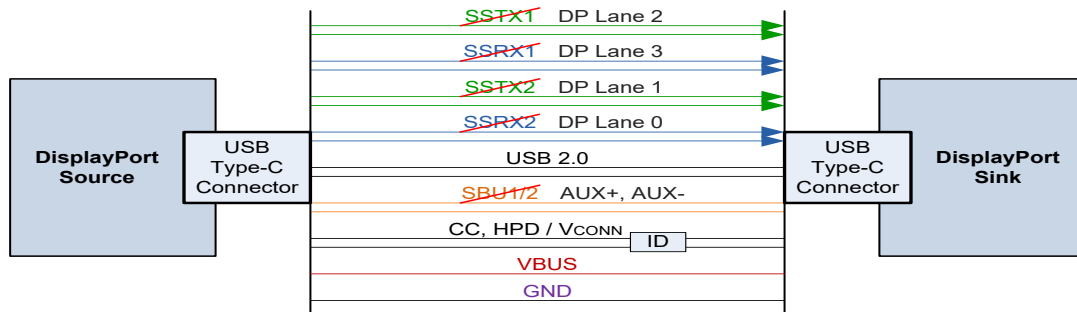
- A passive Full Feature USB Type-C to Type-C cable can carry up to four DisplayPort lanes
 - Same performance and features as a standard DisplayPort connection
 - Allows DisplayPort data rates to increase in the future, since the USB Type-C connector has very high data rate capability
- DisplayPort can be combined with USB 3.2 operation over the same USB Type-C cable
- USB 2.0 and USB Power Delivery is available in all configurations

2xDisplayPort and USB 3.2 over a Standard USB-C Cable



- Uses a standard “Full Feature” USB-C to USB-C cable which is designed to include DisplayPort
- The above configuration uses two high-speed lanes each for DisplayPort and USB 3.2
 - Ideal for docking stations, or for displays or TVs that include USB 3.2 functions
- DisplayPort performance provided by two lanes
 - HBR3: 4K(3840x2160)@60fps 24bpp
 - UHBR20: 8K (7680x4320)@30fps 30bpp

4xDP Over a USB Type-C to USB Type-C Full Feature Passive Cable



- Utilizes optional DP Alt Mode capability of USB Type-C connector
- DisplayPort can use all four high speed lanes to deliver full DisplayPort performance
- The DisplayPort AUX Channel uses the SBU pins
- The DisplayPort HPD / IRQ is transmitted over the CC pin using the USB-PD protocol
- USB 2.0 and USB Power Delivery always available
- DisplayPort performance provided by four lanes
 - HBR3: 5K (5120x2800)@60fps 24bpp
 - UHBR20: 10K (10240x4320)@60fps 24bpp

Typical DisplayPort Alternate Mode Flow

Untitled.crtl - Ellisys Type-C Tracker Analyzer

File View Layout Search Record Tools Help

Record Stop Restart Navigate Markers

USB PD Overview

Grouping 120 items displayed

Item	Bit Rate	Direct...	S.
SOP' Discover Identity (x 4)	296.718 kbit/s	OUT	OK
Source Capabilities (1=Fixed 5V 1.5A)	296.63 kbit/s, 3...	OUT	OK
Request (1=Fixed 5V 1.5A, Requested 1.5A, Max 1.5A) > Accepted	300.553 kbit/s, ...	IN	OK
PsRdy	296.674 kbit/s, ...	OUT	OK
DisplayPort Discover Modes > Ack (UFP_D Capable, CD)	296.63 kbit/s, 3...	OUT	OK
DisplayPort Discover Modes	296.63 kbit/s, 3...	OUT	OK
DisplayPort Discover Modes Ack (UFP_D Capable, CD)	300.553 kbit/s, ...	IN	OK
Apple Discover Modes > Ack (0x00000002, 0x00000001)	296.63 kbit/s, 3...	OUT	OK
Apple Discover Modes	296.63 kbit/s, 3...	OUT	OK
Apple Discover Modes Ack (0x00000002, 0x00000001)	300.481 kbit/s, ...	IN	OK
DisplayPort Enter Mode (Mode=1) > Ack	296.648 kbit/s, ...	OUT	OK
DisplayPort Enter Mode (Mode=1)	296.648 kbit/s, ...	OUT	OK
DisplayPort Enter Mode Ack	300.598 kbit/s, ...	IN	OK
DisplayPort Status Update (DFP_D connected, Not Enabled) > Ack (UFP_D connected, Enabled, HPD Low)	296.648 kbit/s, ...	OUT	OK
DisplayPort Status Update (DFP_D connected, Not Enabled)	296.648 kbit/s, ...	OUT	OK
DisplayPort Status Update Ack (UFP_D connected, Enabled, HPD Low)	300.553 kbit/s, ...	IN	OK
DisplayPort Configure (Set Config as DP Sink, D) > Ack	296.648 kbit/s, ...	OUT	OK
DisplayPort Configure (Set Config as DP Sink, D)	296.648 kbit/s, ...	OUT	OK
DisplayPort Configure Ack	300.418 kbit/s, ...	IN	OK

DisplayPort Alternate Mode 2.1 Update

- **SVDM Header Update (by USB PD Spec)**
- **Cable DP Capabilities VDO update to support UHBR20 and UHBR13.5**
 - Both passive and active cables
- **SOP' Active Cable DisplayPort Configurations VDO update**
- **DP Capabilities VDO Update (DPAM Version field)**
- **SOP DisplayPort Configurations VDO Update**
 - Cable information
 - DPAM Version
- **DisplayPort Status Update VDO Update**

SVDM Header Update

12:11	Structured VDM Version (Minor)^a	Version number (Minor) of the SVDM (not the <i>USB PD</i> version number). 00b = Version 2.0 or earlier 01b = Version 2.1 All other values are RESERVED.
14:13	Structured VDM Version (Major)^a	Version number (Major) of the SVDM (not the <i>USB PD</i> version number). 00b = Version 2.0 or earlier. 01b = Version 2.x. (x indicates SVDM minor version) All other values are RESERVED.

12:11 was reserved

Cable DP Capabilities VDO update

Table 4-5: SOP' Cable DP Capabilities (VDO in the Responder USB PD Discover Modes VDM)^a

Bit(s)	Description	Values
1:0	RESERVED	RESERVED (always 00b).
5:2	Signaling for Transport of DisplayPort Protocol ^b	XXX1b = Supports all defined <i>DP</i> bit rates up to HBR3. XX1Xb = Supports <i>DP</i> bit rate UHBR10. X1XXb = Supports <i>DP</i> bit rate of UHBR20 (e.g., 0111b supports all <i>DP</i> bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates. ^c
7:6	RESERVED	RESERVED (always 00b).
15:8	DP Source Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported. 10h = <i>USB-C</i> and <i>DP</i> connector Pin Assignment E is supported. All other values are RESERVED.
23:16	DP Sink Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10h = <i>USB-C</i> and <i>DP</i> connector Pin Assignment E is supported. All other values are RESERVED.
25:24	RESERVED	RESERVED (always 00b).
26 ^d	UHBR13.5	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported. ^c
27	RESERVED	RESERVED (always 0).
29:28 ^d	Active Component	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30	DPAM Version	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 4-2: Active Cable DP Capabilities (VDO in the Responder USB PD Discover Modes VDM)

Bit(s)	Description	Values
1:0	RESERVED	RESERVED (always 00b).
5:2	Signaling for Transport of DisplayPort Protocol ^a	XXX1b = Supports <i>DP</i> bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	DP Source Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported. All other values are RESERVED.
23:16	DP Sink Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). All other values are RESERVED.
31:24	RESERVED	RESERVED (always 00h).

a. "X" value indicates "Don't Care."

Active Cable DisplayPort Configurations VDO update

Table 4-7: SOP' Active Cable DisplayPort Configurations

Bit(s)	Description	Values
1:0	Select Configuration	00b = Set configuration for <i>USB</i> . ^a 01b = Set configuration for active cable as a <i>DP</i> Source device (UFP_U is a <i>DP</i> Source device). ^b 10b = Set configuration for active cable as a <i>DP</i> Sink device (UFP_U is a <i>DP</i> Sink device). ^b 11b = RESERVED.
5:2	Signaling for Transport of DisplayPort Protocol	0h = Bit rate is unspecified (used only when the <i>Select Configuration</i> field is programmed for USB Configuration). 1h = Select <i>DP</i> bit rates and electrical settings. All other values are RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	Configure Active Cable Pin Assignment	00h = Deselect pin assignment. 04h = Select Pin Assignment C. ^c 08h = Select Pin Assignment D. ^d 10h = Select Pin Assignment E. ^e All other values are RESERVED.
31:16	RESERVED	RESERVED (always 0000h).

Table 4-4: Active Cable DisplayPort Configurations

Bit(s)	Description	Values
1:0	Select Configuration	00b = Set configuration for <i>USB</i> . ^a 01b = Set configuration for active cable as a <i>DP</i> Source device (UFP_U is a <i>DP</i> Source device). ^b 10b = Set configuration for active cable as a <i>DP</i> Sink device (UFP_U is a <i>DP</i> Sink device). ^b 11b = RESERVED.
5:2	Signaling for Transport of DisplayPort Protocol	0h = Bit rate is unspecified (used only when the <i>Select Configuration</i> field is programmed for USB Configuration). 1h = Select <i>DP</i> bit rates and electrical settings. All other values are RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	Configure Active Cable Pin Assignment	00h = De-select pin assignment. 04h = Select Pin Assignment C. ^c 08h = Select Pin Assignment D. ^d All other values are RESERVED.
31:16	RESERVED	RESERVED (always 0000h).

No Pin Assignment E

DP Capabilities VDO Update

Table 5-6: DP Capabilities (VDO in the Responder USB PD Discover Modes VDM)

Bit(s)	Description	Values ^a
1:0	Port Capability	00b = RESERVED. 01b = <i>DP</i> Sink Device Capable (including <i>DP</i> Branch device). 10b = <i>DP</i> Source Device Capable (including <i>DP</i> Branch device). 11b = Both <i>DP</i> Source and Sink Device Capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports <i>DP</i> bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = <i>DP</i> interface is presented on a <i>USB-C</i> plug. 1 = <i>DP</i> interface is presented on a <i>USB-C</i> receptacle.
7	USB 2.0 Signaling Not Used	0 = <i>USB 2.0</i> may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = <i>USB 2.0</i> is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)	0000000b = <i>DP</i> Source device pin assignments are not supported. XXXXXXXX1b = RESERVED. XXXXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported. ^b XXXXX1XXXb = Pin Assignment D is supported. ^{c d} XXX1XXXXb = Pin Assignment E is supported. ^e XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	0000000b = <i>DP</i> Sink device pin assignments are not supported. XXXXXXXX1b = RESERVED. XXXXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported. ^f XXXXX1XXXb = Pin Assignment D is supported. ^{c g} XXX1XXXXb = Pin Assignment E is supported. ^h XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
29:24	RESERVED	RESERVED (always 00h).
31:30	DPAM Version ⁱ	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 5-5: DP Capabilities (VDO in the Responder USB PD Discover Modes VDM)

Bit(s)	Description	Values ^a
1:0	Port Capability	00b = RESERVED. 01b = <i>DP</i> Sink device-capable (including <i>DP</i> Branch device). 10b = <i>DP</i> Source device-capable (including <i>DP</i> Branch device). 11b = Both <i>DP</i> Source and Sink device-capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports <i>DP</i> bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = <i>DP</i> interface is presented on a <i>USB-C</i> plug. 1 = <i>DP</i> interface is presented on a <i>USB-C</i> receptacle.
7	USB 2.0 Signaling Not Used	0 = <i>USB 2.0</i> may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = <i>USB 2.0</i> is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)	0000000b = <i>DP</i> Source device pin assignments are not supported. XXXXXXXX1b = RESERVED. XXXXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported. ^b XXXXX1XXXb = Pin Assignment D is supported. ^{c d} XXX1XXXXb = Pin Assignment E is supported. ^e XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	0000000b = <i>DP</i> Sink device pin assignments are not supported. XXXXXXXX1b = RESERVED. XXXXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported. ^f XXXXX1XXXb = Pin Assignment D is supported. ^{c g} XXX1XXXXb = Pin Assignment E is supported. ^h XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
31:24	RESERVED	RESERVED (always 00h).

If *SVDM* Version is 2.1 or higher, *DPAM* Version field is applicable else this field shall be set to 00b.

A Bit More Background

From DisplayPort Alt Mode 2.0 Spec

Future versions of this Standard may describe other modes associated with the DP_SID. Such modes shall be identified by having a non-zero value in bits 31:24 of the VDO. The DFP_U shall examine the list of modes returned until it finds 0s in bits 31:24 of the VDO and a non-zero value in bits 23:0 of the VDO (i.e., DP Capabilities). The DFP_U and UFP_U shall use the corresponding offset (indexed from 1) as the Object Position in the following commands:

SOP DisplayPort Configurations VDO Update

Table 5-13: SOP DisplayPort Configurations

Bit(s)	Description	Values
1:0	Select Configuration	00b = Set configuration for USB . ^a 01b = Set configuration for UFP_U as a DP Source device. ^b 10b = Set configuration for UFP_U as a DP Sink device. ^b 11b = RESERVED.
5:2 ^c	Signaling for Cable Information Transport of DisplayPort Protocol	XXX1b = Supports all defined DP bit rates up to HBR3 -or- capability is unknown XX1Xb = Supports DP bit rate UHBR10. X1XXb = Supports DP bit rate of UHBR20 (e.g., 0111b supports all DP bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates. ^d
7:6	RESERVED	RESERVED (always 00b).
15:8	Configure UFP_U Pin Assignment	00h = Deselect pin assignment. 04h = Select Pin Assignment C. ^e 08h = Select Pin Assignment D. ^f 10h = Select Pin Assignment E. ^g All other values are RESERVED.
25:16	RESERVED	RESERVED (always 000000000b).
26 ^h	Cable UHBR13.5 Support	0 = Not supported. ¹ -or- capability is unknown 1 = Supported.
27	RESERVED	RESERVED (always 0).
29:28 ^h	Cable Active Component	00b = Passive -or- cable type is unknown 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30 ^j	DPAM Version	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 5-8: DisplayPort Configurations

Bit(s)	Description	Values
1:0	Select Configuration	00b = Set configuration for USB . ^a 01b = Set configuration for UFP_U as a DP Source device. ^b 10b = Set configuration for UFP_U as a DP Sink device. ^b 11b = RESERVED.
5:2	Signaling for Transport of DisplayPort Protocol	0h = Bit rate is unspecified (used only when the Select Configuration field is programmed for USB Configuration). 1h = Select DP bit rates and electrical settings. All other values are RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	Configure UFP_U Pin Assignment	00h = De-select pin assignment. 04h = Select Pin Assignment C. ^c 08h = Select Pin Assignment D. ^d 10h = Select Pin Assignment E. ^e All other values are RESERVED.
31:16	RESERVED	RESERVED (always 0000h).

- This is the most challenging part for DPAM 2.1 DFP_U

DisplayPort Status Update VDO Update

Table 5-7: DisplayPort Status Update

Bit(s)	Description	Values
1:0	DP Source/Sink Device Connected	00b = Neither a <i>DP</i> Source device nor <i>DP</i> Sink device is connected, –or– the adapter is disabled. 01b = <i>DP</i> Source device is connected. 10b = <i>DP</i> Sink device is connected. ^a 11b = Both a <i>DP</i> Source and Sink device are connected.
2 ^b	Power Low	0 = Adapter is not in low power state is functioning normally or is disabled . 1 = Adapter has detected low power and disabled DP support .
3 ^b	Enabled	0 = Adapter <i>DP</i> functionality is disabled. 1 = Adapter <i>DP</i> functionality is enabled and operational.
4 ^d	Multifunction Preferred	0 = No preference for multifunction. 1 = Multifunction is preferred.
5 ^c	DisplayPort/USB Configuration Request	0 = Request change to DisplayPort Configuration (if currently in USB Configuration). 1 = Request change to USB Configuration (if currently in DisplayPort Configuration).
6 ^c	Exit DisplayPort Alt Mode Request	0 = Maintain the current mode. 1 = Request exit from DisplayPort Alt Mode (if currently in DisplayPort Alt Mode).
7 ^d	HPD State	0 = HPD_Low. 1 = HPD_High. ^e
8 ^d	IRQ_HPD	0 = IRQ_HPD has not been issued since the last status Message. 1 = IRQ_HPD. ^f
9 ^g	NO_DPAM_SUSP END	0 = UFP_U/ DP Sink device has no preference for entry into low power state. 1 = UFP_U/ DP Sink device prefers not to enter low power state.
31:10	RESERVED	RESERVED (always 0000000h).

Table 5-6: DisplayPort Status Update

Bit(s)	Description	Values
1:0	DP Source/Sink Device Connected	00b = Neither a <i>DP</i> Source device nor <i>DP</i> Sink device is connected, –or– the adapter is disabled. 01b = <i>DP</i> Source device is connected. 10b = <i>DP</i> Sink device is connected. ^a 11b = Both a <i>DP</i> Source and Sink device are connected.
2 ^b	Power Low	0 = Adapter is functioning normally or is disabled. 1 = Adapter has detected low power and disabled <i>DP</i> support.
3 ^b	Enabled	0 = Adapter <i>DP</i> functionality is disabled. 1 = Adapter <i>DP</i> functionality is enabled and operational.
4 ^b	Multi-function Preferred	0 = No preference for multi-function. 1 = Multi-function is preferred.
5 ^b	DisplayPort/USB Configuration Request	0 = Request change to DisplayPort Configuration (if currently in USB Configuration). 1 = Request change to USB Configuration (if currently in DisplayPort Configuration).
6 ^b	Exit DisplayPort Alt Mode Request	0 = Maintain the current mode. 1 = Request exit from DisplayPort Alt Mode (if currently in DisplayPort Alt Mode).
7 ^c	HPD State	0 = HPD_Low. 1 = HPD_High. ^d
8 ^c	IRQ_HPD	0 = IRQ_HPD has not been issued since the last status Message. 1 = IRQ_HPD. ^e
31:9	RESERVED	RESERVED (always 0000000h).

DPAM Version Resolution

Table 5-5: DPAM Version Resolution

DFP_U, Cable and UFP_U with DP SID	DFP_U	Cable	UFP_U	DPAM Version Resolution
DPAM Version	2.0 or earlier	2.0 or earlier	2.0 or earlier	2.0 or earlier ^{ab}
	2.1 or higher	2.0 or earlier	2.0 or earlier	2.0 or earlier ^{ab}
	2.0 or earlier	2.1 or higher	2.0 or earlier	2.0 or earlier ^{ab}
	2.0 or earlier	2.0 or earlier	2.1 or higher	2.0 or earlier ^{ab}
	2.1 or higher	2.1 or higher	2.0 or earlier	2.0 or earlier ^{ab}
	2.0 or earlier	2.1 or higher	2.1 or higher	2.0 or earlier ^{ab}
	2.1 or higher	2.0 or earlier	2.1 or higher	DPAM 2.1 or higher ^c
	2.1 or higher	2.1 or higher	2.1 or higher	2.1 or higher ^d (Shall support DPAM 2.1 or higher)

- If Initiator and Responder support SVDM Version 2.0 or earlier and if DisplayPort Alternate Mode is supported all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.0 or earlier.
- If Initiator and Responder both support SVDM Version 2.1 or higher and if either Initiator or Responder supports DPAM Version 2.0 or earlier, then all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.0 or earlier.
- When DPAM 2.1 or higher DFP_U and DPAM 2.1 or higher UFP_U are connected with a legacy active DPAM 2.0 cable, then the system shall exchange all DP Capabilities as per DisplayPort Alt Mode on USB Type-C specification 2.1 or higher but support HBR3 rates.
- If Initiator and Responder both support SVDM Version 2.1 or higher and DPAM Version 2.1 all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.1 or higher.

Typical DPAM 2.1 Flow

USB PD Overview		
USB 2.0 Overview USB 3.x Overview		
Grouping ▾ 32 items displayed		
Item	Structured VDM Version	
⊕ SOP' Discover Identity > Ack (Type-C to Type-C 3A)	Version 2.1	
⊕ Source Capabilities (1=Fixed 5V 0.5A)		
⊕ Request (1=Fixed 5V 0.5A, Requested 0.5A, Max 0.5A) > Accepted		
⊕ PsRdy		
⊕ Discover Identity > Ack (PDUSB Peripheral, PDUSB Host)	Version 2.1	
⊖ Discover SVIDs > Ack (DisplayPort)	Version 2.1	
⊕ Discover SVIDs	Version 2.1	
⊕ Discover SVIDs Ack (DisplayPort)	Version 2.1	
⊕ DisplayPort Discover Modes > Ack (UFP_D Capable, CDE)	Version 2.1	
⊕ SOP' Discover SVIDs > Ack (Intel, DisplayPort)	Version 2.1	
⊖ SOP' DisplayPort Discover Modes > Ack (DFP_D=CD, UFP_D=CD)	Version 2.1	
⊕ SOP' DisplayPort Discover Modes	Version 2.1	
⊕ SOP' DisplayPort Discover Modes Ack (DFP_D=CD, UFP_D=CD)	Version 2.1	
⊖ SOP' Intel Discover Modes > Ack (Thunderbolt Cable, No retimer, 20Gb/s)	Version 2.1	
⊕ SOP' Intel Discover Modes	Version 2.1	
⊕ SOP' Intel Discover Modes Ack (Thunderbolt Cable, No retimer, 20Gb/s)	Version 2.1	
⊖ SOP' DisplayPort Enter Mode (Mode=1) > Ack	Version 2.1	
⊕ SOP' DisplayPort Enter Mode (Mode=1)	Version 2.1	
⊕ SOP' DisplayPort Enter Mode Ack	Version 2.1	
⊖ DisplayPort Enter Mode (Mode=1) > Ack	Version 2.1	
⊕ DisplayPort Enter Mode (Mode=1)	Version 2.1	
⊕ DisplayPort Enter Mode Ack	Version 2.1	
⊖ DisplayPort Status Update (DFP_D connected, Not Enabled) > Ack (UFP_D connected, Not Enabled, HPD High)	Version 2.1	
⊕ DisplayPort Status Update (DFP_D connected, Not Enabled)	Version 2.1	
⊕ DisplayPort Status Update Ack (UFP_D connected, Not Enabled, HPD High)	Version 2.1	
⊖ SOP' DisplayPort Configure (Set Config as DP Sink, C) > Ack	Version 2.1	
⊕ SOP' DisplayPort Configure (Set Config as DP Sink, C)	Version 2.1	
⊕ SOP' DisplayPort Configure Ack	Version 2.1	
⊖ DisplayPort Configure (Set Config as DP Sink, C) > No Response	Version 2.1	
⊕ DisplayPort Configure (Set Config as DP Sink, C)	Version 2.1	

DisplayPort Alternate Mode 2.1a Update

- **DisplayPort Alt Mode v2.1a_SCR_on_Clarification on Device Types**
- **DisplayPort Alt Mode v2.1a_SCR_on_CableSupport**
- **DisplayPort Alt Mode v2.1a_SCR_on_Deprecating DP40 Cables**
- **DisplayPort Alt Mode v2.1a_SCR_on_tAttentionToDPConfigure time**
- **DisplayPort Alt Mode v2.1a_SCR_on_mandatory PD Message support for DPAM2.1 Cables**

DisplayPort Alt Mode v2.1a_SCR_on_Clarification on Device Types

Table 5-1 USB-C and USB PD Power and Data Roles

<u>12</u>	<u>USB-C-to-DP receptacle</u>	<u>V_{CONN}-powered accessory (Rd/Ra)</u>	<u>No</u>	<u>DFP_U and UFP_U</u>	<u>No Preference</u>	<u>Never VCONN Source</u>
<u>13</u>	<u>USB-C-to-DP cable adapter</u>	<u>V_{CONN}-powered accessory (Rd/Ra)</u>	<u>No</u>	<u>DFP_U and UFP_U</u>	<u>No Preference</u>	<u>Never VCONN Source</u>

Table 5-2 USB PD Data Role Policies

Prefer UFP_U	<u>Issue a <i>USB PD DR_Swap</i> Message to become a UFP_U</u> <u>If the <i>USB PD DR_Swap</i> Message is rejected, and port results in a DFP_U role, the port shall be responsible for discovering and initiating Alternate Mode entry</u>	
--------------	--	--

DisplayPort Alt Mode v2.1a_SCR_on_CableSupport

Table 5-15: DP Rates for TBTSID Capable cables

Cable Type	SVDM Version	DPAM Version	DP SID	TBT SID	TBT Alt Mode Response (see Appendix F of USB-C specification)			DP Alt Mode Response (see Table 4-5)	SOP DP Configure (see Table 5-13)	
					B25	B22	B[18:6]		B[5:2]	B[29:28]
2,3 (See Table 2-1)	2.0	NA	No	Yes	0	0 Not Re-timer	001b, 010b or 011b	NA	001b or 010b = UHBR10 011b = UHBR20	00b
4 (See Table 2-2)	2.0	NA	No	Yes	Don't care	1 Re-timer		NA	No DP	NA

*Note: If cable supports both DPSID and TBTSID, TBT VDO Bit 22 and Bit 25 **can** be used by the DP Source to determine the cable type (Passive, Re-driven, or Re-timed).*

DisplayPort Alt Mode v2.1a_SCR_on_Deprecating DP40 Cables

Reference Number in Tables 2-4	Cable Type	Minimum DP Bit-rate Capability ^a	DisplayPort Alt Mode Directionality and Main-Link Lane-count Capability ^a	Certification and Logo Applicability
1	Full-Featured Passive <i>USB-C USB 3.2</i> Gen 1 Cables (<i>USB-C</i> CC3G1-X)	HBR3 ^b UHBR10 ^b	Reversible 4 Lanes	<i>USB</i> certification and logo only
2	Full-Featured Passive <i>USB-C USB 3.2</i> and <i>USB4</i> Gen 2 Cables and Thunderbolt Alt Mode Gen 2 Cables (<i>USB-C</i> CC3G2-X)	UHBR10 (<i>DP54</i>) UHBR13.5 ^d (<i>DP54</i>)		No VESA certification or logo
3	Full-Featured Passive <i>USB-C USB4</i> Gen 3 (or higher) Cables and Thunderbolt Alt Mode Gen 3 (or higher) Cables (<i>USB-C</i> CC4G3-X)	UHBR20 ^e (<i>DP80</i>)		

DisplayPort Alt Mode

v2.1a_SCR_on_tAttentionToDPConfigure time

1. Table 1-5 Glossary

Term	Definition
<u>tAttentionToDPConfigure</u>	<u>Time between reception of USB PD Attention to transmission of DisplayPort Configure Message, this time is set to 500 ms. This time is applicable to DFPs in active state and functioning normally.</u>

- Port is a DFP_U in DisplayPort Alt Mode and DisplayPort Configuration** – Port shall change to USB Configuration by issuing an appropriate *DisplayPort Configure* Command to both the UFP_U and cable within tAttentionToDPConfigure time after receiving a *USB PD Attention* Command request with the *DisplayPort/USB Configuration Request* bit (bit 5) set to 1 in the *DisplayPort Status Update* (refer Table 5-7)
- Port is a DFP_U in DisplayPort Alt Mode and USB Configuration** – Port shall change to an appropriate DisplayPort Configuration by issuing an appropriate *DisplayPort Configure* Command to both the UFP_U and cable within tAttentionToDPConfigure time after receiving a *USB PD Attention* Command request with the *DisplayPort/USB Configuration Request* bit cleared to 0 (refer Table 5-7)

DisplayPort Alt Mode v2.1a_SCR on mandatory PD Message support for DPAM2.1 Cables

Table 4-1: Cable eMarking Mandates

Reference Number in Tables 2-4	Cable Type	<i>USB PD Discover Identity</i>	DisplayPort Alt Mode <i>USB PD Commands</i>
1	Full-Featured Passive <i>USB-C USB 3.2</i> Gen 1 Cables (<i>USB-C CC3G1-X</i>)	Mandatory	Not Allowed
6	Captive Cable with <i>USB-C</i> connector	Mandatory When the DP Sink supports UHBR rates	Optional When the DP Sink supports HBR rates

DPAM 2.1 CTS Update - 1

- 🔖 10.3.2 DPAM2.1 Entry with USB-C to USB-C non-emarked cable
- 🔖 10.3.3 DPAM2.1 Entry with USB-C to USB-C Passive TBT3 cable
- 🔖 10.3.4 DPAM2.1 Entry with Passive E-Marked USB-C to USB-C
- 🔖 10.3.5 DPAM2.1 Entry with USB-C to USB-C DP2.0 LRD Cable
- 🔖 10.3.6 DPAM2.1 Entry with USB-C to USB-C DP2.0 Active Retimer cable
- 🔖 10.3.7 DPAM2.1 Entry with USB-C to USB-C DP2.1 LRD cable
- 🔖 10.3.8 DPAM2.1 Entry with USB-C to USB-C Active Non-DP cable
- 🔖 10.3.9 DPAM2.1 Entry with USB-C to USB-C USB2.0 cable
- 🔖 10.3.10 DPAM2.1 Entry with USB-C to DP2.1 cable

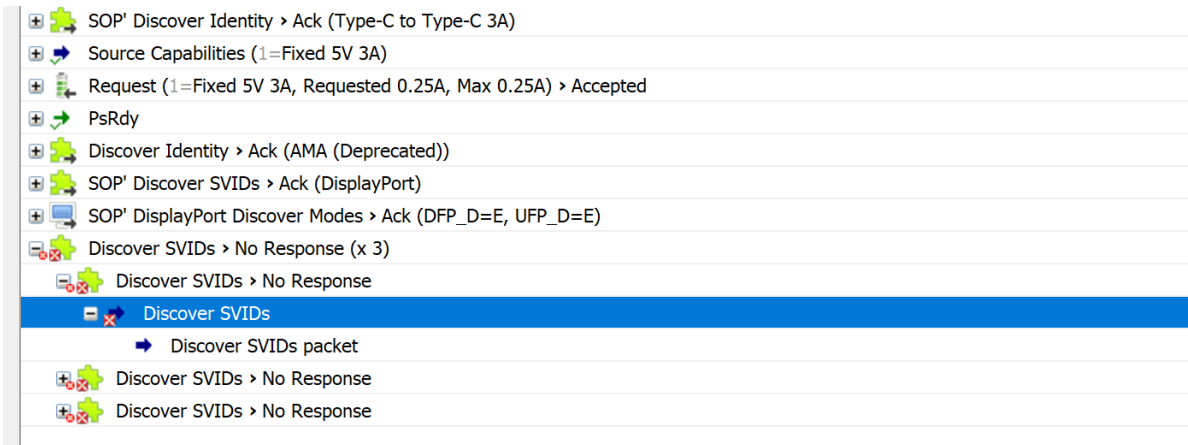
- Make sure the DFP_U set correct cable information in DisplayPort Configurations VDO
- 10.3.5 and 10.3.6 Using TBT info is now optional (was mandatory)

DPAM 2.1 CTS Update - 2

- **DPAM Version Resolution Tests**

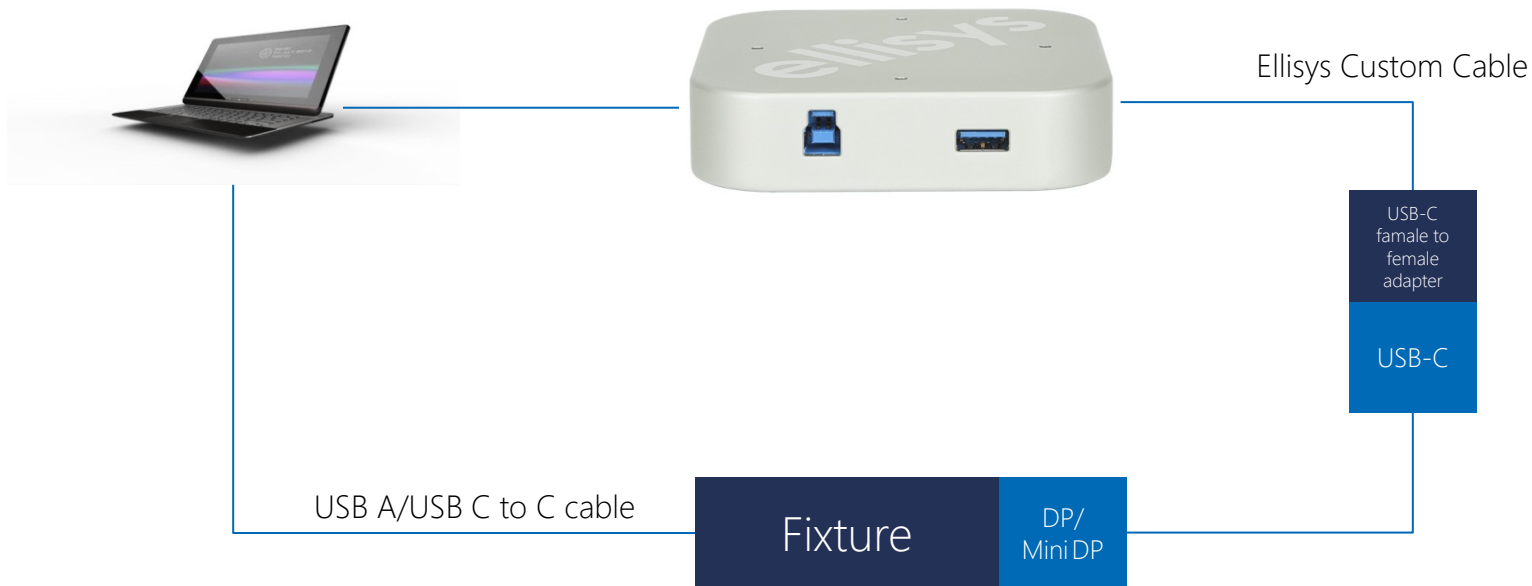
- **10.3.23 DPAM Version 2.1 DFP_U Connected to DPAM Version 2.0 or 2.1 UFP_U**
- **10.4.3 DPAM Version 2.1 Cable Connected to DPAM Version 2.0 or 2.1 DFP_U**
- **10.2.8 DPAM Version 2.1 UFP_U Connected to DPAM Version 2.0 or 2.1 DFP_U**

- **10.2.9 DPAM Discovery Interoperability Flow for UFPs**



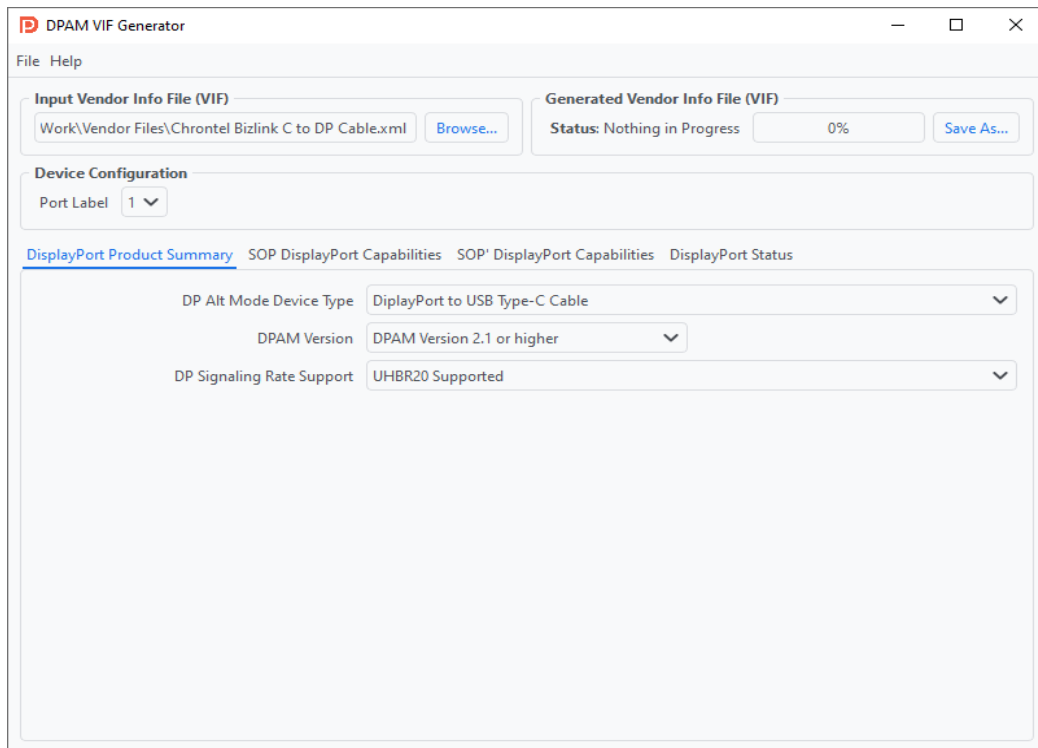
DPAM 2.1 CTS Update - 3

- C to DP Adapter tests automation



DPAM 2.1 CTS Update - 4

- **VESA VIF TOOL**



The screenshot shows the DPAM VIF Generator application window. It has a menu bar with 'File' and 'Help'. The main interface is divided into several sections:

- Input Vendor Info File (VIF):** Contains a text box with the path 'Work\Vendor Files\Chrontel Bizlink C to DP Cable.xml' and a 'Browse...' button.
- Generated Vendor Info File (VIF):** Contains a 'Status: Nothing in Progress' label, a progress indicator at '0%', and a 'Save As...' button.
- Device Configuration:** Contains a 'Port Label' dropdown menu currently set to '1'.
- Navigation Tabs:** A row of tabs including 'DisplayPort Product Summary' (which is selected), 'SOP DisplayPort Capabilities', 'SOP* DisplayPort Capabilities', and 'DisplayPort Status'.
- Configuration Fields:** Below the tabs, there are three rows of configuration options, each with a label and a dropdown menu:
 - 'DP Alt Mode Device Type' is set to 'DisplayPort to USB Type-C Cable'.
 - 'DPAM Version' is set to 'DPAM Version 2.1 or higher'.
 - 'DP Signaling Rate Support' is set to 'UHBR20 Supported'.

Ellisys USB Test and Analysis Solutions

USB Explorer™ 350



Multi-function USB Type-C®, USB 3.2,
and Power Delivery Protocol Test Platform

VESA-Approved Tester for DisplayPort ALT Mode



Type-C Tracker™



Protocol and Electrical Analysis Tool
for USB Type-C® Standards

Includes DP AUX and DP ALT Support



DisplayPort Alternate Mode 2.1b Upcoming

- **C to DP cable shall support DFP role**
- **C to DP cable pin assignment mandatory (Pin E required, Pin C optional, Pin D forbidden)**
- **Cable Attributes update**
- **Data Role clarification (cannot rely on DR_Swap being successful)**
- **DP80LL Loss Budget Supported bit**

Questions?

DisplayPort over USB-C

The most advanced display connection now uses the most versatile connector.

Learn More

Go to www.displayport.org



Break

VESA Logos and Marketing Guidelines

VESA Membership Allows Use of VESA Logos

- When your product passes certification company can use VESA logo to show customers proof of quality

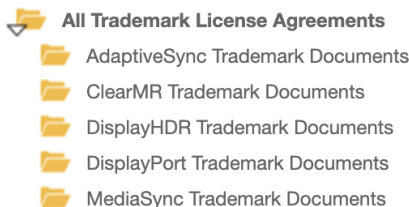
Cable Logos include:



DP Product Logos include:



Display Logos include:



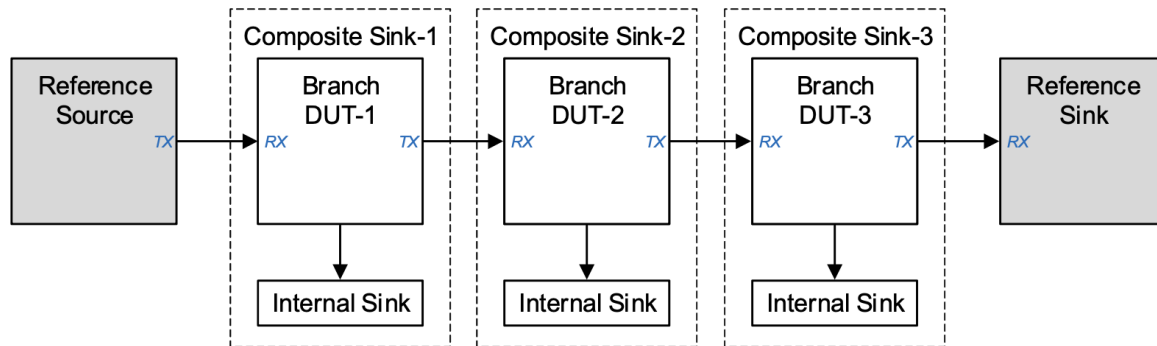
Compliance Testing

VESA PlugTest Events

- Provide significant value to VESA compliance program and member companies, particularly as new capabilities and products are deployed.
- Demonstrate and improve traditional interoperability
- Test Native DP and DP Alt Mode over USB Type-C™ products
 - UHBR rates, DSC, New MST Link Layer Tests, FEC, DisplayHDR and other new capabilities
 - Verify Test Equipment Correlation
- VESA hosted two successful PlugTests in 2024 (Taiwan and US)
- VESA hosts two PlugTests in 2025
 - South San Francisco, CA USA: **Q1 2025 (completed)**
 - Taipei, Taiwan: **Q4 2025 (Oct 20-23rd Taiwan)**

Multi-Stream Transport (MST) Compliance Testing Enhancements

- After over a year of specification and test equipment test development VESA is preparing to release its biggest MST test update since DP 1.2. With the introduction of UHBR20 + DSC, users can now daisy chain multiple 4K/120Hz displays from a single output connector
- The unique DP capability of driving multiple daisy chained displays with a single output connection/cable is increasingly the most popular feature of DP for end users
- To further improve end user experience with MST configurations, VESA's latest DP Link Layer Compliance Test Specification adds dozens of new MST source/sink tests to verify products are implemented according to DP specifications



DP 2.1a LL CTS Composite Sink (Daisy-chainable Sink) Setup 3

DP54, DP80 and DP80LL Cable Specifications and Certification program

- Work on Enhanced DP cable and connector specifications and test requirements started in 2021 to ensure high performance connectors and cables would be available for products supporting UHBR rates
- DP54 and DP80 Certified cables provide added assurance of proper operation at the highest link rates (UHBR10, UHBR13.5 and UHBR20 Gbps).
- DP80LL active LRD cable CTS and certification added to provide UHBR20 Gbps rate support for longer cables (can support ~3 meter cables)
 - Linear Redrivers (LRD) are level boosting amplifiers that boost signal transmission over longer distances
- Over 150 Enhanced DP cables and connectors have been certified since launch of the Enhanced DP cable and connector certification programs

Product certifications* 2023/2024/2025

Products	2023	2024	2025
DP Sources	99	93	136
DP Sinks	277	491	428
DP Cables	59	70	57
DisplayHDR	397	556	582
ClearMR	45	53	71
AdaptiveSync	80	75	113

*Note: Numbers are base model certs not including family models. Updates to Compliance Management System (CMS) will include feature to count family models in the future.

Summary

Summary

- Product shipments and certifications based on VESA technologies continue impressive growth
- DP 2.1 UHBR capable product development and certifications are in mass production
- VESA Enhanced cable and connector certification programs have been very successful with significant numbers of DP54, DP80 and now DP80LL cables certified
- DisplayPort over USB-C is a game changer for small form factor and portable products and is now the defacto standard for laptops, tablets and handheld devices
- MST continues to be a popular DP feature and with UHBR20 + DSC it can be used to drive multiple high resolutions displays at high refresh rates through a single connector
- Display Performance Standards adoption and certification have been extremely successful the last several years
- Development and adoption of new technologies continues to drive increases in VESA membership growth

THANK YOU

[DisplayPort.org](https://displayport.org)

[DisplayHDR.org](https://displayhdr.org)

[ClearMR.org](https://clearmr.org)

[AdaptiveSync.org](https://adaptivesync.org)

[VESA.org](https://vesa.org)

Questions?

Demo Tables

Teledyne LeCroy Test Solutions for DisplayPort v2.1



M42de 80G Video Analyzer/ Generator



Teledyne LeCroy
7F., No. 667, Bannan Rd
Zhonghe Dist, New Taipei City 235
Taiwan
Phone: +886-2-8228-6100

protocolsales@teledynelecroy.com

Teledyne LeCroy DisplayPort Test Platforms

■ Quantumdata M42de Analyzer / Generator

- DisplayPort 1.4 & 2.1 (UHBR) Lane Rates
- DP80 and USB Type-C[®] connectors
- Deep Capture / Analysis
- T.A.P.4[™] Passive Monitoring
- Comprehensive DP 1.4 & 2.1 Compliance Coverage
 - Link, DSC, LTTPR, EDID & MST
- qdPrime[™] Automated Test Suite

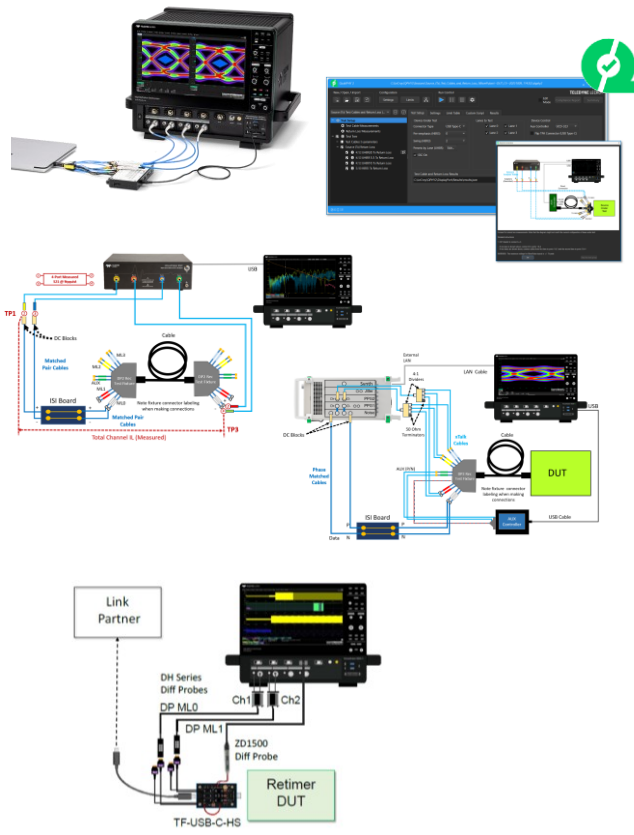


■ Quantumdata M21 Analyzer

- Portable DP Analyzer & HDMI Analyzer / Generator
- DisplayPort Source Testing only (up to UHBR 13.5Gb/s)
- AUX Channel Monitoring



DisplayPort 2.1 PHY Compliance and PHY-Logic Debug



- DisplayPort 2.1 Source (Tx) Compliance
 - WaveMaster/SDA 8000HD with QualiPHY® 2 software
 - SDAX-DP expert analysis – Find Best CTLE/DFE
 - Reduced test times with QPHY2-PC
 - Automated Return Loss with WavePulser 40iX
- DisplayPort 2.1 Sink (Rx) Compliance
 - WaveMaster/SDA 8000HD with QualiPHY 2 software
 - SSG Cal and BER testing using Anritsu MP1900 SQA
 - Automated Channel Cal with WavePulser 40iX
- PHY-Logic (Interop) Debug
 - AUX Triggered + Main Link capture
 - TF-USB-C-HS – probing access
 - DP-AUX, USB-PD TDMP software
 - Clock switch testing on live link



Unigraf DisplayPort and USB-C Test Solutions

UCD-500 Gen2



16K DP 2.1 Generator & Analyzer

- DP 2.1 Link Layer CTS Tool
- DP 2.1 Sinks and Sources up to 8K@60Hz (UHBR 20Gbps / Lane) and 16K@60Hz with DSC
- Featuring Link Analyzer, Panel Replay and eDP test functions

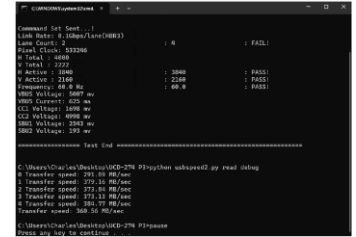


UTC-274



USB-C Test Automation Tool

- Test DP Alt Mode, Power Delivery and USB Speed
- Support EPR function up to 240W Source and Sink
- Test USB-C connector pins soldering and assembly quality with a single cable insertion





DisplayPort Alt Mode Compliance Testing and Analysis solutions

Ellisys USB/DPAM Test and Analysis Solutions

USB Explorer™ 350



Multi-function USB Type-C®, USB 3.2,
and Power Delivery Protocol Test Platform

VESA-Approved Tester for DisplayPort ALT Mode



Type-C Tracker™



Protocol and Electrical Analysis Tool
for USB Type-C® Standards

Includes DP AUX and DP ALT Support



GRL DisplayPort

DP2.1 Tx PHY Test Solution

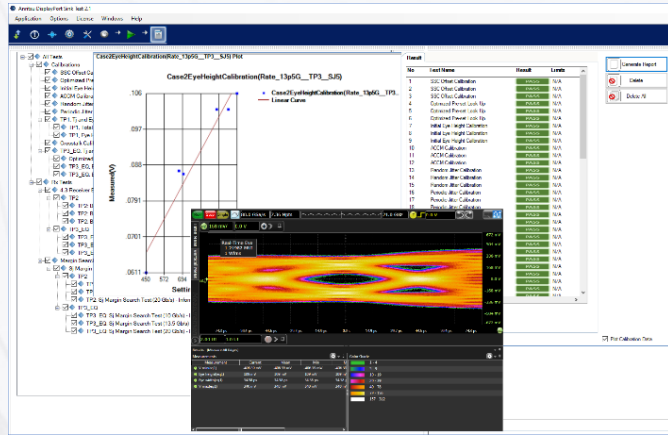
DP2.1 Rx PHY Test Solution

DPAM Test Solution



GRL Test Solution

DisplayPort 2.1 Tx/Rx Test Automation Solution



USB Type-C® Power Delivery Tester & Analyzer - EPR



- USB Power Delivery Specification 3.2
- Type-C® Functional Specification
- IEC Functional Safety (IEC 62368-1)
- **DisplayPort™ Alternate Mode Tests**
- Thunderbolt 3/4/5 Alternate Mode Tests
- Thunderbolt 3/4/5 Power Tests
- Qualcomm® Quick Charge 2™
- Qualcomm® Quick Charge 3™ and 3+™
- Qualcomm® Quick Charge 4™ and 4+™
- Qualcomm® Quick Charge 5™
- BC 1.2 for QC Sink products
- IEC 63680-1-2

The only instrument you need for validating compliance, interoperability, and reliability of your designs

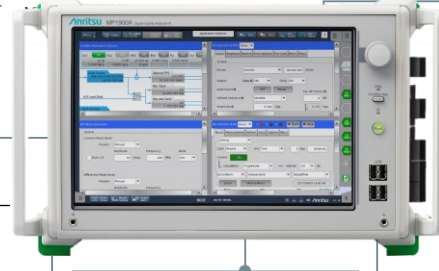


MP1900A Signal Quality Analyzer

High Speed Bus SINK Compliance Solution

MP1900A Standalone

Multi-channel BER Measurement
High-quality PPG
High-input-sensitivity ED
PAM3/4 BER Measurements



Thunderbolt
4/5&DP1.4/2.1 Rx Test
Stressed Signal Calibration and
Stressed Signal Input Test

USB Link Sequence Generation
Transition to Loopback mode

Jitter Tolerance Test
SJ/RJ/BUJ Injection
Low-rate estimated BER measurement

Stressed Signal Calibration
PCI Express Link Sequence Generation
Transition to Loopback Mode
Pass/Fail evaluation using BER measurement

Calibration of stressed signal*

Transition DUT state to Loopback

Stressed Receiver Testing

MX183000A Software

Stressed Signal Calibration*

USB Link Sequence Generation Function

PCI Express Link Sequence Generation Function

Stressed Signal Input Test Function

Jitter Tolerance Test

Auto-receiver Test Function

MP1800A Hardware

Up to 32 Gbit/s, 8ch

High Quality Signal

Jitter
Emphasis

MP1900A Signal Quality Analyzer

DP1.4/2.1 SINK Compliance Test Structure



MP1900A Standalone

- Multi-channel BER Measurement
- High-quality PPG
- High-input-sensitivity ED
- PAM3/4 BER Measurements
- DP1.4/2.1 and USB4v1&v2 Compliance test Support



Thank you for attending the
VESA Workshop
Seoul, Korea
2025