Welcome
VESA Workshop
Shenzhen, China
2025

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Time	Topic	Speaker
10:00am	VESA Overview and Standards Updates: DisplayPort v 2.1b, Display Panel Standards, and Automotive Extension Services	Jim Choate, VESA CPM
11:00am	DisplayPort Link Layer CTS v 2.1 MST Updates	Neal Kendall, Senior Staff Product Marketing Manager, Teledyne LeCroy
12:00pm	eDP and DP v 2.1 PHY CTS Overview and Updates	Zhi-Dong Tian, Keysight Technologies
12:30pm – 1:30pm	Lunch	-
1:30pm	DP Alt Mode v 2.1a Overview and CTS Updates	Tim Wei, Senior Application Engineer, Ellisys
2:00pm	DP v 2.1 Panel Replay and Advanced Link Power Management: Implementation and Testing Challenges	Marco Denicolai, Product Owner, IP Cores, Unigraf Oy
3:00pm	LRD/Active Cable Testing and DP 2.1 Enhanced Connector Certification	Lexus Lee, Technical Program Manager, Allion Labs
3:30pm – 3:45pm	Break	-
3:45pm	VESA Marketing: Logo Usage, Trademarks, and Resellers	Jim Choate, VESA CPM
4:05pm	VESA Compliance Program	Jim Choate, VESA CPM
4:25pm	Summary, Questions & Answers	Jim Choate, VESA CPM
4:45pm	Demo Stations Overview	

VESA Overview and Standards Updates

Jim Choate
VESA Compliance Program Manager
October 28, 2025

Agenda

- VESA Overview
- DisplayPort Overview
- VESA Certified DisplayHDR, ClearMR and Adaptive-Sync
- VESA Technology Development Areas
- Summary

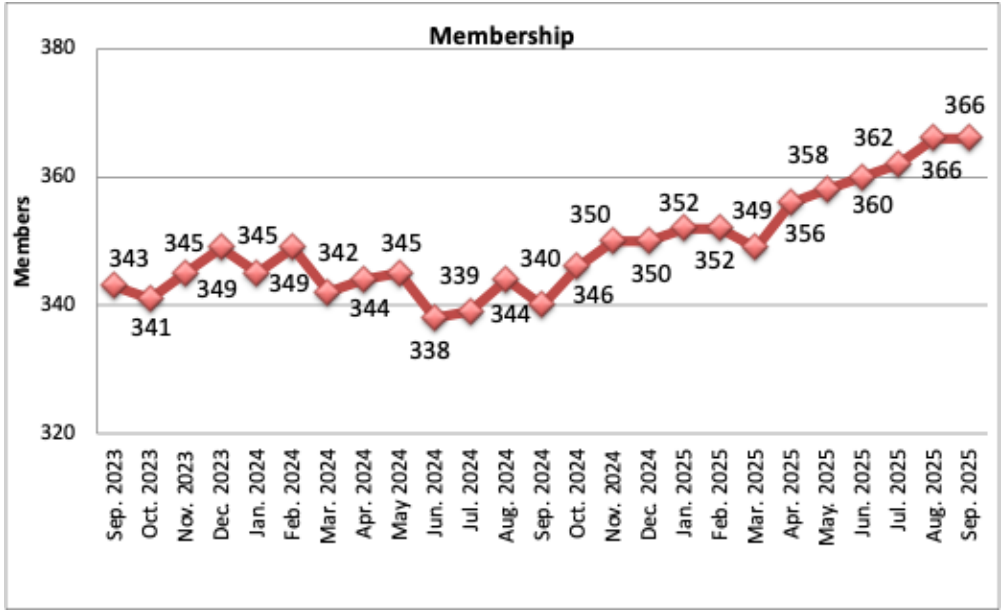
VESA OVERVIEW

VESA Vision

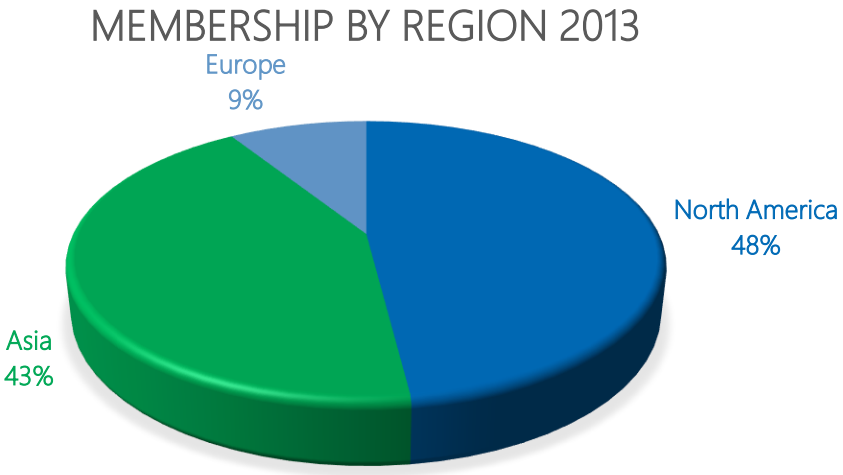
- VESA's vision is continual growth in technical standards development and evolution into an international trade association, with a worldwide membership driving standards initiatives, product implementations, and market implementation.

About VESA

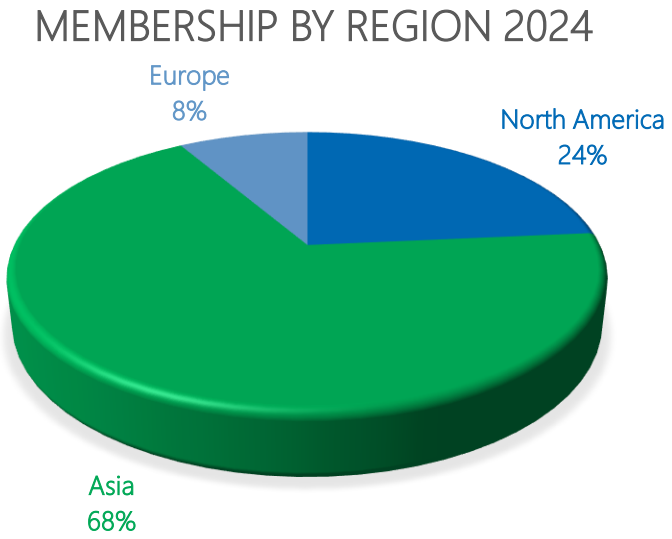
- A growing global industry alliance with 366 members. Strong growth in membership.
- Mission to develop, promote and support ecosystem of vendors and certified interoperable products for the electronics industry.
- *Develops OPEN standards, contribution is open to all companies at all stages of development*



VESA Membership Growth



Changes from 2013:
Asia + 25%
North America – 24%
Europe – 1%



VESA Standards Enable Many Market Segments…

Monitors, PCs and laptops

Gaming consoles and headsets

Smartphones and tablets

Automotive

NEW: VESA DP AE specification

Multi-Stream Transport (MST)

VESA Local Asian Support Capability

- VESA continues to provide local support to Asia to address growing regional membership needs
- **Kellen** is VESA's Representative in Asia
- This partnership provide members with a communication option in their native language. Kellen handles membership related activities including, new membership requests, renewals, event support and translation of VESA member messaging, etc.
- AsiaVESA@kellencompany.com or at +86 10 6580 0670

DisplayPort ™ Overview

DisplayPort Market Penetration

- DisplayPort adoption continues to grow in 2025
- DisplayPort and DisplayPort Alternate Mode over USB-C
  - The common monitor interface for personal computers
  - Supported on the USB-C interfaces
    - Mandated for USB4 and Thunderbolt
  - Automotive integration with DP AE specification
  - Mobile phones with USB-C
- Embedded DisplayPort (eDP)
  - ~95% penetration in notebook PCs, used in many high-end tablets and automotive

DisplayPort 2.1a Summary

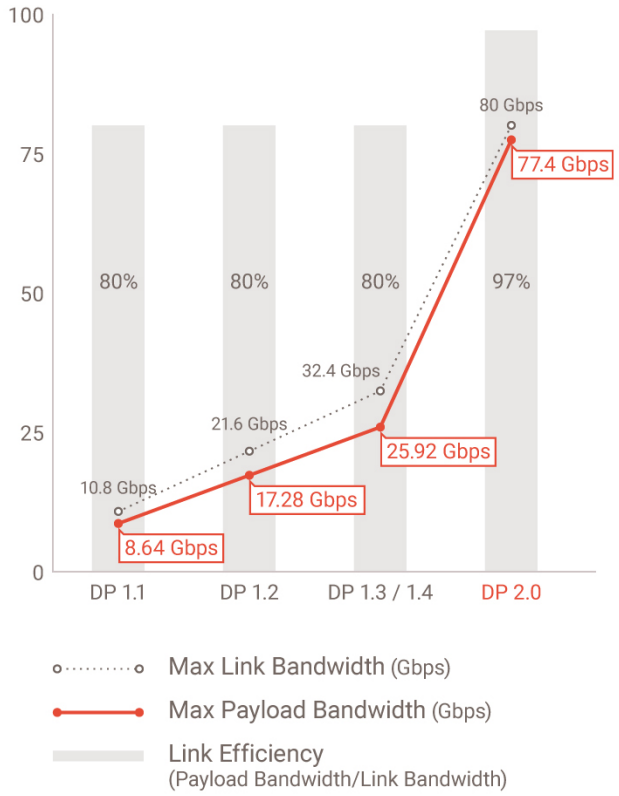
- DisplayPort v2.1a was released in December 2023
- Major features added in v2.0/v2.1/v2.1a/v2.1b:
  - Added 128b/132b DP channel coding
  - Increase in data bandwidth performance (almost 3X) with new link rates up to 20 Gbps/lane
  - Panel Replay, similar to PSR (Panel Self Refresh) used for eDP
  - DSC support mandated
  - Enhanced DP connectors and cables (DP54 and DP80)
  - DP PHY specification alignment with USB4 PHY specification
  - Updated DP to HDMI v2.1 or higher protocol converter (PCON)
  - Corrects errata
  - Replaces DP40 cables with DP54 to expand higher rate cable length
  - Expanded Tunneling capability
  - Updates for DP AE Services specification
  - DP80LL cable spec section
  - LRD Active Cable Electrical Mandate section

VESA

- DisplayPort 2.1a enables up to 3X increase in video bandwidth performance vs DP 1.4
- 3 new data rates added. UHBR10, UHBR13.5 and UHBR20 provides up to 80Gbps link bandwidth for 4 lanes at 20Gbps.
- First standard to support 8K resolution (7680 x 4320) at 60 Hz refresh rate with full-color 4:4:4 resolution, including with 30 bits per pixel (bpp) for HDR-10 support
- Beyond 8K resolutions achieved with maximum link rate to up to 20 Gbps/lane and more efficient 128b/132b channel coding

DisplayPort™

EVOLUTION OF DISPLAYPORT DATA BANDWIDTH



DisplayPort 2.1 Link Layer CTS Summary

- DP 2.1 LL CTS v1.1 will release in Q4 2025
- Major updates:
  - Updates to align with other published VESA standards and terminology
  - Incorporated many approved and published SCRs
    - For example: FEC, Audio, DisplayID, min Hblank/Vblank, etc
  - Addition of new Source, Sink and Branch device MST tests (covered separately)

VESA Certified DisplayHDR, ClearMR and AdaptiveSync

VESA Display Performance Standards

VESA's display performance metrics work group has been busy since the initial release of the DisplayHDR CTS in 2017.

- VESA Certified DisplayHDR r1.2
- VESA Certified Clear Motion Ratio (CMR) r1.1 and expansion to add new tiers
- VESA Certified AdaptiveSync r1.1

DisplayHDR Summary

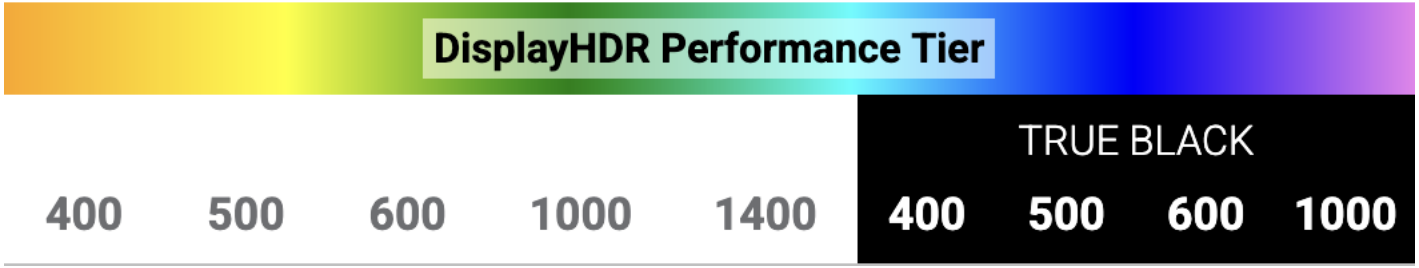
- Industry's first open HDR specification for LCD and emissive (OLED/microLED) displays with a fully transparent testing methodology
- More than 3000 display models certified under logo program to date makes VESA Certified DisplayHDR one of the most successful logo programs in VESA history.
- More details available at https://displayhdr.org

VESA Defines New Standard to Help Speed PC Industry Adoption of High Dynamic Range Technology in Laptop and Desktop Monitor Displays

DisplayHDR is industry's first open HDR specification with a fully transparent testing methodology

SAN JOSE, Calif. – December 11, 2017 – The Video Electronics Standards Association (VESA®) today announced it has defined the display industry's first fully open standard specifying high dynamic range (HDR) quality, including luminance, color gamut, bit depth and rise time, through the release of a test specification. The new VESA High-Performance Monitor and Display Compliance Test Specification (DisplayHDR) initially addresses the needs of laptop displays ar

DisplayHDR Certified Products



- Test tools and measurement templates for all DisplayHDR CTS versions are available for download from the **VESA GitHub page**
- DisplayHDR certification program is the most successful certification program in VESA history with thousands of certified product listings
- Total certified DisplayHDR 1400 products exceeded 240 certifications this year (including family models)

ClearMR Summary

- VESA developed motion blur performance compliance test specification for LCD and emissive (OLED/microLED) displays with a new Clear Motion Ratio (CMR) metric and fully transparent testing methodology
- Over 270 display models certified under ClearMR logo program to date
- More details available at https://www.clearmr.org/

VESA BRINGS CLARITY TO MOTION BLUR IN DIGITAL DISPLAYS WITH NEW COMPLIANCE TEST SPECIFICATION AND LOGO PROGRAM

ClearMR specification and logo program provide consumers with a true quality metric for grading motion blur performance for LCD and OLED panels, TVs, desktop monitors and embedded displays

BEAVERTON, Ore. – August 22, 2022 – The Video Electronics Standards Association (VESA®) today introduced the ClearMR Compliance Test Specification (ClearMR), an industry standard and logo program that provides a new quality metric for grading motion blur in digital displays. ClearMR is applicable to both LCD and emissive display products, including display panels, TVs, monitors, and computers with embedded displays, such as all-in-ones, laptops, notebooks and tablets. The new metric Clear Motion Ratio (CMR), as

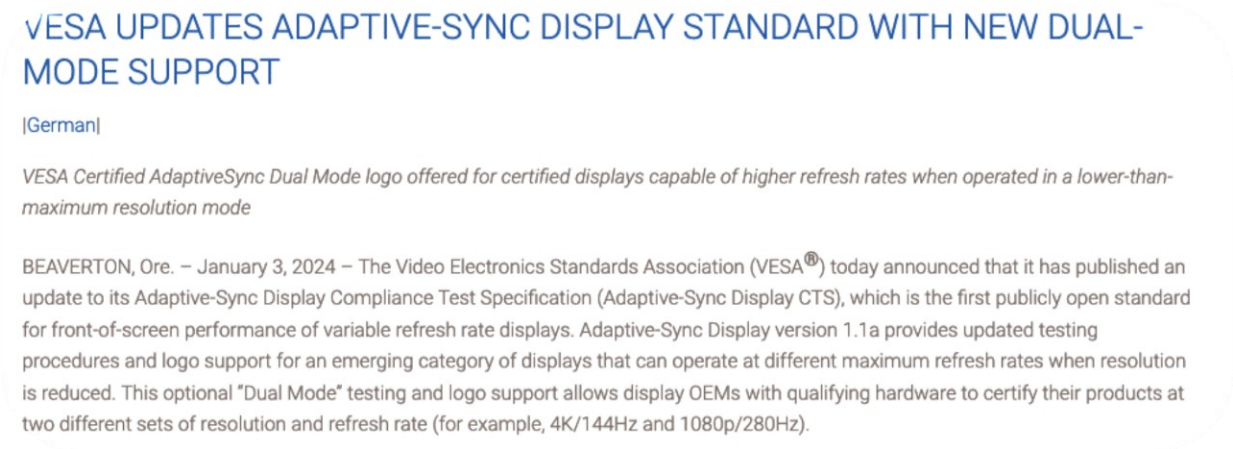
ClearMR Certified Products

- Certified ClearMR performance tiers
  - ClearMR 3000 to ClearMR 21000
  - 15000, 18000 and 21000 are new tiers added in 2024
- ClearMR performance criteria and certified product listing CTS and test tool are available here:
- https://www.clearmr.org/certified-products/

ClearMR TIER	CMR Range
3000	2500 ≤ CMR < 3500
4000	3500 ≤ CMR < 4500
5000	4500 ≤ CMR < 5500
6000	5500 ≤ CMR < 6500
7000	6500 ≤ CMR < 7500
8000	7500 ≤ CMR < 8500
9000	8500 ≤ CMR < 9500
10000	9500 ≤ CMR < 10500
11000	10500 ≤ CMR < 11500
12000	11500 ≤ CMR < 12500
13000	12500 ≤ CMR < 14000
15000	14000 ≤ CMR < 16500
18000	16500 ≤ CMR < 19500
21000	19500 ≤ CMR

VESA Adaptive-Sync Display Summary

- Industry's first publicly open standard for front-of-screen performance of variable refresh rate displays.
- Over 280 AdaptiveSync certifications (20 dual mode) and 31 MediaSync certifications since introduction of certification program
- More details available at https://www.adaptivesync.org/



VESA UPDATES ADAPTIVE-SYNC DISPLAY STANDARD WITH NEW DUAL-MODE SUPPORT

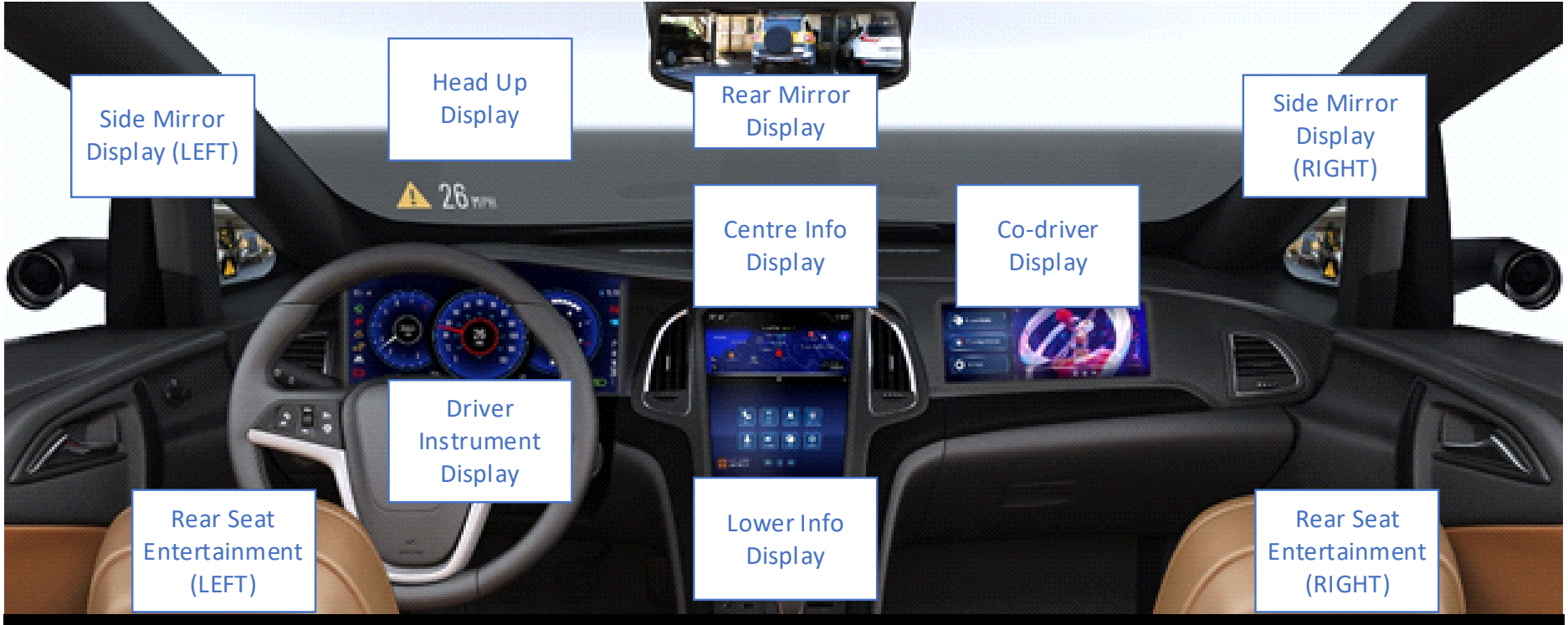
|German|

VESA Certified AdaptiveSync Dual Mode logo offered for certified displays capable of higher refresh rates when operated in a lower-than-maximum resolution mode

BEAVERTON, Ore. – January 3, 2024 – The Video Electronics Standards Association (VESA®) today announced that it has published an update to its Adaptive-Sync Display Compliance Test Specification (Adaptive-Sync Display CTS), which is the first publicly open standard for front-of-screen performance of variable refresh rate displays. Adaptive-Sync Display version 1.1a provides updated testing procedures and logo support for an emerging category of displays that can operate at different maximum refresh rates when resolution is reduced. This optional "Dual Mode" testing and logo support allows display OEMs with qualifying hardware to certify their products at two different sets of resolution and refresh rate (for example, 4K/144Hz and 1080p/280Hz).

Introduction to VESA

DisplayPort Automotive Extensions



- Instrument clusters, HUDs, mirrors, and rear-seat entertainment
- ASIL-D safety, UN155 and ISO 21434 security may be required
- Existing DP/eDP protocols were not built with these challenges in mind.
- Forcing OEMs into fragmented, non-standard solutions.

Introducing DisplayPort Automotive Extension (DP-AE)

- Builds on DP 2.1a/eDP 2.0 with safety & security enhancements
- Functional Safety via ROI CRCs, Frame Counters, Timeout Monitoring
  - Per region CRCs (up to 16 ROIs)
  - Automatic SafeState transitions
- Data Integrity with SPDM (Security Protocol and Data Model) authentication & MAC (Message Authentication Code) tagging
- Secure AUX messaging & protocol stack isolation
- End-to-end Safety/Security supporting CRCs, MACs, SPDM-based authentication
- Support for Superframes and Subframes
- C-Model Emulator enables compliance testing
- Low complexity, high ecosystem readiness

Key Takeaways

- Protocol level extension of DP 2.1 for the use of automotive display interface
  - Enablement with AES_SDP and extensive DPCD registers
- Features that facilitate the support of Functional Safety (FuSa) and security
  - ROI: region of interest
  - CRCs for Datapath, MSA, and SDP
  - Soft Fail/Hard Fail fault detection for robustness
  - SPDM-based device authentication
  - MACs for Datapath, MSA and Active Frame data
  - Automotive-grade encryption on control plane (DP AUX) and/or data plane (MSA, AES_SDP, active frame)
- Profiles 1-4 to accommodate various levels of FuSa and security requirements
- Use Superframe to simplify connectivity while maintaining the versatility of DP AE functions

Current Status and Timeline

- Spec:
  - 1.0 released in December 2023
  - 1.1 adoption vote: end of October 2025
- CTS:
  - First draft release: December 2025
  - TE implementation completion: end of March 2026
  - PlugFest to be held in Q1 or Q2 2026

VESA Technology Development Areas

VESA Technology Development

VESA members are collaborating on several key technology areas

- Embedded DisplayPort - v2.0 (published Sept 2024)
- DP Tunneling over USB4 – compliance testing has begun
- AR/VR Task Group
  - Focused on creating solutions roadmap to meet performance, power and implementation requirements for future AR/VR needs. Specification is released. Work on CTS underway
- DP Automotive Extension Task Group
  - Working with automotive industry to address needs for high-resolution performance in this market segment
  - Working on DP AE CTS and testing
- MST Compliance Test Updates
  - DP 2.1 LL CTS v1.1 near release and new tests were run at last weeks PlugTest event
- Display Performance Metrics Task Group
  - DisplayHDR, ClearMR, AdaptiveSync updates and proposals for future capabilities

DP2.1 Compliance Tests Update Rev 1.1

DP2.1 合规性测试更新修订版 1.1

Name: Neal Kendall (Alok Soni)
Company: Teledyne LeCroy
Date: 10/28/2025 (28-Oct-2025)

姓名：Neal Kendall
公司：Teledyne LeCroy
日期：2025年10月28日（2025年10月28日）

Overview of Test Updates for CTS Rev 1.1

CTS 修订版1.1的测试更新概述

Section 4 Source Device Tests

- 4.2 Source Device Services Test Procedures.
- 4.3 Source Device Link Services Test Procedures.
- 4.4 Source Device Isochronous Transport Services Test Procedures.
- 4.5 Source Device FEC Test Procedures.
- 4.6 DSC Source Device Test Procedures.
- 4.7 Source Device DisplayPort DisplayID/EDID and Native DisplayID Test Procedures.
- 4.8 Source Device DisplayPort Adaptive-Sync Test Procedures.
- 4.9 Source Device LTTPR Test Procedures.
- 4.10 Source Device MST Compliance Tests.
- 4.10.1 Source Device MST Protocol Tests.

第 4 部分 源设备测试

- 4.2 源设备服务测试程序
- 4.3 源设备链路服务测试程序
- 4.4 源设备同步传输服务测试程序
- 4.5 源设备 FEC 测试程序
- 4.6 DSC 源设备测试程序
- 4.7 源设备 DisplayPort DisplayID/EDID 和 Native DisplayID 测试程序
- 4.8 源设备 DisplayPort 自适应同步测试程序
- 4.9 源设备LTTPR测试程序
- 4.10 源设备 MST 合规性测试
- 4.10.1 源设备 MST 协议测试

Color Code: Updated Test – New Test

颜色代码：更新测试 - 新测试

Section 5 Sink Device Tests

- 5.2 Sink Device Services Test Procedures
- 5.3 Sink Device Link Services Test Procedures
- 5.4 Sink Device Isochronous Transport Services Test Procedures
- 5.5 Sink Device FEC Test Procedures
- 5.6 Sink DSC Protocol
- 5.7 Sink Device DisplayPort DisplayID/EDID Test Procedures
- 5.8 Sink Device DisplayPort Adaptive-Sync Test Procedures
- 5.9 Sink Device Embedded LTTPR Test Procedures

第 5 节 水槽设备测试

- 5.2 **接收**设备服务测试程序
- 5.3 **接收**设备链路服务测试程序
- 5.4 接收设备等时运输服务测试程序
- 5.5 接收设备 FEC 测试程序
- 5.6 接收Sink DSC 协议
- 5.7 **接收**设备 DisplayPort DisplayID/EDID 测试程序
- 5.8 **接收**设备 DisplayPort **自适**应同步测试程序
- 5.9 **接收**设备嵌入式 LTTPR 测试程序

Color Code: Updated Test – New Test

颜色代码：更新测试 - 新测试

预

Section 6 Branch Device Tests

- 6.1 to 6.9 (Reserved)
- 6.10 Branch Device MST Tests (Normative)
  - 6.10.1 Branch Setup 1 Tests
  - 6.10.2 Branch Setup 2 Tests
  - 6.10.3 Branch Setup 3 Tests
  - 6.10.4 Branch Setup 4 Tests
  - 6.10.5 Branch Setup 5 Tests
  - 6.10.6 Composite Sink (Daisy-chainable Sink) Setup 1 Tests
  - 6.10.7 Composite Sink (Daisy-chainable Sink) Setup 2 Tests
  - 6.10.8 Composite Sink (Daisy-chainable Sink) Setup 3 Tests
  - 6.10.9 Composite Sink (Daisy-chainable Sink) Setup 4 Tests

第 6 节 分支设备测试

- 6.1 至 6.9（预留）
- 6.10 分支设备 MST 测试（规范）
  - 6.10.1 分支设置 1 测试
  - 6.10.2 分支设置 2 测试
  - 6.10.3 分支设置 3 测试
  - 6.10.4 分支设置 4 测试
  - 6.10.5 分支设置 5 测试
  - 6.10.6 复合接收（菊花链接收）设置 1 测试
  - 6.10.7 复合接收（菊花链接收）设置 2 测试
  - 6.10.8 复合接收（菊花链接收）设置 3 测试
  - 6.10.9 复合接收（菊花链接收）设置 4 测试

Color Code: Updated Test – New Test

颜色代码：更新测试 - 新测试

Sec. 7 LTTPR & DP Tunnel Device Tests

- 7.1 LTTPR and DP Tunnel Device Test Procedures

第 7 节 LTTPR 和 DP 隧道设备测试

- 7.1 LTTPR和DP隧道设备测试程序

MST Source Tests

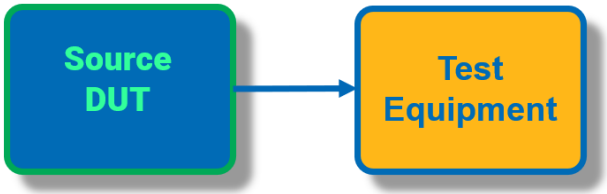
MST 源测试

Approved DP 2.1 Compliance Tests
Source Device MST tests

- VESA Approved Tests with new numbers (4.10.1.1 to 4.10.1.21).

经批准的 DP 2.1 合规性测试
源设备 MST 测试

- VESA 批准的新编号测试（4.10.1.1 至 4.10.1.21）。



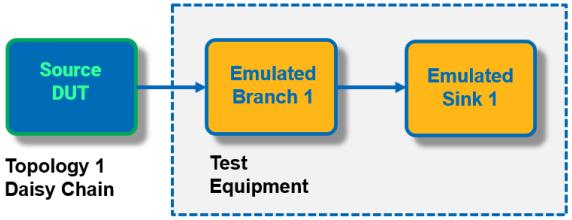
Source Setup - 1

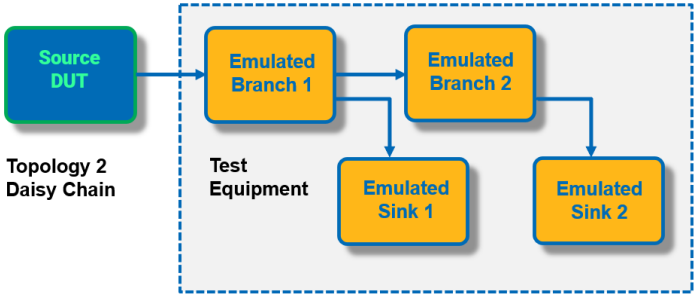
Color Code: Updated Test – New Test

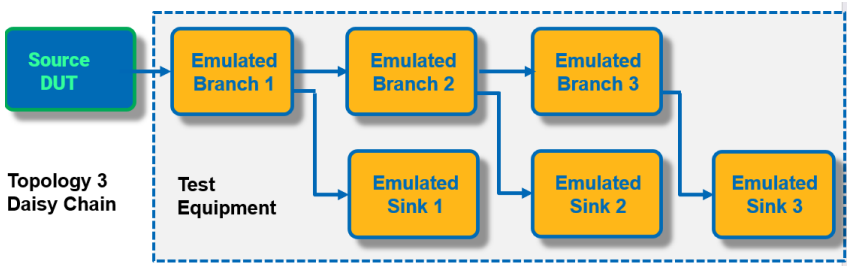
颜色代码：更新测试 - 新测试

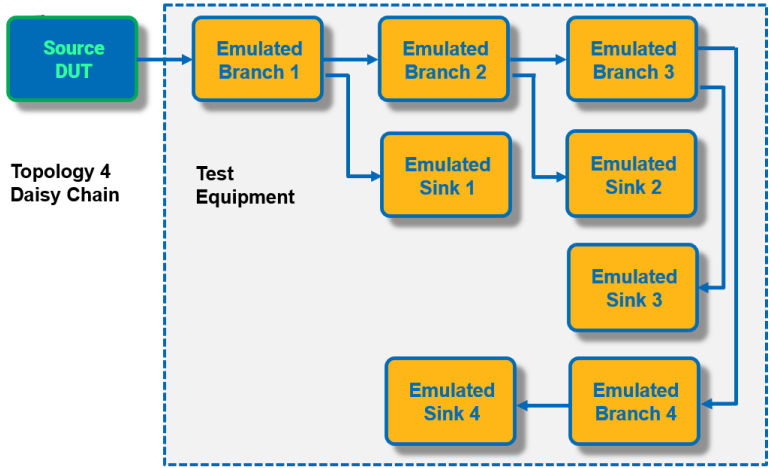
Approved DP 2.1 Compliance Tests
Source Device MST Test Setups

经批准的 DP 2.1 合规性测试
源设备 MST 测试设置



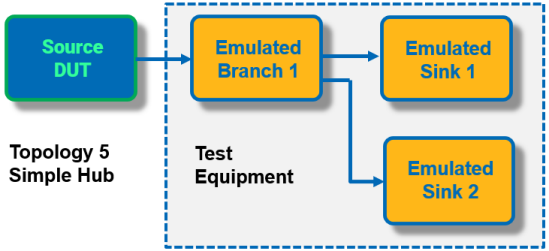


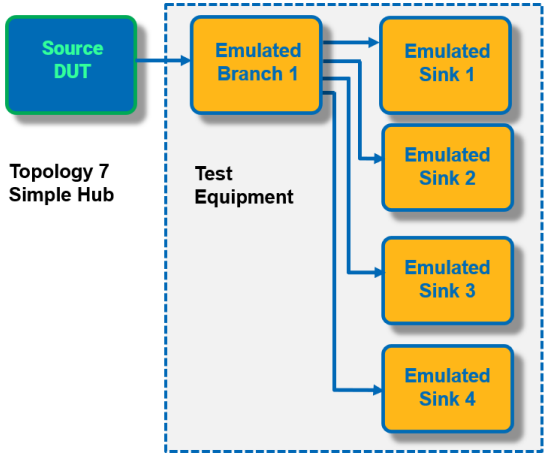


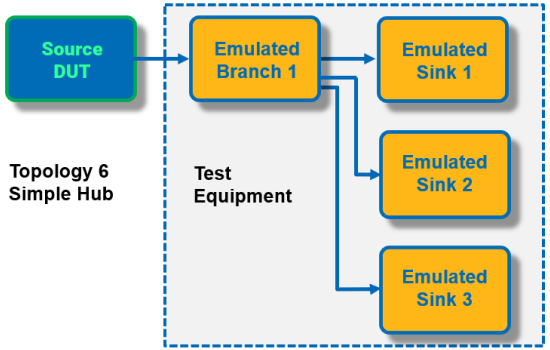


Approved DP 2.1 Compliance Tests
Source Device MST Test Setups

经批准的 DP 2.1 合规性测试
源设备 MST 测试设置







MST Source CTS CDF entries　　MST 源 CTS CDF 条目

S.No	CDF Entry	Default Value
1	MST_TRANSMISSION	Yes
2	MST_MAX_STREAM_COUNT	4
3	MST_UP_REQUEST_SUPPORTED	Yes
4	MST_RSN_REQUEST_SUPPORTED	No
5	MST_MAX_DAISY_CHAIN_SINK_SUPPORTED	4
6	MST_POWER_UP_DOWN_PHY_SUPPORTED	Yes

MST Source Device Tests

Main validation points

- MST Capability read, Link Address, Path Enum Resources, Allocate Payload, Video Validation.
- Connection Status Notification (CSN) Up Request handling for addition, removal.
- Optional Resource Notification (RSN) update handling.
- EDID and NDID read, DSC & FEC capability read.
- Handling of error case (Unknown Up request, NACK, incorrect Down reply or timeout during down reply).
- MST to SST and SST to MST transition.
- In and out of Low Power Mode (Wake/Sleep).
- Writing unique GUIDs.

MST 源设备测试

主要验证点

- MST 功能读取、链路地址、路径枚举资源、分配有效负载、视频验证。
- 连接状态通知 （CSN） 启动请求处理添加、删除。
- 可选资源通知 （RSN） 更新处理。
- 读取 EDID 和 NDID，读取 DSC 和 FEC 功能。
- 处理错误情况（未知的启动请求、NACK、不正确的关闭回复或关闭回复期间的超时）。
- MST 到 SST 和 SST 到 MST 的转换。
- 进入和退出低功耗模式。
- 编写唯一的 GUID。

Branch Device Tests

分支设备测试

Approved DP 2.1 Compliance Tests
MST Branch Device tests

- Branch Device Setup 1 (loopback to TE with no External Sink) (6.10.1.1 to 6.10.1.12)
- Branch Device Setup 2 (loopback to TE with 1 External Sink) (6.10.2.1 to 6.10.2.10)
- Branch Device Setup 3 (loopback to TE with 2 External Sink) (6.10.3.1 to 6.10.3.14)
- Branch Device Setup 4 (loopback to TE with 3 External Sink) (6.10.4.1 to 6.10.4.14)
- Branch Device Setup 5 (with 4 External Sink) (6.10.5.1 to 6.10.5.4)

经批准的 DP 2.1 合规性测试
分支设备 MST 测试

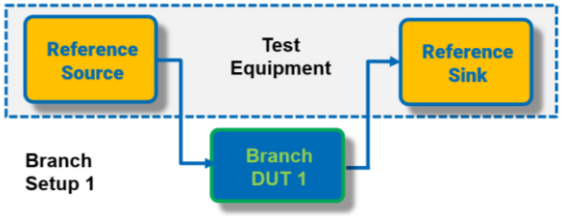
- 分支设备设置1（环回到TE，无外部接收器）（6.10.1.1至6.10.1.12）
- 分支设备设置2（环回到带有 1 个外部接收器的 TE）（6.10.2.1 至 6.10.2.10）
- 分支设备设置3（环回到带有 2 个外部接收器的 TE）（6.10.3.1 至 6.10.3.14）
- 分支设备设置4（环回到带有 3 个外部接收器的 TE）（6.10.4.1 至 6.10.4.14）
- 分支设备设置5（带 4 个外部接收器）（6.10.5.1 至 6.10.5.4）

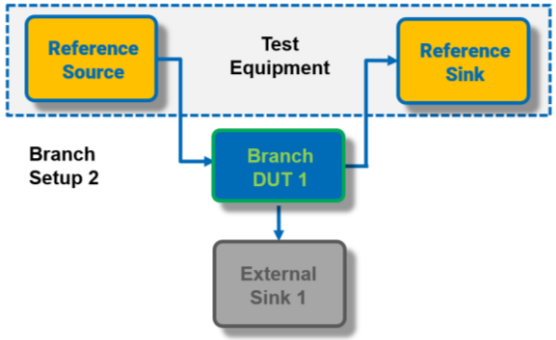
Color Code: Updated Test – New Test

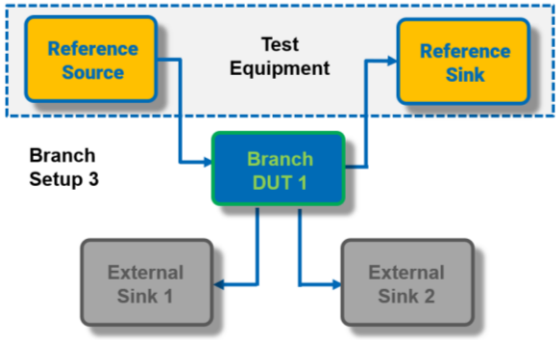
颜色代码：更新测试 - 新测试

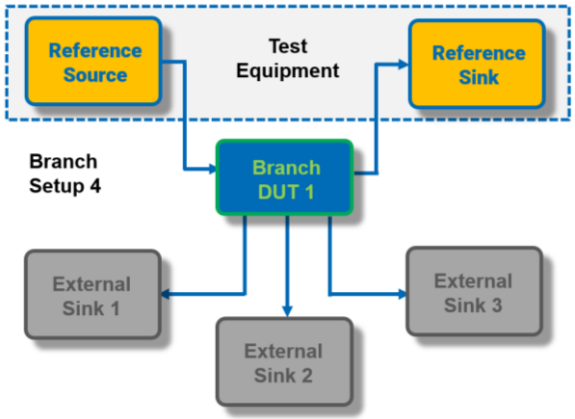
Approved DP 2.1 Compliance Tests
MST Branch Device Test Setups

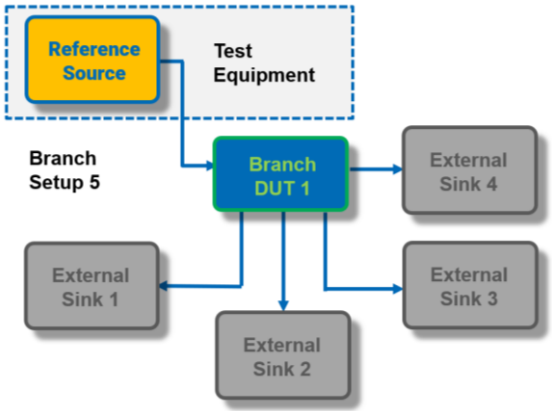
经批准的 DP 2.1 合规性测试
MST 分支设备测试设置











MST Branch Device CDF entries　　MST分支设备 CDF 条目

S.No	CDF Entry	Default Value	Range
1	BRANCH_DUT_NO_OF_DFP_DPPORT	0	[1-4]
2	BRANCH_DUT_UFP_PORT_NUM_CONNECTED_TO_TE	0	[1-16]
3	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_TE	0	[1-16]
4	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK1	0	[1-16]
5	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK2	0	[1-16]
6	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK3	0	[1-16]
7	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK4	0	[1-16]
8	BRANCH_DUT_CSN_DFP_BROADCAST	No	Yes/No

Branch DUT tests
Main validation points

- Capability validation, forwards up/down request, response for Enum Path Resources, Query Payload, Video Validation for DSC and Non-DSC video.
- Remote DPCD read/write validation via TE internal memory.
- Timeslots calculation and allocations.
- Response for Remote I2C Read, Remote DPCD read/write, link address request.
- Low Power mode enter/exit.
- CSN Up/down request generation.
- Time slot increase/decrease/delete/addition.

分支 DUT 测试
主要验证点

- **功能**验证、转发上/**下**请求、枚举路**径**资源的响应、查询有效负载、DSC **和非** DSC 视频的视频验证。
- **通**过 TE **内部存**储器进行远程 DPCD 读/**写**验证。
- 时段计算和分配。
- **响**应远程 I2C 读取、远程 DPCD 读/**写**、链路地址请求。
- **低功耗模式**进入/**退出**
- CSN **上**/**下**请求生成。
- 时隙增加/**减少**/删除/**添加**

MST Composite Sink Device Tests

MST 复合接收设备测试

Approved DP 2.1 Compliance Tests
MST Composite Sink Device tests

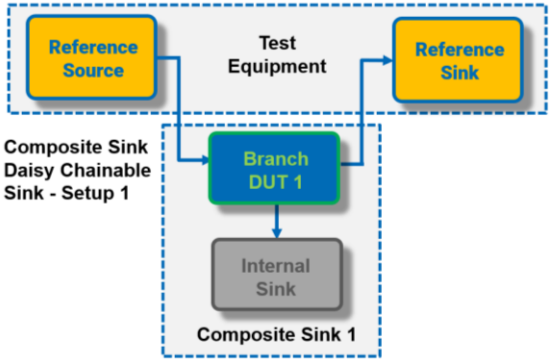
- Composite Sink Device Setup1 (loopback to TE from DP OUT port) (6.10.6.1 to 6.10.6.22).
- Composite Sink Device Setup2 (loopback to TE from DP OUT port) (6.10.7.1 to 6.10.7.21).
- Composite Sink Device Setup3 (loopback to TE from DP OUT port) (6.10.8.1 to 6.10.8.5).
- Composite Sink Device Setup4 (4 DUTs in Daisy chain) (6.10.9.1 to 6.10.9.3).

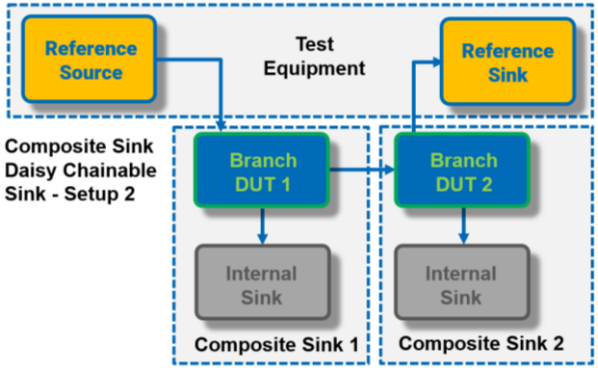
经批准的 DP 2.1 合规性测试
复合接收设备 MST 测试

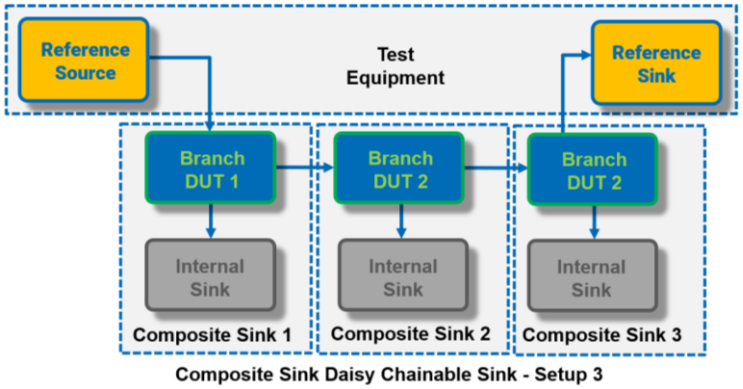
- 复合接收设备设置1（从 DP输出端口环回到 TE）（6.10.6.1 至 6.10.6.22）
- 复合接收设备设置2（从 DP输出端口环回到 TE）（6.10.7.1 至 6.10.7.21）
- 复合接收设备设置3（从 DP 输出端口环回到 TE）（6.10.8.1 至 6.10.8.5）
- 复合接收装置设置4（菊花链中的 4 个 DUT）（6.10.9.1 至 6.10.9.3）

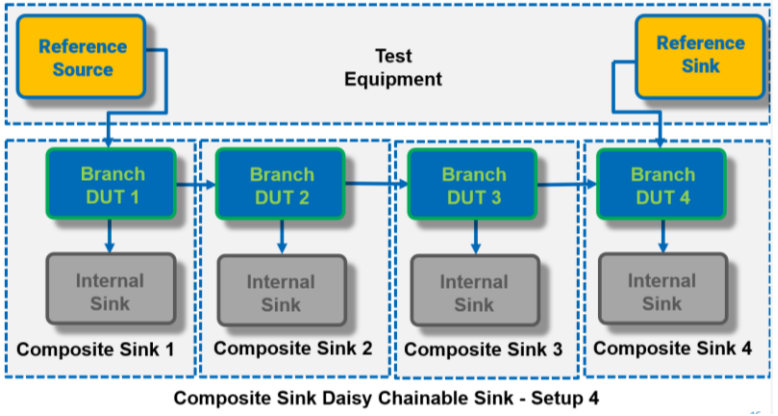
Approved DP 2.1 Compliance Tests
Composite Sink Device Test Setups

经批准的 DP 2.1 合规性测试
复合接收设备测试设置









MST Composite Sink DUT tests
Main validation points

- Capability validation, forward up/down request, response for Enum Path Resources, Query Payload, Video Validation for DSC and Non-DSC video.
- Remote DPCD read/write validation via TE internal memory.
- Timeslots calculation and allocations.
- Response for Remote I2C Read, Remote DPCD read/write, link address request.
- Low Power mode enter/exit
- CSN Up/down request generation.
- Time slot increase/decrease/delete/addition.

MST 复合接收器 DUT 测试
主要验证点

- **功能**验证、转发向上/**向下**请求、枚举**路径**资源的响应、查询有效负载、DSC **和非** DSC 视频的视频验证。
- **通**过 TE **内部存**储器进行远程 DPCD 读/**写**验证。
- 时段计算和分配。
- **响**应远程 I2C 读取、远程 DPCD 读/**写**、链路地址请求。
- **低功耗模式**进入/**退出**
- CSN **上**/**下**请求生成。
- 时隙增加/**减少**/删除/**添加**。

EDID and NDID Tests

EDID 和 NDID 测试

Unique Test Numbers
EDID & NDID tests

EDID Tests

- EDID Sink CTS (5.7.15.12) (5.7.16.11).

NDID Tests

- NDID Source CTS (4.7.4.5 to 4.7.4.8) (4.7.5.2)
- NDID Source Adaptive Sync (4.8.1.3 to 4.8.1.4) (4.8.2.4 to 4.8.2.6).
- NDID Sink CTS (5.4.7.10 to 5.4.7.18) (5.7.5.2) (5.7.6.6 to 5.7.6.10) (5.7.7.7 to 5.7.7.12) (5.7.8.7 to 5.7.8.12) (5.7.9.4 to 5.7.9.6) (5.7.10.4 to 5.7.10.6) (5.7.11.6 to 5.7.11.10) (5.7.12.5 to 5.7.12.8) (5.7.14.9 to 5.7.14.16) (5.7.17.6 to 5.7.17.10).
- NDID Sink Adaptive Sync (5.8.1.4 to 5.8.1.6).

唯一测试编号
EDID 和 NDID 测试

EDID测试

- EDID 接收 CTS （5.7.15.12） （5.7.16.11）

NDID 测试

- NDID 源 CTS（4.7.4.5 至 4.7.4.8） （4.7.5.2）
- NDID 源自适应同步（ 4.8.1.3 至 4.8.1.4） （4.8.2.4 至 4.8.2.6）
- NDID 接收 CTS（5.4.7.10 至 5.4.7.18） （5.7.5.2） （5.7.6.6 至 5.7.6.10） （5.7.7.7 至 5.7.7.12） （5.7.8.7 至 5.7.8.12） （5.7.9.4 至 5.7.9.6） （5.7.10.4 至 5.7.10.6） （5.7.11.6 至 5.7.11.10） （5.7.12.5 至 5.7.12.8） （5.7.14.9 至 5.7.14.16） （5.7.17.6 至 5.7.17.10）
- NDID 接收自适应同步（ 5.8.1.4 至 5.8.1.6）

New Tests in CTS Rev 1.1

CTS Rev 1.1 中的新测试

New Test Additions in Rev 1.1

Source Tests:

- 4.2.2.15 Verification of DPCD 110h Values on USB-C Cable Connect with Source DUT before Link Training.

Sink Tests:

- 5.2.2.11 Verification of DPCD 2217h Values on Upstream Device Disconnect and Power-on Reset.

Rev 1.1 中的新增测试

源测试：

- 4.2.2.15 在链路训练之前,验证 USB-C 电缆与源 DUT 连接上的 DPCD 110h 值。

水槽测试：

- 5.2.2.11 上游设备断开和上电复位时 DPCD 2217h值的验证。

Color Code: Updated Test – New Test

颜色代码：更新测试 - 新测试

Updated Tests in CTS Rev 1.1

CTS Rev 1.1 中的更新测试

Test Updates in Rev 1.1
Source Device Tests

- Link Training Tests - INTRAHOP_AUX_REPLY_INDICATION check before UHBR Link Training. If set only then Source driver shall write DPCD 102h=00h to clear it, else do not write 102h=00h to clear intra hop as it is already clear. This change affects all UHBR Link Training procedure validation.
- Link Training Tests - Same Link Configuration retry 1 time or 2 times, controlled by CDF and affect all Link Training fallback tests.

Rev 1.1 中的测试更新
源设备测试

- 链路训练测试 - INTRAHOP_AUX_REPLY_INDICATION在 UHBR 链路训练之前进行检查。如果仅设置了该值，则源驱动程序应写入 DPCD 102h=00h 来清除该值， 否则不要写入 102h=00h 以清除跳内数据，因为该值已经清除。此更改会影响所有 UHBR 链路训练流程验证。
- 链路训练测试 - 相同的链路配置重试 1 次或 2 次，由 CDF 控制并影响所有链路训练回退测试。

Color Code: Updated Test – New Test

颜色代码：更新测试 - 新测试

Test Updates in Rev 1.1
Source Device Tests (continued)

- 4.3.1.21 Update for 20 loop or max time budget during EQ loop not able to achieve EQ lock.
- 4.2.2.13 update check defer after LTTPR discovery.
- 4.9.1.22 LTTPR discovery check validation handling after HPD may not be the first transaction.
- 4.3.3.2 Least pack format change for 1L UHBR10 for video test.
- Minor update in 4.7.5.1.

Rev 1.1 中的测试更新
源设备测试（续）

4.3.1.21 更新 20 循环或 EQ 循环期间的最大时间预算无法实现 EQ 锁定。

4.2.2.13 LTTPR 发现后更新检查延迟。

4.9.1.22 HPD 后的 LTTPR 发现检查验证处理可能不是第一个事务。

4.3.3.2 用于视频测试的 1L UHBR10 的包装格式变化最少。

4.7.5.1 中的小更新

Test Updates in Rev 1.1
Sink Device Tests

- 5.2.2.5 DPCD Address Range - Do not check Vendor Specific fields
- 5.3.1.5 Successful Link Training at Lower Link Rate/Bandwidth Due to Loss of Symbol Lock during Channel Equalization Sequence - EQ Done bit validation removed. Only use Symbol lock for validation.
- Some Sink Tests will be skipped if DP Tunnel is detected.
- Minor update in 5.7.14.1 EDID – DTD Type X Block Revision (Byte #1).
- Minor updates in 5.6.2.[12/13/14] – DSC Interrupt tests.

Rev 1.1 中的测试更新
水槽设备测试

- 5.2.2.5 DPCD 地址范围 - 不选中“供应商特定”字段
- 5.3.1.5 由于在信道均衡序列期间丢失符号锁定，在较低的链路速率/带宽下成功进行链路训练 - EQ 已删除完成位验证。仅使用符号锁进行验证。
- 如果检测到 DP 隧道，则某些接收器测试将被跳过。
- 5.7.14.1 EDID 中的小更新 – DTD Type X 块修订版（字节 #1）。
- 5.6.2 中的小更新。[12/13/14] – DSC 中断测试。

Color Code: Updated Test – New Test

颜色代码：更新测试 - 新测试

Test Updates in Rev 1.1
LTTPR Device Tests

- 7.1.1.4 Phy Repeater Link Rate Validation test - Wait for 10 second cable unplug before switching to Non-LTTPR Mode. Update clarification for Tunnel working as retimer.
- 7.1.5.1 LTTPR 8b/10b DP Symbol Error Validation Test, With 0 Emulated LTTPRs, Symbol Error Counter Validation at Max Supported Lane Count and 8b/10b DP Link Rate - Correction of Symbol error counter setting on LTTPR Address range, not the sink DPCD.

Test Updates in Rev 1.1
LTTPR Device Tests

- 7.1.1.4 Phy 中继器链路速率验证测试 - 等待电缆拔下 10 秒后再切换到非 LTTPR 模式。更新了 Tunnel 用作重定时器的说明。
- 7.1.5.1 LTTPR 8b/10b DP 符号错误验证测试，模拟 LTTPR 为 0，在最大支持通道数和 8b/10b DP 链路速率下进行符号错误计数器验证 - 校正 LTTPR 地址范围内的符号错误计数器设置，而不是接收器 DPCD。

Color Code: Updated Test – New Test

颜色代码：更新测试 - 新测试

Questions?

问题？

DisplayPort Electrical Testing Overview

Zhidong Tian
Keysight Technologies
10/28/2025

Agenda

- DP2.1 Electrical Compliance Test Requirements
- DP2.1 PHY Updates
- DP2.1 Transmitter Test
- DP2.1 Receiver Test
- eDP PHY Electrical Conformance Testing

DP2.1a Electrical Compliance Test Requirement

DisplayPort Interface

Main Link

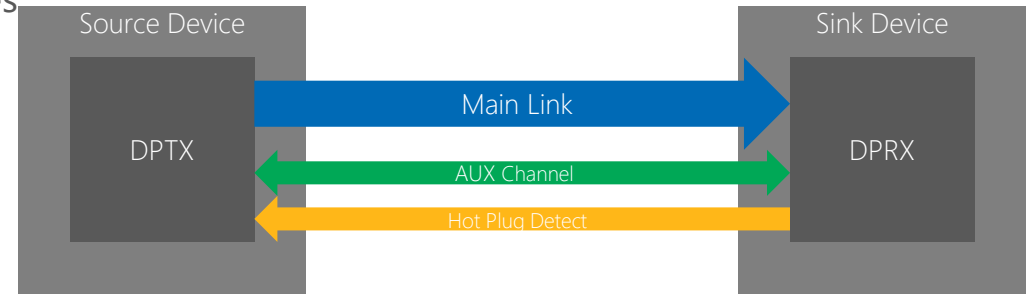
- Display data transfer
- 4 unidirectional high-speed lanes
- Multiple bitrates supported

AUX Channel

- Link management
- Test mode control
- 1 bidirectional low-speed lane

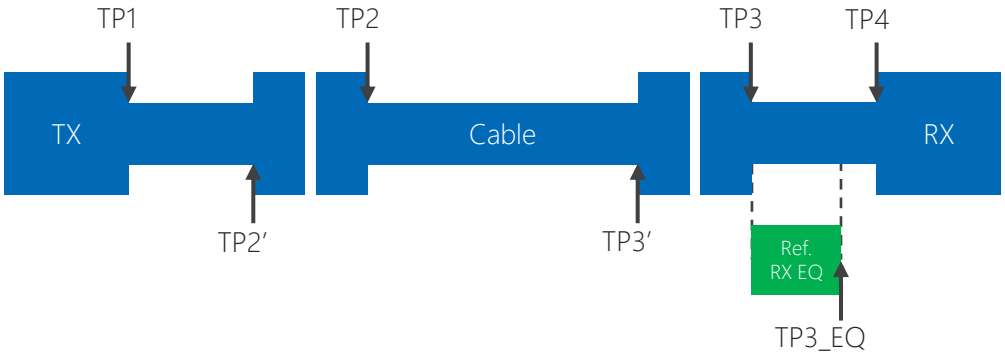
Hot Plug Detect

- Source detects presence of sink
- Sink notifies of status changes via IRQ



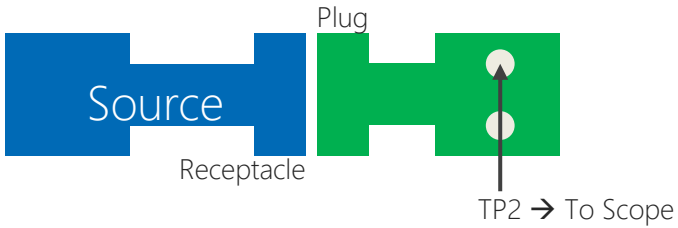
Test Points

Test Point	Definition
TP1	Source transmitter pins.
TP2	Test interface of a TPA, next to mated connection to a DP source.
TP2’	RX JTOL signal injection point for DUTs with plug.
TP2_CTLE	RX JTOL calibration and test point for DUTs with plug.
TP3	Test interface of a TPA, next to mated connection to a DP sink.
TP3’	Signal injection point to a DP sink.
TP3_EQ	TP3 using a defined DP cable model with equalization applied.’
TP3_CTLE	TP3 using a defined HBR3 cable model with CTLE applied.
TP3_DFE	TP3 using a defined HBR3 cable model with CTLE and DFE applied.
TP4	Sink receiver pins.

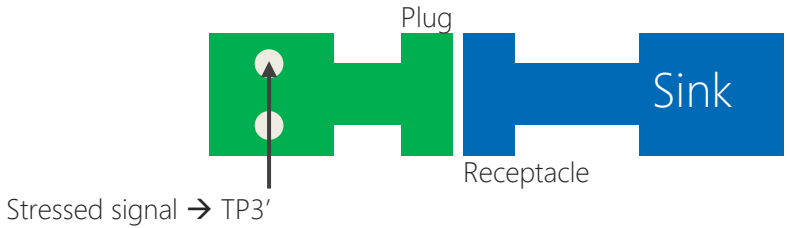


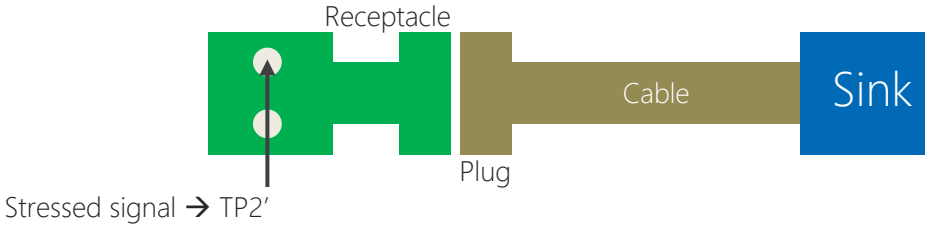
Test Point Access Examples

DPTX Testing



DPRX Testing





How to test the PHY layer?

Source

- Configure the source to output test patterns with certain drive settings → **AUX controller**
- Embed worst-case channels, apply equalization on the oscilloscope
- Run measurements

Sink

- Generate the stress signal with a pattern generator
- Guide the sink through Link Training → **AUX controller**
- Read built-in error counter → **AUX controller**

DP2.1 PHY Updates

Electrical Updates from DP2.1 to DP2.1a to DP2.1b

- There are minimal changes in 8b/10b electrical compliance testing.
- A new DP54 cable has been introduced in DP2.1a for UHBR13.5.
- The UHBR13.5 Source Enhanced FSDP testing will utilize the new DP54 cable model.
- A new DP80LL cable has been introduced in DP2.1b for UHBR20.
- The UHBR20 Source with 9dB loss budget will utilize the DP80LL cable.
- Changes in test limits primarily affect Source Testing.

- UHBR10
  - DPTX TP2
    - Total Jitter =380 mUI
    - Data-Dependent Jitter =160 mUI
    - Eye Width = 600 mUI
    - Eye Height = 242 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 185 mV
  - DPTX TP3_EQ
    - Total Jitter =450 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 115 mV
  - DPRX TP3_EQ
    - Total Jitter =485 mUI
    - Data-Dependent Jitter =240 mUI
    - Eye Width = 540 mUI
    - Eye Height = 112 mV
- UHBR20
  - DPTX TP2
    - Total Jitter =435 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 240 mV
  - DPTX TP3_EQ
    - Total Jitter =455 mUI
    - Data-Dependent Jitter =210 mUI
    - Eye Width = 560 mUI
    - Eye Height = 100 mV
  - DPRX TP3_EQ
    - Data-Dependent Jitter =255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV

- UHBR10
  - DPTX TP2
    - Total Jitter =440 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 550 mUI
    - Eye Height = 162 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 200 mV
  - DPTX TP3_EQ
    - Total Jitter =515 mUI
    - Data-Dependent Jitter =245 mUI
    - Eye Width = 520 mUI
    - Eye Height = 80 mV
  - DPRX TP3_EQ
    - Total Jitter =530 mUI
    - Data-Dependent Jitter =260 mUI
    - Eye Width = 520 mUI
    - Eye Height = 73 mV
- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI

- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI

- UHBR20
  - DPTX TP2 EnhDP DP80
    - Total Jitter = 480 mUI
    - Data-Dependent Jitter = 200 mUI
    - Eye Width =540 mUI
    - Eye Height = 240 mV
  - DPTX TP2 EnhDP DP80LL
    - Total Jitter = 495 mUI
    - Data-Dependent Jitter = 220 mUI
    - Eye Width =530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ for all connector Type
    - Total Jitter = 500 mUI
    - Data-Dependent Jitter = 210 mUI
    - Eye Width =560 mUI
    - Eye Height = 100 mV
  - DPRX TP3EQ for all connector type
    - Data-Dependent Jitter = 255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV

DP2.1 PHY CTS Errata

- Clarification on 8b/10b SSC Modulation Deviation Limit
- Test fixture insertion loss update
- FFE Preset 15 measurement update
- LTTPR Frequency Variation test update
- Eye Height and Mask requirement update for UHBR Rates
- BERT Preset Calibration

DP2.1 Transmitter Test

Electrical Transmitter Tests

Item	Name	Normative/ Informative
3.1	Eye Diagram Test	Normative
3.2	HBR/RBR Non-PE Level Verification Test	Normative
3.3	HBR/RBR PE Level Verification and Maximum Differential Peak-to-Peak Voltage Test	Normative
3.4	HBR3/HBR2 PE Level and Equalization Verification Test	Normative
3.5	HBR3/HBR2 $V_{TX\_DIFFp\text{-}p\_MAX}$ Test	Normative
3.6	Inter-pair Skew Test	Informative
3.7	Intra-pair Skew Test	Informative
3.8	AC Common Mode Noise Test	Informative
3.9	Non-ISI Jitter Measurement Test	Normative
3.10	HBR3 TX Differential RL Test	Informative
3.11	TJ/RJ/DJ Measurement Tests	Normative
3.12	Main-Link Frequency Compliance Test	Normative
3.13	Spread-spectrum Modulation Frequency Test	Normative
3.14	Spread-spectrum Modulation Deviation Test	Normative
3.15	dF/dT Spread-spectrum Deviation High-frequency Variation Test	Informative
xx	Embedded Re-timer Frequency Variation Test	Normative

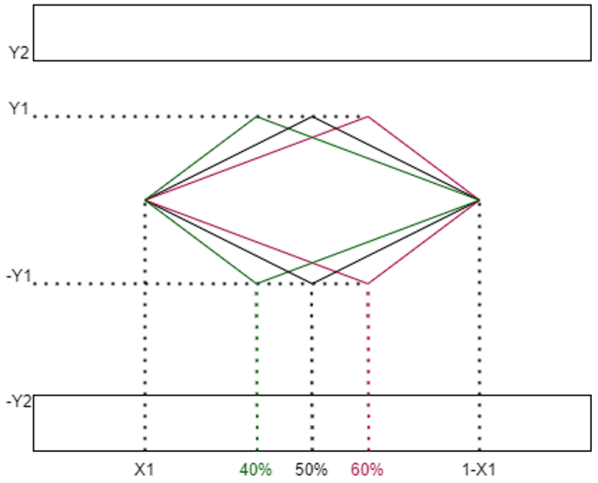
8b/10b

Item	Name	Normative/ Informative
4.2	Preset and CTLE-DFE Declaration	Normative
4.3	UHBR Source Transmitter Equalization	Normative
4.4	UHBR Bit Rate	Normative
4.4	UHBR Unit Interval	Informative
4.5	UHBR SSC Down Spread Range, Rate, Phase Deviation, and Slew Rate	Normative
4.6	UHBR Embedded Re-timer Frequency Variation	Informative
4.7	UHBR TP2 Eye at 1E-6 BER	Normative
4.8	UHBR TP2 Jitter at 1E-9 BER	Normative
4.9	UHBR AC Common Mode Nosie Test	Informative
4.10	UHBR TP3_EQ Eye at 1E-6	Normative
4.11	UHBR TP3_CTLE Jitter at 1E-9	Informative
4.12	UHBR Transmitter Return Loss	Informative

128b/132b

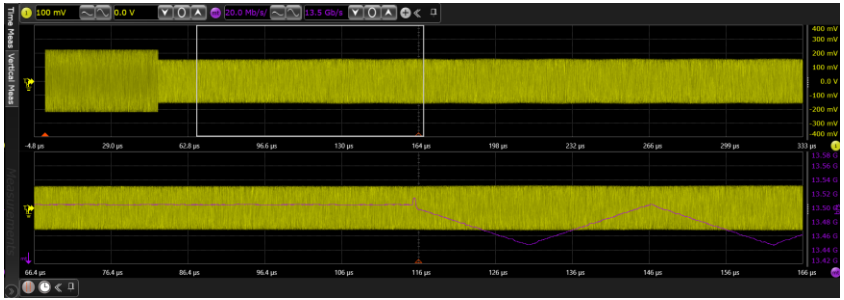
UHBR Eye Mask Update

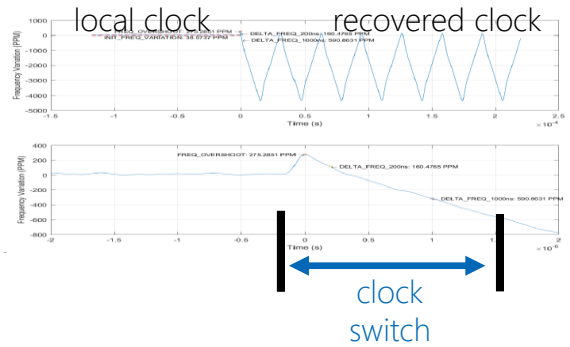
- If original eye mask fails, then modified mask will be used to re-test.
- Modify mask must comply the Y1 and X1 as per the DP 2.1 PHY CTS



LTTPR Frequency Variation Test

- LTTPRs are needed as total channel loss increases with the PHY rate
  - Longer channel
  - More complex link training
- LTTPR Re-timer Clock Switch Test Mode
  - DPCD 0x0010B – 0x0010Eh [7] =1
- Initial Test Challenges
  - Entering Clock Switch test mode
  - Triggering on LTTPR local clock event





DP TX testing challenges

- The test time for DP TX is significant
- DP Source not supporting PHY Test Automation
  - DP Source does not transmit the compliance pattern

DP2.1 Receiver Test

Electrical Receiver Tests

Item	Name	Normative/ Informative
5.1	8b/10b DP Sink JTOL Test	Normative

Item	Name	Normative/ Informative
6.1	128b/132b DP UHBR Sink JTOL Test	Normative

Item	Calibration Point	Name
5.1.3.1.1	TP1-TP3	HBR3 Jitter Calibration
5.1.3.1.2	TP1-TP3	HBR2 Jitter Calibration
5.1.3.1.3	TP1-TP3	HBR Jitter Calibration
5.1.3.1.4	TP2/TP3	HBR3 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR2 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR Eye Height and Total Jitter Calibration
5.1.3.1.5	TP1/TP3	HBR3/HBR2/HBR Crosstalk Calibration
5.1.3.2	TP2/TP3	RBR Jitter Calibration
5.1.3.2	TP3	RBR Eye Height Calibration
5.1.3.2.1	TP3	RBR Crosstalk Calibration

Item	Calibration Point	Name
6.1.3.1.4.1	TP1	AC Common-Mode Interference Calibration
6.1.3.1.4.2	TP1	Random Jitter Calibration
6.1.3.1.4.3	TP1	Periodic Jitter Calibration
6.1.3.1.4.4	TP1	Total Jitter Calibration
6.1.3.1.4.5	TP1	Eye Height Calibration
6.1.3.1.5	TP3	Insertion Loss Calibration
6.1.3.1.6	TP3	Eye Diagram Calibration

BERT Preset Calibration

- To verify the BERT FFE as outlined in the DP 2.1 PHY CTS specification
- The Preset calibration check can assist in identifying setup problems.

Set Preset []	Expected Preshoot [dB]	Measured Preshoot [dB]	Expected Deemphasis [dB]	Measured Deemphasis [dB]	Coeff_1 []	Coeff0 []	Coeff1 []	Pass/Fail
1	0.00	0.10	-1.90	-1.75	0.030	0.870	-0.100	Pass
2	-3.10	-3.16	-3.60	-3.57	0.130	0.690	-0.180	Pass
3	0.00	0.03	-5.00	-4.81	0.030	0.750	-0.220	Pass
4	0.00	-0.20	-8.40	-8.25	0.030	0.655	-0.315	Pass
5	0.90	1.13	0.00	0.20	-0.035	0.965	0.000	Pass
6	1.10	1.18	-1.90	-1.86	-0.020	0.880	-0.100	Pass
7	1.40	1.35	-3.80	-3.60	-0.020	0.810	-0.170	Pass
8	1.70	1.65	-5.80	-5.61	-0.020	0.750	-0.230	Pass
9	2.10	2.03	-8.00	-7.89	-0.020	0.690	-0.290	Pass
10	1.70	1.82	0.00	0.13	-0.080	0.920	0.000	Pass
11	2.20	2.49	-2.20	-2.24	-0.080	0.820	-0.100	Pass
12	2.50	2.31	-3.60	-3.47	-0.060	0.790	-0.150	Pass
13	3.40	3.57	-6.70	-6.64	-0.070	0.700	-0.230	Pass
14	3.60	3.67	0.00	0.01	-0.170	0.830	0.000	Pass

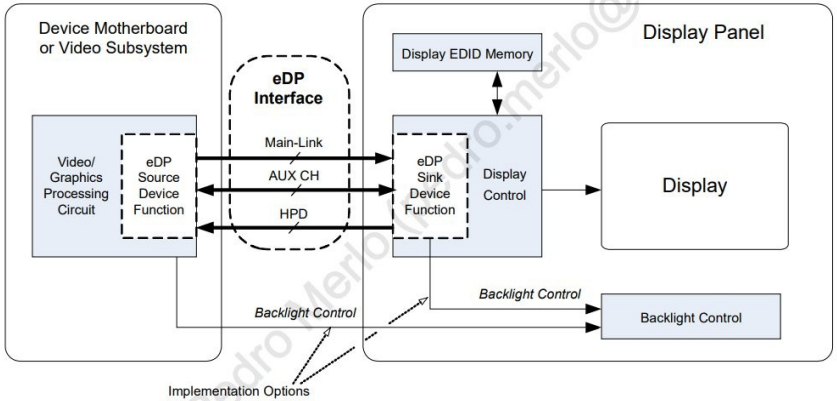
DP RX testing challenges

- Error count registers not enabled in DP Sink
  - Error count register always report 0 errors
  - USB-C Lane orientation causing failure in error counter and link training
- Calibrations take a significant amount of time
  - Different setup needs for 8b/10b and 128b/132b

Embedded DisplayPort

eDP

- Standardized features and interoperability guidelines
  - Feature set determined by the system integrator
- Current specification is eDP2.0
  - Based on DP2.1
- No compliance program = Conformance Test!!



eDP2.0 Update

- eDP2.0 v1.0 published in September 2024
- Supports 128b/132b encoding
- Supports UHBR data rates
  - UHBR10, UHBR13.5 and UHBR20
- Leverages worst-case end-to-end link budget from DP2.1

Key Differences eDP2.0 vs DP2.1

Required

- DPCD registers for eDP
- Reduced AUX timing
- Enhanced framing
- Fast link training (sink)
- eDP-specific sink noise/jitter budget, reference EQ

Optional

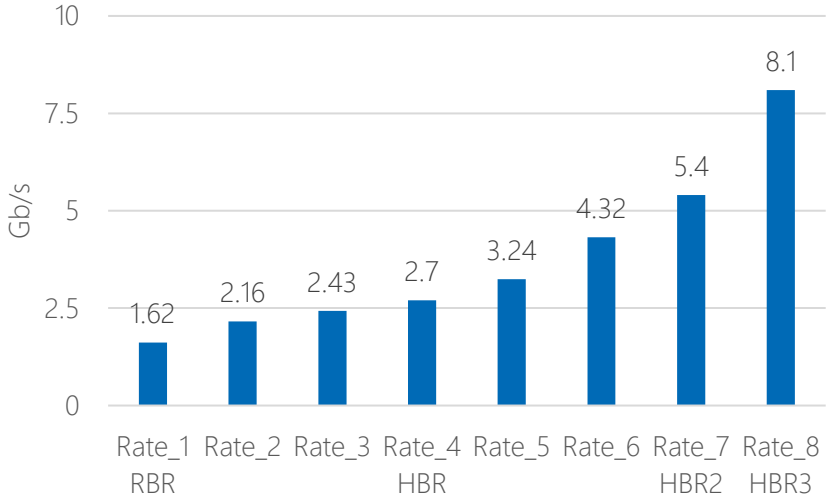
- Low AUX voltage swing
- Source detection by way of AUX CH
- STREAM_STATUS_CHANGED bits support
- GUID registers support
- Fast link training (host)
- Reduced main-link voltage swing level
- EDID
- HPD pin on sink device

Recommended

- Fewest number of lanes possible

Main Link Differences

- Eight 8b/10b rates, and Three UHBR rates
- Custom rates supported



- TP3_EQ total jitter budget
- BER = 10^{-9}

Test Point	Description	I/N	DJ_{MAX}	TJ_{MAX}
TP1	eDPTX package pin	Informative	0.17 UI	0.27 UI
TP2	Source device eDP cable connector	Informative	N/A	N/A
TP3	Sink device (panel) eDP cable connector	-	-	-
TP3_EQ	**After reference RX equalizer**	**Normative**	**0.41 UI**	**0.50 UI**
TP4	eDPRX package pins	Informative	0.46 UI	0.55 UI

AUX Channel Differences

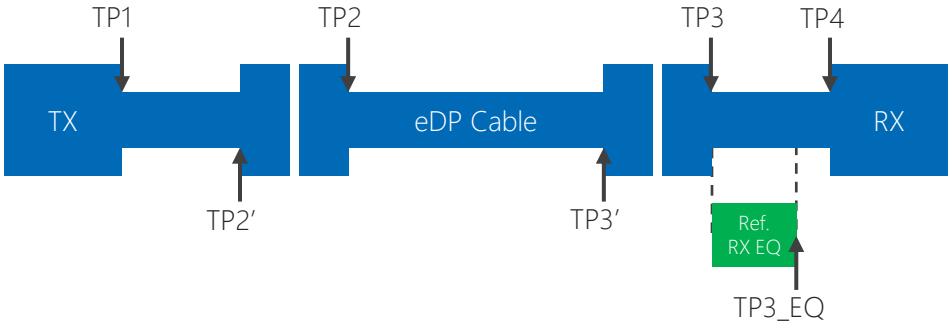
- No AC-coupling capacitors on Sink device side
- No pull-up/-down resistors
- Why?
  - The Sink device does not monitor the common mode voltage on AUX_CH_P and AUX_CH_N for Source device Hot Plug/Unplug and powered/unpowered detection

eDP Electrical Specification

- Low voltage swing levels
- Framework to apply optional customized voltage swings
- Reduced RX differential voltage sensitivity
- New transfer rates
- Framework to apply jitter specifications to optional customized frequencies
- Same Link Training procedures and voltage swing tables like DP, but with lower signal voltages

eDP Transmitter Test

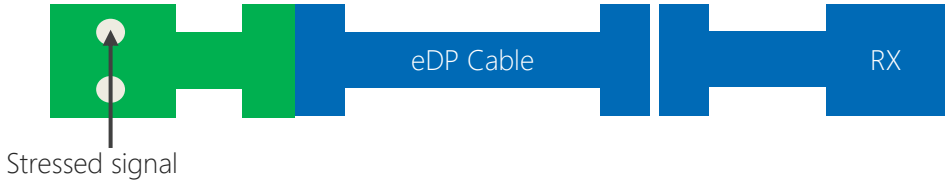
- Test Point/Fixture

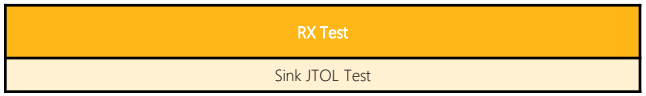


Recommended Source Main-Link TX Electrical Specification
Link Rate
Unit Interval
Total Jitter
Residual ISI
Non-ISI
Eye Diagram

eDP Receiver Test

- Test Point/Fixture





Calibration Point	RX Calibration
TP1	Sinusoidal Jitter Calibration
TP1	Random Jitter Calibration
TP3	Residual ISI
TP3	Eye Diagram
TP3	Crosstalk

VESA

Thank You!

VESA

Demo Tables

Poster x1

Demo Tester x1

GRL-C2-EPR

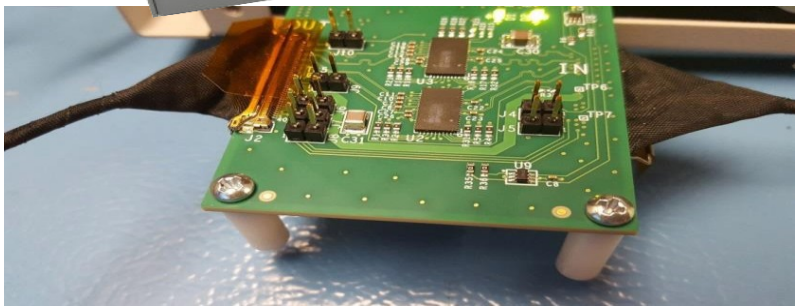
eDP and DisplayPort Protocol Analysis and Validation Real Time *ANY* Source to *ANY* Sink

FuturePlus Systems

Advancing Technology Development

NEW NEW

USB-C Power Delivery Analysis Software for DisplayPort Ask for a Demo!



eDP 1.4b and 1.5a, DP2.1
USB-C and DisplayPort
Probes
UHBR10, UHBR13.5
Up to 4 Lanes
Single Stream Transport and
Multi-Stream Transport
and more....

Something Special? We Like Challenges!

Accelerate Your High-Speed Digital Compliance Testing

KEYSIGHT

Measurement disaggregation solution

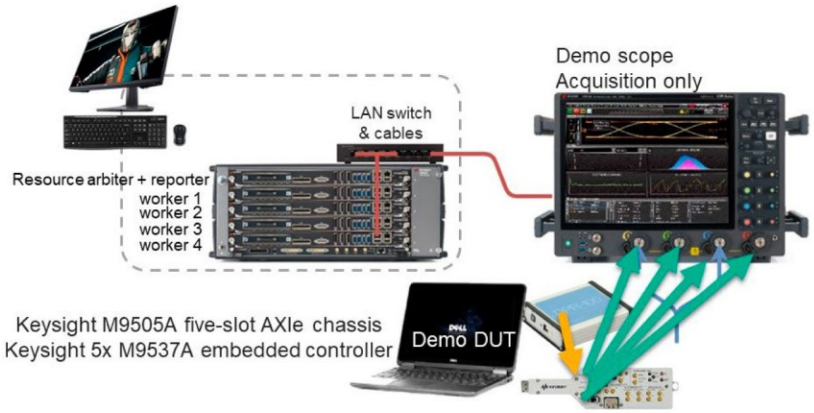


Figure 1. Keysight measurement disaggregation hardware setup

Summary

- Each new generation of high-speed computing standards includes more tests and factors to consider.
- Complex computations slow down overall throughput, and the acquisition hardware stays idle during the analysis.
- Measurement disaggregation offloads measurements and analysis to the cloud speeding up the overall test time.

For more information: Measurement Disaggregation

UNIGRAF

DisplayPort

USB Type-C

sales.asia@unigraf.fi

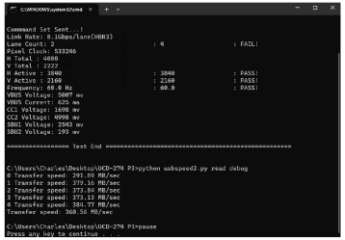
Unigraf DisplayPort and USB-C Test Solutions

UCD-500 Gen2

16K DP 2.1 Generator & Analyzer

- DP 2.1 Link Layer CTS Tool
- DP 2.1 Sinks and Sources up to 8K@60Hz (UHBR 20Gbps / Lane) and 16K@60Hz with DSC
- Featuring Link Analyzer, Panel Replay and eDP test functions

UTC-274



USB-C Test Automation Tool

- Test DP Alt Mode, Power Delivery and USB Speed
- Support EPR function up to 240W Source and Sink
- Test USB-C connector pins soldering and assembly quality with a single cable insertion





UNIGRAF

DisplayPort Alt Mode Compliance Testing and Analysis solutions

SYMBIOSYS ALLIANCE

Ellisys USB/DPAM Test and Analysis Solutions

USB Explorer™ 350

Multi-function USB Type-C®, USB 3.2, and Power Delivery Protocol Test Platform

VESA-Approved Tester for DisplayPort ALT Mode

Type-C Tracker™

Protocol and Electrical Analysis Tool for USB Type-C® Standards

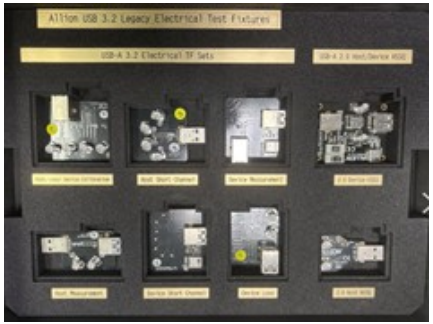
Includes DP AUX and DP ALT Support

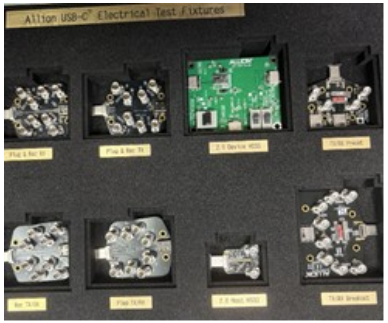
ellisys
Better Analysis

Allion Demo Table

- Test Fixtures
  - Designed for USB-C to (m)DP Cable Compliance Testing
  - Designed for USB 3.2 & USB-C Compliance Testing

- Brochures
  - PCIe 6.0 Test Fixture
  - USB 3.2 Test Fixture
  - DP/HDMI Test Fixture
  - C to DP/mDP Cable Test Fixture





Teledyne LeCroy
Test Solutions for DisplayPort v2.1

M42de 80G Video Analyzer/ Generator

TELEDYNE LECROY
Everywhereyoulook™

Teledyne LeCroy
7F., No. 667, Bannan Rd
Zhonghe Dist, New Taipei City 235
Taiwan
Phone: +886-2-8228-6100

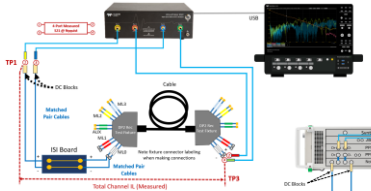
protocolsales@teledynelecroy.com

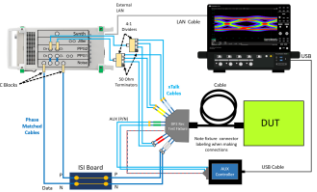
Teledyne LeCroy DisplayPort Test Platforms

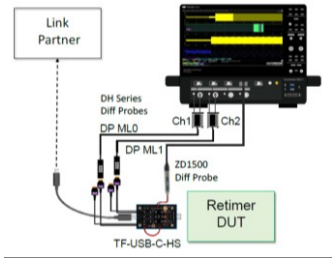
- **Quantumdata M42de Analyzer / Generator**
  - DisplayPort 1.4 & 2.1 (UHBR) Lane Rates
  - DP80 and USB Type-C® connectors
  - Deep Capture / Analysis
  - T.A.P.4™ Passive Monitoring
  - Comprehensive DP 1.4 & 2.1 Compliance Coverage
    - Link, DSC, LTTPR, EDID & MST
  - qdPrime™ Automated Test Suite

- **Quantumdata M21 Analyzer**
  - Portable DP Analyzer & HDMI Analyzer / Generator
  - DisplayPort Source Testing only (up to UHBR 13.5Gb/s)
  - AUX Channel Monitoring

DisplayPort 2.1 PHY Compliance and PHY-Logic Debug





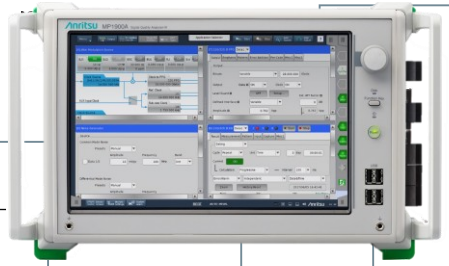


- DisplayPort 2.1 Source (Tx) Compliance
  - WaveMaster/SDA 8000HD with QualiPHY® 2 software
  - SDAX-DP expert analysis – Find Best CTLE/DFE
  - Reduced test times with QPHY2-PC
  - Automated Return Loss with WavePulser 40iX
- DisplayPort 2.1 Sink (Rx) Compliance
  - WaveMaster/SDA 8000HD with QualiPHY 2 software
  - SSG Cal and BER testing using Anritsu MP1900 SQA
  - Automated Channel Cal with WavePulser 40iX
- PHY-Logic (Interop) Debug
  - AUX Triggered + Main Link capture
  - TF-USB-C-HS – probing access
  - DP-AUX, USB-PD TDMP software
  - Clock switch testing on live link

MP1900A Signal Quality Analyzer
High Speed Bus SINK Compliance Solution

Anritsu
Advancing beyond

MP1900A Standalone
Multi-channel BER Measurement
High-quality PPG
High-input-sensitivity ED
PAM3/4 BER Measurements



Jitter Tolerance Test
SJ/RJ/BUJ Injection
Low-rate estimated BER measurement

Thunderbolt
4/5&DP1.4/2.1 Rx Test
Stressed Signal Calibration and
Stressed Signal Input Test

USB Link Sequence Generation
Transition to Loopback mode

Stressed Signal Calibration
PCI Express Link Sequence Generation
Transition to Loopback Mode
Pass/Fail evaluation using BER measurement

Calibration of stressed signal* → Transition DUT state to Loopback → Stressed Receiver Testing

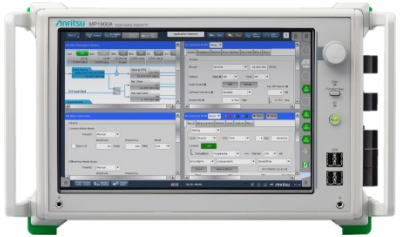
MX183000A Software

Stressed Signal Calibration*	USB Link Sequence Generation Function PCI Express Link Sequence Generation Function	Stressed Signal Input Test Function Jitter Tolerance Test Auto-receiver Test Function

MP1800A Hardware

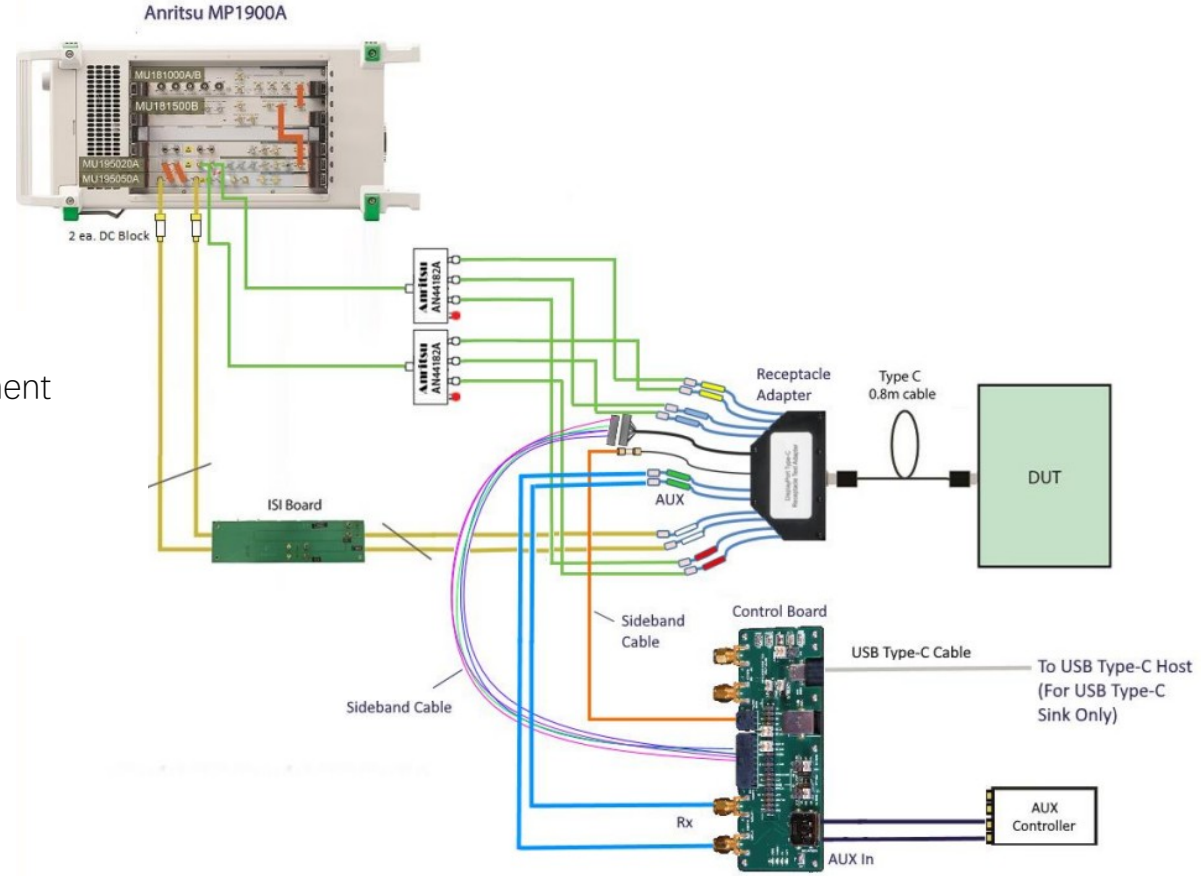
Up to 32 Gbit/s, 8ch	High Quality Signal	Jitter Emphasis

MP1900A Signal Quality Analyzer
DP1.4/2.1 SINK Compliance Test Structure



MP1900A Standalone

- Multi-channel BER Measurement
- High-quality PPG
- High-input-sensitivity ED
- PAM3/4 BER Measurements
- DP1.4/2.1 and USB4v1&v2 Compliance test Support



Lunch

DP Alt Mode v 2.1a Overview and Updates

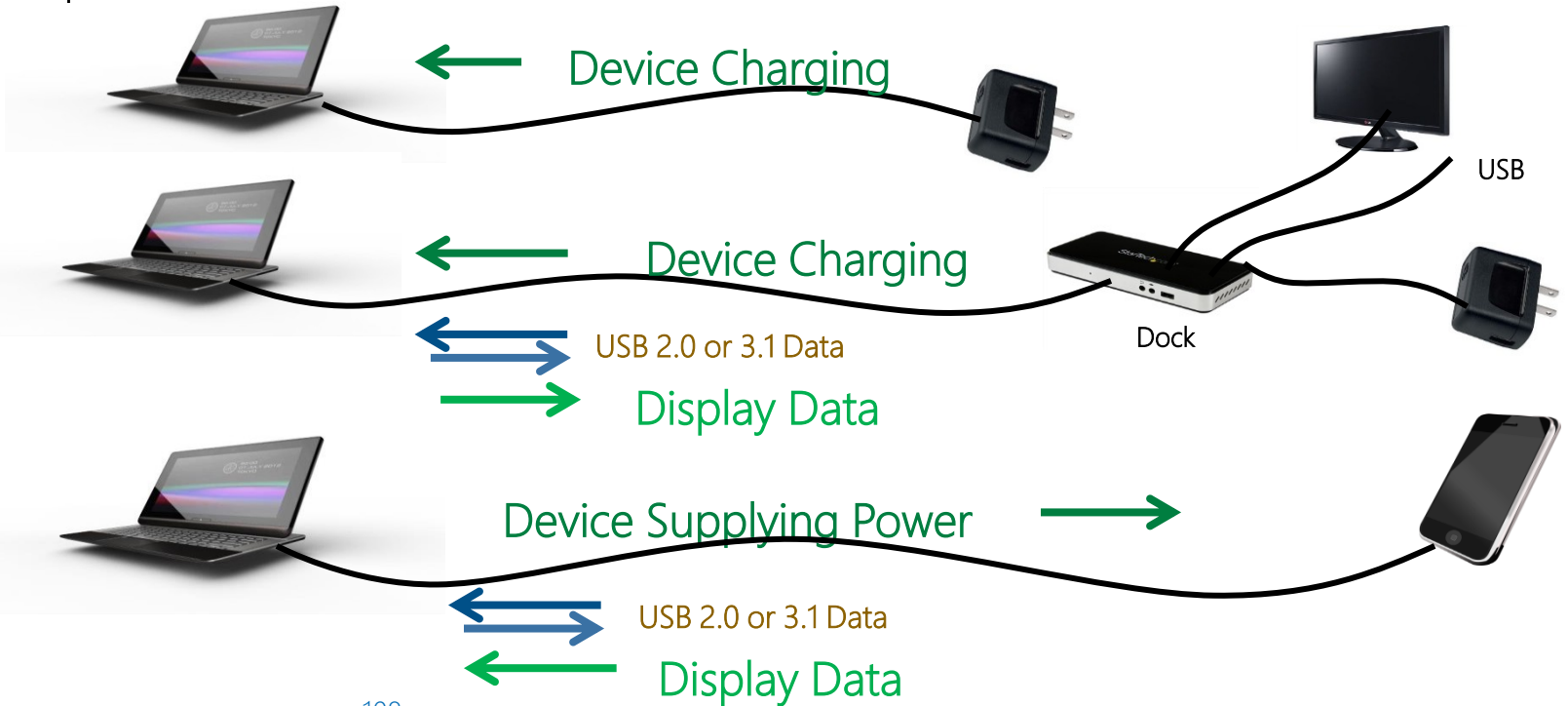
Tim Wei– Senior Application Engineer

Ellisys

Oct 28, 2025

Example USB Type-C Configurations

Either end can serve as USB Host, USB-PD Power Consumer, and DisplayPort Video Source (these services are independent of each other



DP Alt Mode over USB-C Ecosystem is Mainstream


USB-C Tablets


USB-C Laptops


USB-C Displays


Multi Function Adapters

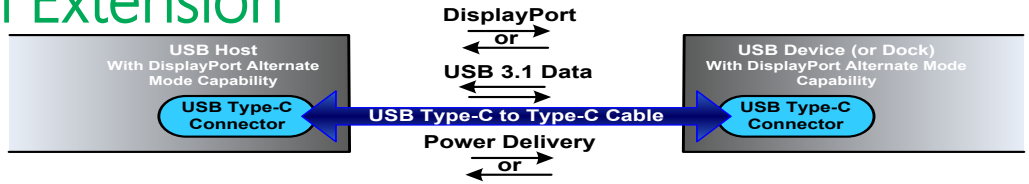
All types of certified adapters available

- C to DP adapters, Multifunction docks
- Type C protocol converters (HDMI, VGA, DVI) using DP Alt Mode

More are certified every week

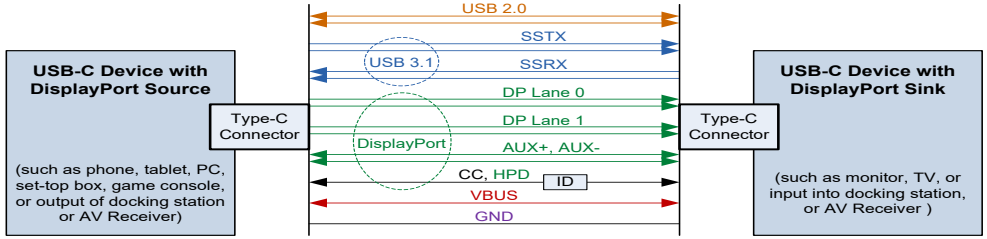
- Major PC OEMs continue to launch new products with DP Alt Mode over USB-C
- Major Display OEMs continue to add USB-C inputs to their products

USB-C Connector Functional Extension DP Alt Mode



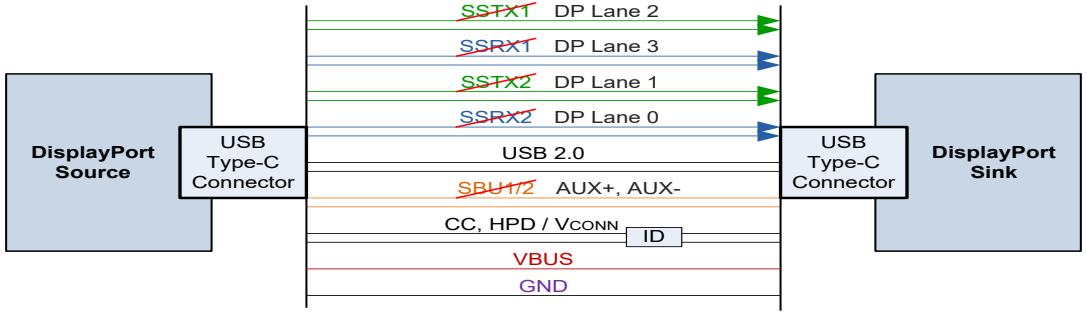
- A passive Full Feature USB Type-C to Type-C cable can carry up to four DisplayPort lanes
  - Same performance and features as a standard DisplayPort connection
  - Allows DisplayPort data rates to increase in the future, since the USB Type-C connector has very high data rate capability
- DisplayPort can be combined with USB 3.2 operation over the same USB Type-C cable
- USB 2.0 and USB Power Delivery is available in all configurations

2xDisplayPort and USB 3.2 over a Standard USB-C Cable



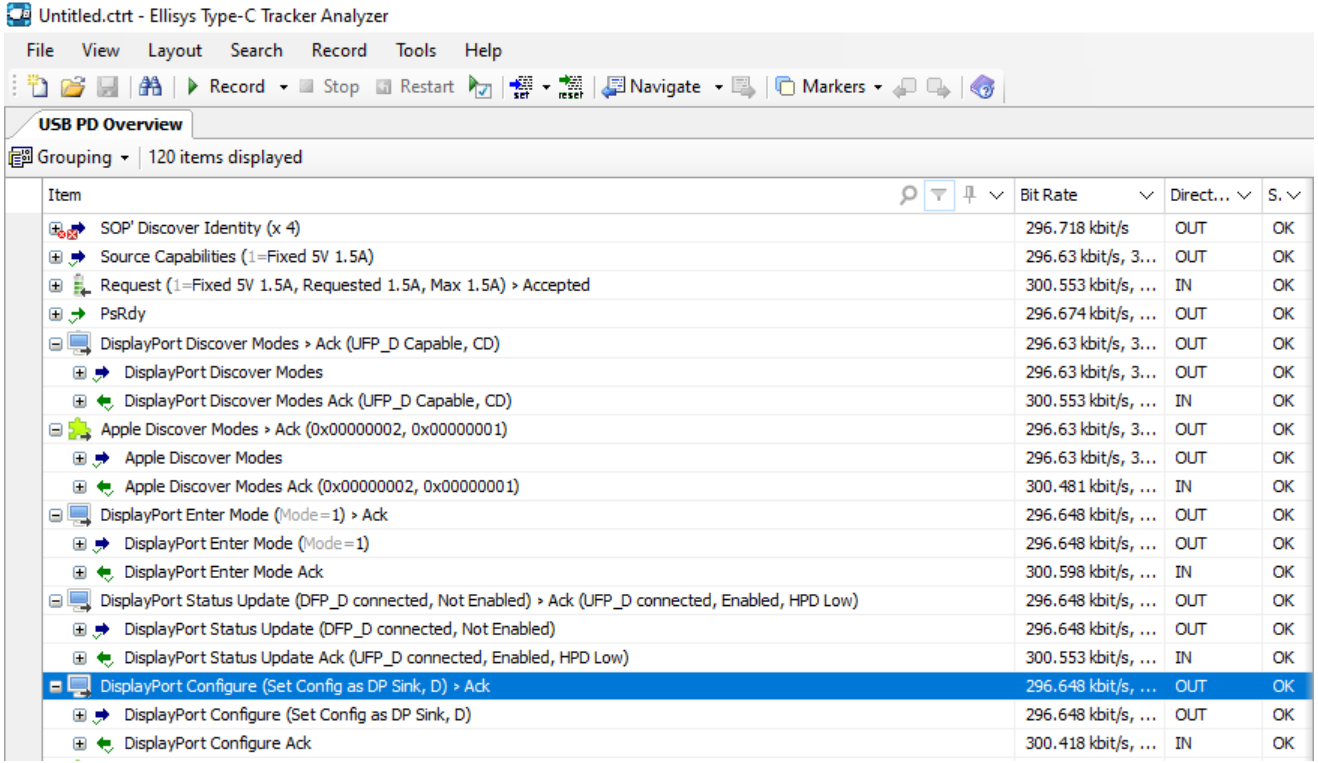
- Uses a standard “Full Feature” USB-C to USB-C cable which is designed to include DisplayPort
- The above configuration uses two high-speed lanes each for DisplayPort and USB 3.2
  - Ideal for docking stations, or for displays or TVs that include USB 3.2 functions
- DisplayPort performance provided by two lanes
  - HBR3: 4K(3840x2160)@60fps 24bpp
  - UHBR20: 8K (7680x4320)@30fps 30bpp

4xDP Over a USB Type-C to USB Type-C Full Feature Passive Cable



- Utilizes optional DP Alt Mode capability of USB Type-C connector
- DisplayPort can use all four high speed lanes to deliver full DisplayPort performance
- The DisplayPort AUX Channel uses the SBU pins
- The DisplayPort HPD / IRQ is transmitted over the CC pin using the USB-PD protocol
- USB 2.0 and USB Power Delivery always available
- DisplayPort performance provided by four lanes
  - HBR3: 5K (5120x2800)@60fps 24bpp
  - UHBR20: 10K (10240x4320)@60fps 24bpp

Typical DisplayPort Alternate Mode Flow



Item	Bit Rate	Direct...	S.
SOP' Discover Identity (x 4)	296.718 kbit/s	OUT	OK
Source Capabilities (1=Fixed 5V 1.5A)	296.63 kbit/s, 3...	OUT	OK
Request (1=Fixed 5V 1.5A, Requested 1.5A, Max 1.5A) › Accepted	300.553 kbit/s, ...	IN	OK
PsRdy	296.674 kbit/s, ...	OUT	OK
DisplayPort Discover Modes › Ack (UFP_D Capable, CD)	296.63 kbit/s, 3...	OUT	OK
DisplayPort Discover Modes	296.63 kbit/s, 3...	OUT	OK
DisplayPort Discover Modes Ack (UFP_D Capable, CD)	300.553 kbit/s, ...	IN	OK
Apple Discover Modes › Ack (0x00000002, 0x00000001)	296.63 kbit/s, 3...	OUT	OK
Apple Discover Modes	296.63 kbit/s, 3...	OUT	OK
Apple Discover Modes Ack (0x00000002, 0x00000001)	300.481 kbit/s, ...	IN	OK
DisplayPort Enter Mode (Mode=1) › Ack	296.648 kbit/s, ...	OUT	OK
DisplayPort Enter Mode (Mode=1)	296.648 kbit/s, ...	OUT	OK
DisplayPort Enter Mode Ack	300.598 kbit/s, ...	IN	OK
DisplayPort Status Update (DFP_D connected, Not Enabled) › Ack (UFP_D connected, Enabled, HPD Low)	296.648 kbit/s, ...	OUT	OK
DisplayPort Status Update (DFP_D connected, Not Enabled)	296.648 kbit/s, ...	OUT	OK
DisplayPort Status Update Ack (UFP_D connected, Enabled, HPD Low)	300.553 kbit/s, ...	IN	OK
DisplayPort Configure (Set Config as DP Sink, D) › Ack	296.648 kbit/s, ...	OUT	OK
DisplayPort Configure (Set Config as DP Sink, D)	296.648 kbit/s, ...	OUT	OK
DisplayPort Configure Ack	300.418 kbit/s, ...	IN	OK

DisplayPort Alternate Mode 2.1 Update

- SVDM Header Update (by USB PD Spec)
- Cable DP Capabilities VDO update to support UHBR20 and UHBR13.5
  - Both passive and active cables
- SOP' Active Cable DisplayPort Configurations VDO update
- DP Capabilities VDO Update (DPAM Version field)
- SOP DisplayPort Configurations VDO Update
  - Cable information
  - DPAM Version
- DisplayPort Status Update VDO Update

SVDM Header Update

12:11	**Structured VDM Version (Minor)[a]**	Version number (Minor) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier 01b = Version 2.1 All other values are RESERVED.
14:13	**Structured VDM Version (Major)[a]**	Version number (Major) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier. 01b = Version 2.x. (x indicates SVDM minor version) All other values are RESERVED.

12:11 was reserved

Cable DP Capabilities VDO update

Table 4-5: SOP' Cable DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)[a]

Bit(s)	Description	Values
1:0	**RESERVED**	RESERVED (always 00b).
5:2	**Signaling for Transport of DisplayPort Protocol[b]**	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[c]
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**DP Source Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported. 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
23:16	**DP Sink Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
25:24	**RESERVED**	RESERVED (always 00b).
26[d]	**UHBR13.5**	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[c]
27	**RESERVED**	RESERVED (always 0).
29:28[d]	**Active Component**	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30	**DPAM Version**	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 4-2: Active Cable DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)

Bit(s)	Description	Values
1:0	RESERVED	RESERVED (always 00b).
5:2	Signaling for Transport of DisplayPort Protocol[a]	XXX1b = Supports *DP* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	DP Source Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported. All other values are RESERVED.
23:16	DP Sink Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). All other values are RESERVED.
31:24	RESERVED	RESERVED (always 00h).

a. "X" value indicates "Don't Care."

Active Cable DisplayPort Configurations VDO update

Table 4-7: SOP' Active Cable DisplayPort Configurations

Bit(s)	Description	Values
1:0	**Select Configuration**	00b = Set configuration for *USB*.[a] 01b = Set configuration for active cable as a *DP* Source device (UFP_U is a *DP* Source device).[b] 10b = Set configuration for active cable as a *DP* Sink device (UFP_U is a *DP* Sink device).[b] 11b = RESERVED.
5:2	**Signaling for Transport of DisplayPort Protocol**	0h = Bit rate is unspecified (used only when the Select Configuration field is programmed for USB Configuration). 1h = Select *DP* bit rates and electrical settings. All other values are RESERVED.
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**Configure Active Cable Pin Assignment**	00h = Deselect pin assignment. 04h = Select Pin Assignment C.[c] 08h = Select Pin Assignment D.[d] 10h = Select Pin Assignment E.[e] All other values are RESERVED.
31:16	**RESERVED**	RESERVED (always 0000h).

Table 4-4: Active Cable DisplayPort Configurations

Bit(s)	Description	Values
1:0	Select Configuration	00b = Set configuration for *USB*.[a] 01b = Set configuration for active cable as a *DP* Source device (UFP_U is a *DP* Source device).[b] 10b = Set configuration for active cable as a *DP* Sink device (UFP_U is a *DP* Sink device).[b] 11b = RESERVED.
5:2	Signaling for Transport of DisplayPort Protocol	0h = Bit rate is unspecified (used only when the Select Configuration field is programmed for USB Configuration). 1h = Select *DP* bit rates and electrical settings. All other values are RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	Configure Active Cable Pin Assignment	00h = De-select pin assignment. 04h = Select Pin Assignment C.[c] 08h = Select Pin Assignment D.[d] All other values are RESERVED.
31:16	RESERVED	RESERVED (always 0000h).

No Pin Assignment E

DP Capabilities VDO Update

Table 5-6: DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	**Port Capability**	00b = RESERVED. 01b = *DP* Sink Device Capable (including *DP* Branch device). 10b = *DP* Source Device Capable (including *DP* Branch device). 11b = Both *DP* Source and Sink Device Capable.
5:2	**Signaling for Transport of DisplayPort Protocol**	XXX1b = Supports *DP* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	**Receptacle Indication**	0 = *DP* interface is presented on a *USB-C* plug. 1 = *DP* interface is presented on a *USB-C* receptacle.
7	**USB 2.0 Signaling Not Used**	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	**DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)**	00000000b = *DP* Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	**DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)**	00000000b = *DP* Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
29:24	**RESERVED**	RESERVED (always 00h).
31:30	**DPAM Version[i]**	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 5-5: DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED. 01b = *DP* Sink device-capable (including *DP* Branch device). 10b = *DP* Source device-capable (including *DP* Branch device). 11b = Both *DP* Source and Sink device-capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = *DP* interface is presented on a *USB-C* plug. 1 = *DP* interface is presented on a *USB-C* receptacle.
7	USB 2.0 Signaling Not Used	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	DP Source Device Pin Assignments Supported (reported by a *DP* Source device receptacle or *DP* Sink device (direct-attach) plug)	00000000b = *DP* Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a *DP* Sink device receptacle or *DP* Source device (direct-attach) plug)	00000000b = *DP* Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
31:24	RESERVED	RESERVED (always 00h).

If SVDM Version is 2.1 or higher, DPAM Version field is applicable else this field shall be set to 00b.

A Bit More Background

From DisplayPort Alt Mode 2.0 Spec

Future versions of this Standard may describe other modes associated with the DP_SID. Such modes shall be identified by having a non-zero value in bits 31:24 of the VDO. The DFP_U shall examine the list of modes returned until it finds 0s in bits 31:24 of the VDO and a non-zero value in bits 23:0 of the VDO (i.e., DP Capabilities). The DFP_U and UFP_U shall use the corresponding offset (indexed from 1) as the Object Position in the following commands:

SOP DisplayPort Configurations VDO Update

Table 5-13: SOP DisplayPort Configurations

Bit(s)	Description	Values
1:0	**Select Configuration**	00b = Set configuration for *USB*.[a] 01b = Set configuration for UFP_U as a *DP* Source device.[b] 10b = Set configuration for UFP_U as a *DP* Sink device.[b] 11b = RESERVED.
5:2[c]	**Signaling for Cable Information Transport of DisplayPort Protocol**	XXX1b = Supports all defined *DP* bit rates up to HBR3 -or- capability is unknown XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[d]
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**Configure UFP_U Pin Assignment**	00h = Deselect pin assignment. 04h = Select Pin Assignment C.[e] 08h = Select Pin Assignment D.[f] 10h = Select Pin Assignment E.[g] All other values are RESERVED.
25:16	**RESERVED**	RESERVED (always 0000000000b).
26[h]	**Cable UHBR13.5 Support**	0 = Not supported.[i] ~~-or- capability is unknown~~ 1 = Supported.
27	**RESERVED**	RESERVED (always 0).
29:28[h]	**Cable Active Component**	00b = Passive -or- cable type is unknown 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30[j]	**DPAM Version**	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Table 5-8: DisplayPort Configurations

Bit(s)	Description	Values
1:0	Select Configuration	00b = Set configuration for *USB*.[a] 01b = Set configuration for UFP_U as a *DP* Source device.[b] 10b = Set configuration for UFP_U as a *DP* Sink device.[b] 11b = RESERVED.
5:2	Signaling for Transport of DisplayPort Protocol	0h = Bit rate is unspecified (used only when the Select Configuration field is programmed for USB Configuration). 1h = Select *DP* bit rates and electrical settings. All other values are RESERVED.
7:6	RESERVED	RESERVED (always 00b).
15:8	Configure UFP_U Pin Assignment	00h = De-select pin assignment. 04h = Select Pin Assignment C.[c] 08h = Select Pin Assignment D.[d] 10h = Select Pin Assignment E.[e] All other values are RESERVED.
31:16	RESERVED	RESERVED (always 0000h).

- This is the most challenging part for DPAM 2.1 DFP_U

DisplayPort Status Update VDO Update

Table 5-7: DisplayPort Status Update

Bit(s)	Description	Values
1:0	**DP Source/Sink Device Connected**	00b = Neither a *DP* Source device nor *DP* Sink device is connected, –or– the adapter is disabled. 01b = *DP* Source device is connected. 10b = *DP* Sink device is connected.[a] 11b = Both a *DP* Source and Sink device are connected.
2[b]	**Power Low**	0 = Adapter is not in low power state ~~is functioning normally or is disabled~~. 1 = Adapter has detected low power ~~and disabled *DP* support~~.
3[b]	**Enabled**	0 = Adapter *DP* functionality is disabled. 1 = Adapter *DP* functionality is enabled and operational.
4[d]	**Multifunction Preferred**	0 = No preference for multifunction. 1 = Multifunction is preferred.
5[c]	**DisplayPort/ USB Configuration Request**	0 = Request change to DisplayPort Configuration (if currently in USB Configuration). 1 = Request change to USB Configuration (if currently in DisplayPort Configuration).
6[c]	**Exit DisplayPort Alt Mode Request**	0 = Maintain the current mode. 1 = Request exit from DisplayPort Alt Mode (if currently in DisplayPort Alt Mode).
7[d]	**HPD State**	0 = HPD_Low. 1 = HPD_High.[e]
8[d]	**IRQ_HPD**	0 = IRQ_HPD has not been issued since the last status Message. 1 = IRQ_HPD.[f]
9[g]	**NO_DPAM_SUSPEND**	0 = UFP_U/ DP Sink device has no preference for entry into low power state. 1 = UFP_U/ DP Sink device prefers not to enter low power state.
31:10	**RESERVED**	RESERVED (always 0000000h).

Table 5-6: *DisplayPort Status Update*

Bit(s)	Description	Values
1:0	DP Source/Sink Device Connected	00b = Neither a *DP* Source device nor *DP* Sink device is connected, –or– the adapter is disabled. 01b = *DP* Source device is connected. 10b = *DP* Sink device is connected.[a] 11b = Both a *DP* Source and Sink device are connected.
2[b]	Power Low	0 = Adapter is functioning normally or is disabled. 1 = Adapter has detected low power and disabled *DP* support.
3[b]	Enabled	0 = Adapter *DP* functionality is disabled. 1 = Adapter *DP* functionality is enabled and operational.
4[b]	Multi-function Preferred	0 = No preference for multi-function. 1 = Multi-function is preferred.
5[b]	DisplayPort/ USB Configuration Request	0 = Request change to DisplayPort Configuration (if currently in USB Configuration). 1 = Request change to USB Configuration (if currently in DisplayPort Configuration).
6[b]	Exit DisplayPort Alt Mode Request	0 = Maintain the current mode. 1 = Request exit from DisplayPort Alt Mode (if currently in DisplayPort Alt Mode).
7[c]	HPD State	0 = HPD_Low. 1 = HPD_High.[d]
8[c]	IRQ_HPD	0 = IRQ_HPD has not been issued since the last status Message. 1 = IRQ_HPD.[e]
31:9	RESERVED	RESERVED (always 0000000h).

DPAM Version Resolution

Table 5-5: DPAM Version Resolution

DFP_U, Cable and UFP_U with DP SID	DFP_U	Cable	UFP_U	DPAM Version Resolution
DPAM Version	2.0 or earlier	2.0 or earlier	2.0 or earlier	2.0 or earlier[ab]
	2.1 or higher	2.0 or earlier	2.0 or earlier	2.0 or earlier[ab]
	2.0 or earlier	2.1 or higher	2.0 or earlier	2.0 or earlier[ab]
	2.0 or earlier	2.0 or earlier	2.1 or higher	2.0 or earlier[ab]
	2.1 or higher	2.1 or higher	2.0 or earlier	2.0 or earlier[ab]
	2.0 or earlier	2.1 or higher	2.1 or higher	2.0 or earlier[ab]
	2.1 or higher	2.0 or earlier	2.1 or higher	DPAM 2.1 or higher[c]
	2.1 or higher	2.1 or higher	2.1 or higher	2.1 or higher[d] (Shall support DPAM 2.1 or higher)

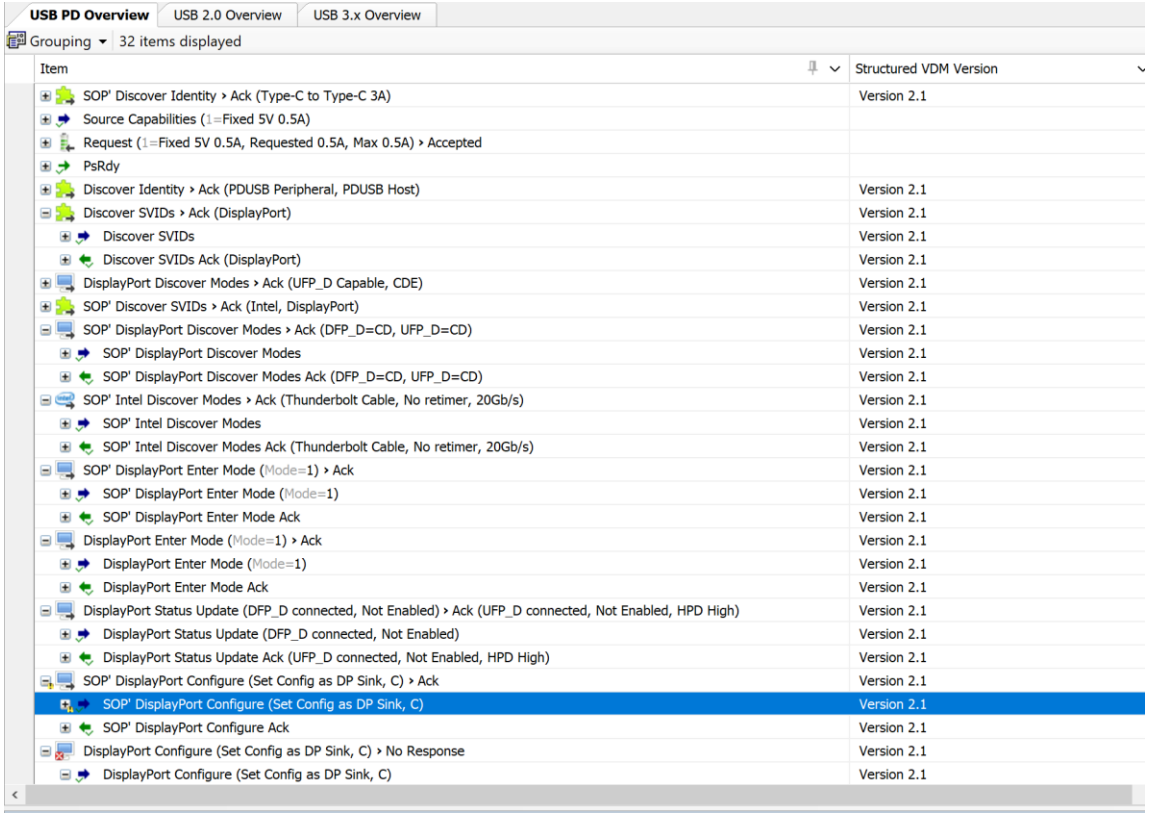
a. *If Initiator and Responder support SVDM Version 2.0 or earlier and if DisplayPort Alternate Mode is supported all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.0 or earlier.*

b. *If Initiator and Responder both support SVDM Version 2.1 or higher and if either Initiator or Responder supports DPAM Version 2.0 or earlier, then all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.0 or earlier.*

c. *When DPAM 2.1 or higher DFP_U and DPAM 2.1 or higher UFP_U are connected with a legacy active DPAM 2.0 cable, then the system shall exchange all DP Capabilities as per DisplayPort Alt Mode on USB Type-C specification 2.1 or higher but support HBR3 rates.*

d. *If Initiator and Responder both support SVDM Version 2.1 or higher and DPAM Version 2.1 all DP Capabilities exchange shall follow DisplayPort Alt Mode on USB Type-C specification 2.1 or higher.*

Typical DPAM 2.1 Flow



DisplayPort Alternate Mode 2.1a Update

- **DisplayPort Alt Mode v2.1a_SCR_on_Clarification on Device Types**
- **DisplayPort Alt Mode v2.1a_SCR_on_CableSupport**
- **DisplayPort Alt Mode v2.1a_SCR_on_Depricating DP40 Cables**
- **DisplayPort Alt Mode v2.1a_SCR_on_tAttentionToDPConfigure time**
- **DisplayPort Alt Mode v2.1a_SCR_on_mandatory PD Message support for DPAM2.1 Cables**

DisplayPort Alt Mode v2.1a_SCR_on_Clarification on Device Types

Table 5-1 USB-C and USB PD Power and Data Roles

12	USB-C-to-DP receptacle	V_{CONN}-powered accessory (Rd/Ra)	No	DFP_U and UFP_U	No Preference	Never VCONN Source
13	USB-C-to-DP cable adapter	V_{CONN}-powered accessory (Rd/Ra)	No	DFP_U and UFP_U	No Preference	Never VCONN Source

Table 5-2 USB PD Data Role Policies

Prefer UFP_U	Issue a *USB PD* ***DR_Swap*** Message to become a UFP_U If the *USB PD* ***DR_Swap*** Message is rejected, and port results in a DFP_U role, the port shall be responsible for discovering and initiating Alternate Mode entry

DisplayPort Alt Mode v2.1a_SCR_on_CableSupport

Table 5-15: DP Rates for TBTSID Capable cables

Cable Type	SVDM Version	DPAM Version	DP SID	TBT SID	TBT Alt Mode Response (see Appendix F of USB-C specification)			DP Alt Mode Response (see Table 4-5)	SOP DP Configure (see Table 5-13)	
					B25	B22	B[18:6]	B[5:2], B26 & B[29:28]	B[5:2]	B[29:28]
2,3 (See Table 2-1)	2.0	NA	No	Yes	0	0 Not Re-timer	001b, 010b or 011b	NA	001b or 010b = UHBR10 011b = UHBR20	00b
4 (See Table 2-2)	2.0	NA	No	Yes	Don't care	1 Re-timer		NA	No DP	NA

Note: If cable supports both DPSID and TBTSID, TBT VDO Bit 22 and Bit 25 can be used by the DP Source to determine the cable type (Passive, Re-driven, or Re-timed).

DisplayPort Alt Mode v2.1a_SCR_on_Depricating DP40 Cables

Reference Number in Tables 2-4	Cable Type	Minimum DP Bit-rate Capability[a]	DisplayPort Alt Mode Directionality and Main-Link Lane-count Capability[a]	Certification and Logo Applicability
1	Full-Featured Passive *USB-C USB 3.2* Gen 1 Cables (*USB-C* CC3G1-X)	HBR3[b] UHBR10[b]	Reversible 4 Lanes	*USB* certification and logo only **No VESA certification or logo**
2	Full-Featured Passive *USB-C USB 3.2* and *USB4* Gen 2 Cables and Thunderbolt Alt Mode Gen 2 Cables (*USB-C* CC3G2-X)	UHBR10 (DP54) UHBR13.5[d] (DP54)		
3	Full-Featured Passive *USB-C USB4* Gen 3 (or higher) Cables and Thunderbolt Alt Mode Gen 3 (or higher) Cables (*USB-C* CC4G3-X)	UHBR20[c] (DP80)		

DisplayPort Alt Mode v2.1a_SCR_on_tAttentionToDPConfigure time

1. Table 1-5 Glossary

Term	Definition
tAttentionToDPConfigure	Time between reception of USB PD Attention to transmission of DisplayPort Configure Message, this time is set to 500 ms. This time is applicable to DFPs in active state and functioning normally.

- **Port is a DFP_U in DisplayPort Alt Mode and DisplayPort Configuration** – Port shall change to USB Configuration by issuing an appropriate ***DisplayPort Configure*** Command to both the UFP_U and cable within *tAttentionToDPConfigure* time after receiving a *USB PD* ***Attention*** Command request with the DisplayPort/USB Configuration Request bit (bit 5) set to 1 in the ***DisplayPort Status Update*** (refer Table 5-7)
- **Port is a DFP_U in DisplayPort Alt Mode and USB Configuration** – Port shall change to an appropriate DisplayPort Configuration by issuing an appropriate ***DisplayPort Configure*** Command to both the UFP_U and cable within *tAttentionToDPConfigure* time after receiving a *USB PD* ***Attention*** Command request with the DisplayPort/USB Configuration Request bit cleared to 0 (refer Table 5-7)

DisplayPort Alt Mode v2.1a_SCR_on_mandatory PD Message support for DPAM2.1 Cables

Table 4-1: Cable eMarking Mandates

Reference Number in Tables 2-4	Cable Type	*USB PD Discover Identity*	DisplayPort Alt Mode *USB PD* Commands
1	Full-Featured Passive *USB-C USB 3.2* Gen 1 Cables (*USB-C* CC3G1-X)	Mandatory	Not Allowed
6	Captive Cable with *USB-C* connector	Mandatory When the DP Sink supports UHBR rates	**Optional** When the DP Sink supports HBR rates

DPAM 2.1 CTS Update - 1

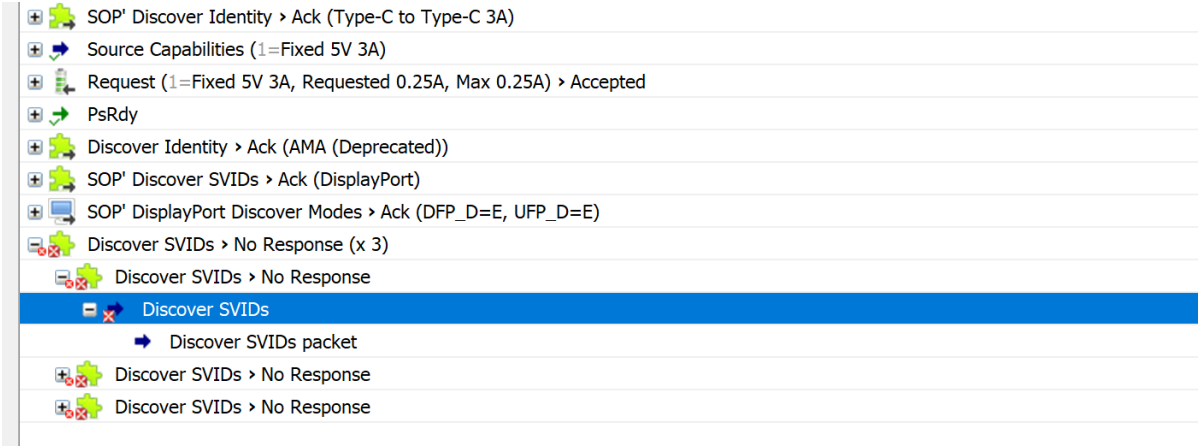
- 10.3.2 DPAM2.1 Entry with USB-C to USB-C non-emarked cable
- 10.3.3 DPAM2.1 Entry with USB-C to USB-C Passive TBT3 cable
- 10.3.4 DPAM2.1 Entry with Passive E-Marked USB-C to USB-C
- 10.3.5 DPAM2.1 Entry with USB-C to USB-C DP2.0 LRD Cable
- 10.3.6 DPAM2.1 Entry with USB-C to USB-C DP2.0 Active Retimer cable
- 10.3.7 DPAM2.1 Entry with USB-C to USB-C DP2.1 LRD cable
- 10.3.8 DPAM2.1 Entry with USB-C to USB-C Active Non-DP cable
- 10.3.9 DPAM2.1 Entry with USB-C to USB-C USB2.0 cable
- 10.3.10 DPAM2.1 Entry with USB-C to DP2.1 cable

- Make sure the DFP_U set correct cable information in DisplayPort Configurations VDO
- 10.3.5 and 10.3.6 Using TBT info is now optional (was mandatory)

DPAM 2.1 CTS Update - 2

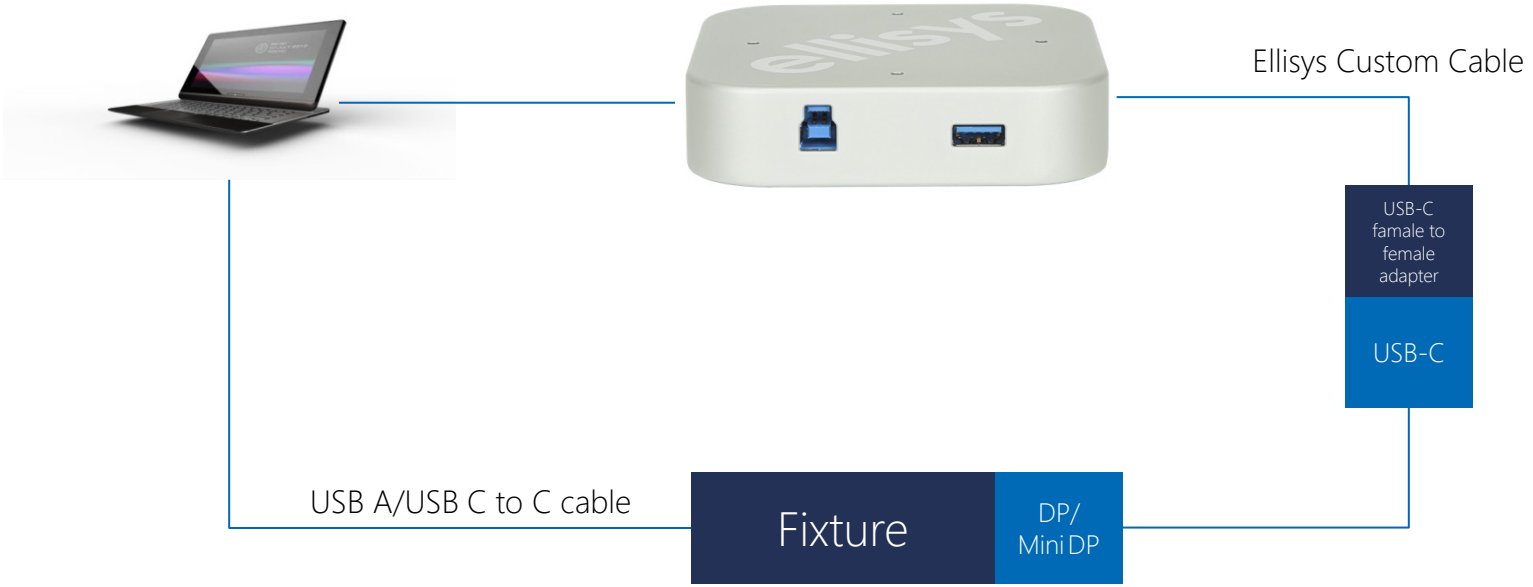
- **DPAM Version Resolution Tests**
  - **10.3.23 DPAM Version 2.1 DFP_U Connected to DPAM Version 2.0 or 2.1 UFP_U**
  - **10.4.3 DPAM Version 2.1 Cable Connected to DPAM Version 2.0 or 2.1 DFP_U**
  - **10.2.8 DPAM Version 2.1 UFP_U Connected to DPAM Version 2.0 or 2.1 DFP_U**

- **10.2.9 DPAM Discovery Interoperability Flow for UFPs**



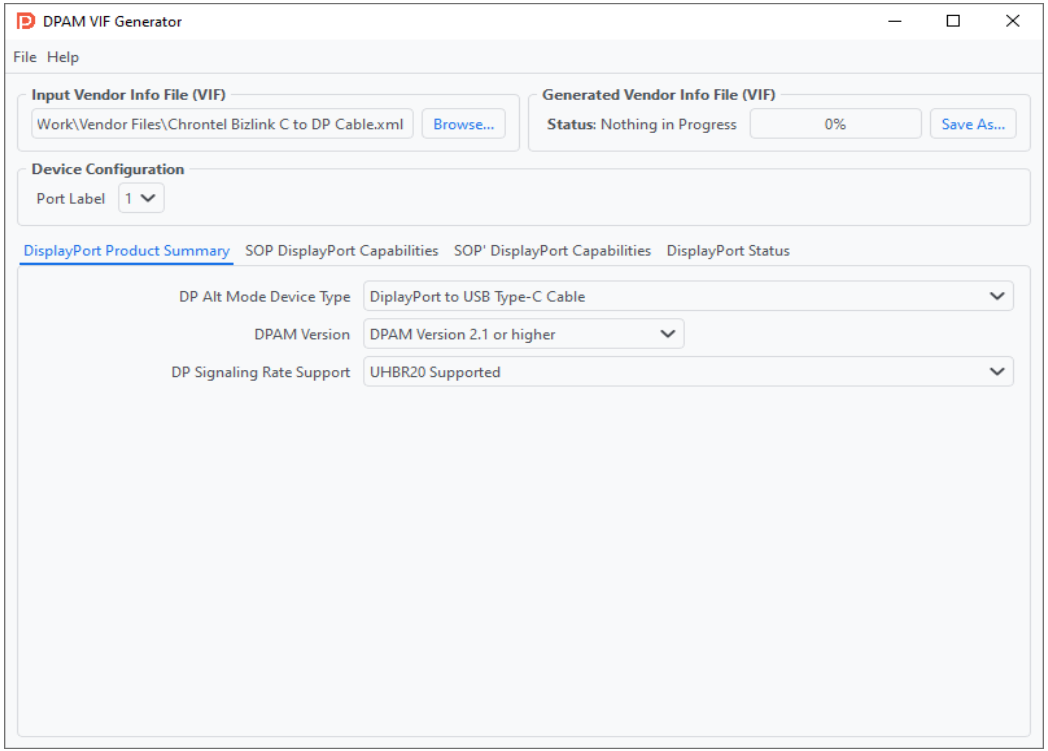
DPAM 2.1 CTS Update - 3

- **C to DP Adapter tests automation**



DPAM 2.1 CTS Update - 4

- **VESA VIF TOOL**



Ellisys USB Test and Analysis Solutions

USB Explorer™ 350

Multi-function USB Type-C®, USB 3.2, and Power Delivery Protocol Test Platform

VESA-Approved Tester for DisplayPort ALT Mode

Type-C Tracker™

Protocol and Electrical Analysis Tool for USB Type-C® Standards

Includes DP AUX and DP ALT Support

ellisys
Better Analysis

DisplayPort Alternate Mode 2.1b Upcoming

- **C to DP cable shall support DFP role**
- **C to DP cable pin assignment mandatory (Pin E required, Pin C optional, Pin D forbidden)**
- **Cable Attributes update**
- **Data Role clarification (cannot rely on DR_Swap being successful)**
- **DP80LL Loss Budget Supported bit**

Questions?


DisplayPort over USB-C
The most advanced display connection now uses the most versatile connector.
Learn More
Go to www.displayport.org

DP2.1 Panel Replay and Advanced Link Power Management: Implementation and Testing Challenges

Marco Denicolai
Unigraf Oy
October 2025

Agenda

- Saving power with Panel Replay (PR)
- Saving power with Advanced Link Power Management (ALPM)
- Interaction with FEC, MST and HDCP

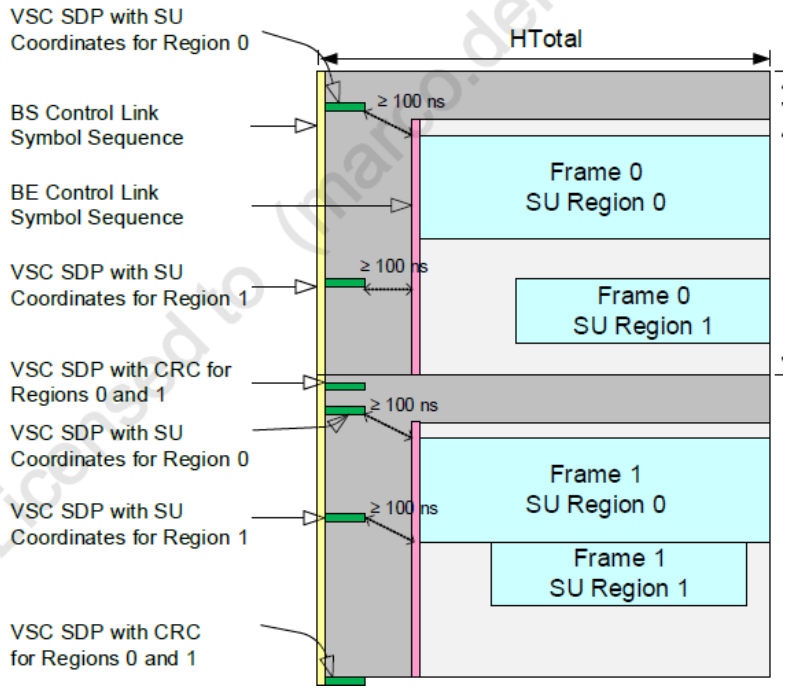
The Devil is in the details…

DisplayPort system-level power conservation

- Optional Panel Replay (PR) can be enabled to turn the Main Link off when no data is being transferred and save power.
- When PR is in Active state, the Sink will use the image captured in its Remote Frame Buffer (RFB) to refresh the display.
- During PR Active state, the Source can either continue to transmit a frame-rate-governed video timing (discarded by the Sink) or, optionally, turn the Main Link off.
- Optional Main Link power on/off management uses Advanced Link Power Management (ALPM) in AUX-less mode.

Panel Replay overview

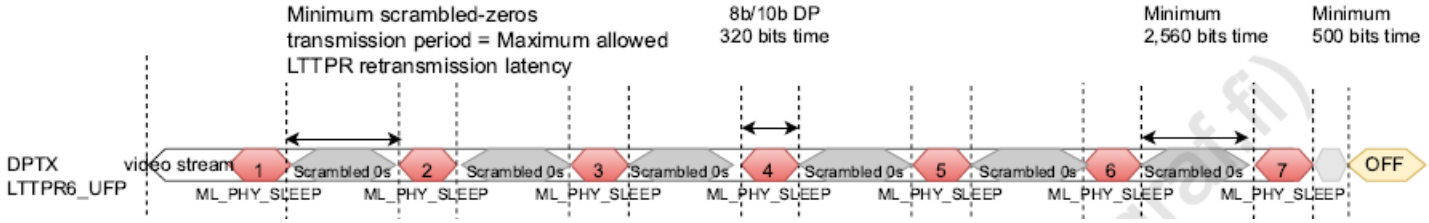
- Transitions between Live Frame mode and PR Active state happen using VSC SDPs.
- The Source can transmit a Full Frame update, or one or more smaller Selective Update (SU) Regions, each starting at their respective video scan line position.
- SU Region coordinates and dimensions are defined using a VSC SDP transmitted at least 100ns before the start of the SU region.
- After a SU Region, the Source may optionally transmit a VSC SDP containing the CRC accumulated for all of the SU Regions of the frame.
- Optional SU Region Early Transport support: the first SU Region is transmitted starting from the first active video scan line instead of its real position. The following regions are transmitted preserving the relative distance between them.



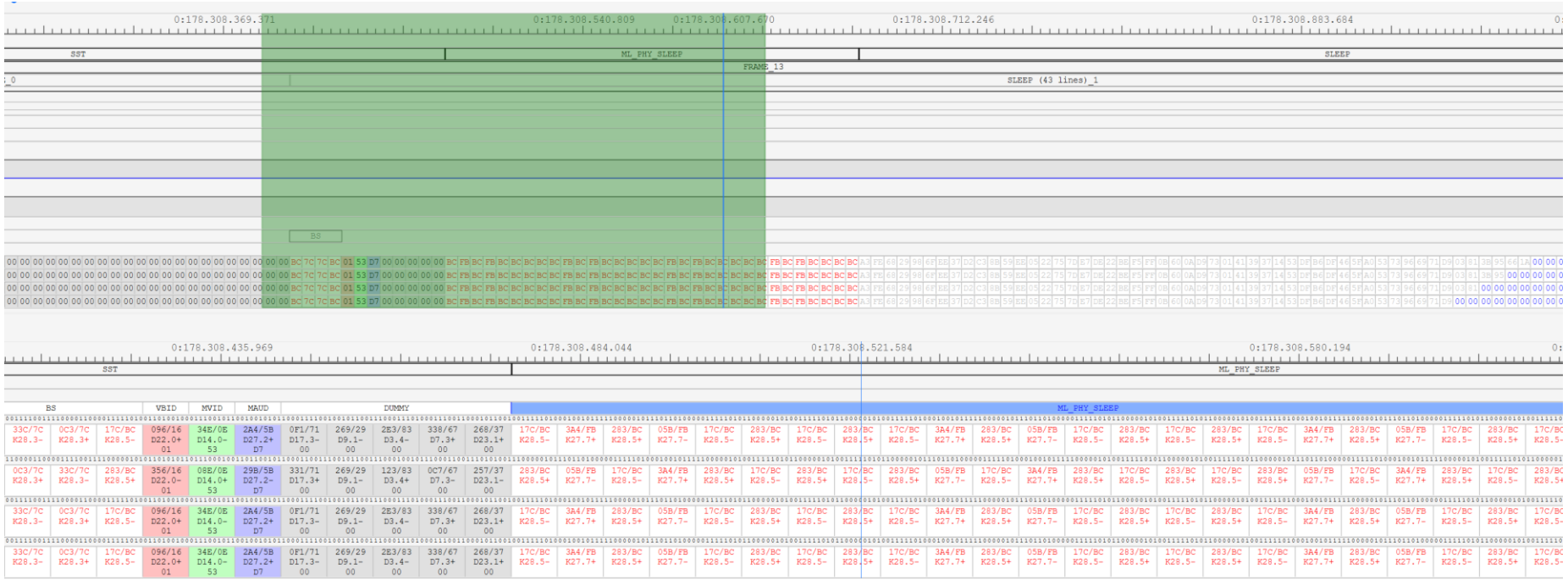
ALPM: Main Link Power-off

- The Source uses the ML_PHY_SLEEP sequence followed by scrambled zeroes to signal LTTPRs and Sink that the Main Link will be powered-off.
- The ML_PHY_SLEEP sequence consists of:
  - 8b/10b: a sequence of [K28.5, K27.7, K28.5, K27.7, K28.5, K28.5, K28.5, K28.5], with correct disparity
  - 128b-132b: a special 129-bit supersymbol [CDI=1 + 89898989h, 89898989h, 89898989h, 89898989h]. CDI is XORed according to standard rules, then precoded
- The Source transmits four consecutive ML_PHY_SLEEP sequences followed by scrambled 0s:
  - Once for each connected LTTPR
  - Once for the Sink

- The ML_PHY_SLEEP sequence must not overwrite BS+VBID, MSA, SDP data or FEC control link symbols.
- The Sink must look for two consecutive ML_PHY_SLEEP sequences and allow for max 4 symbol errors within them.
- Mandatory minimum ALW_SLEEP time after power-off sequence: 15us



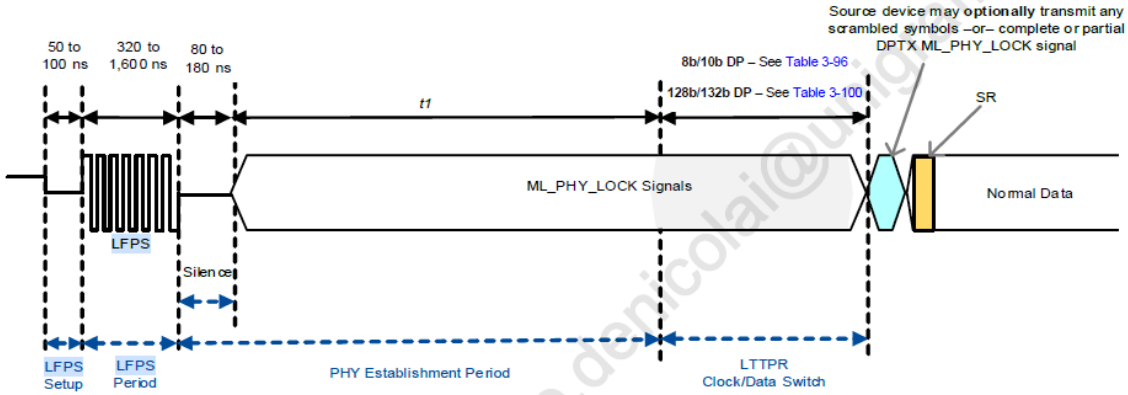
ALPM: Main Link Power-off (cont.)



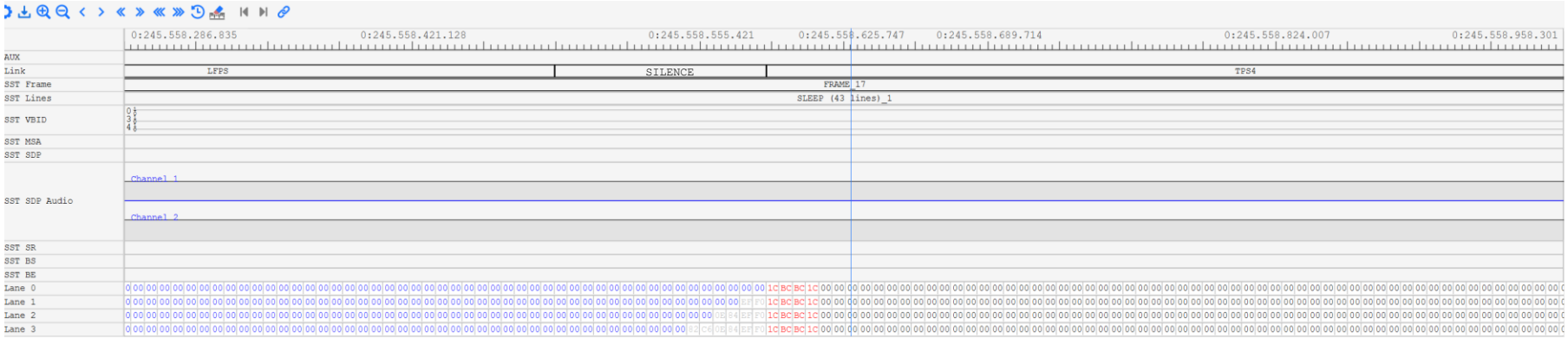
ALPM: Main Link Power-on (aka “wake”)

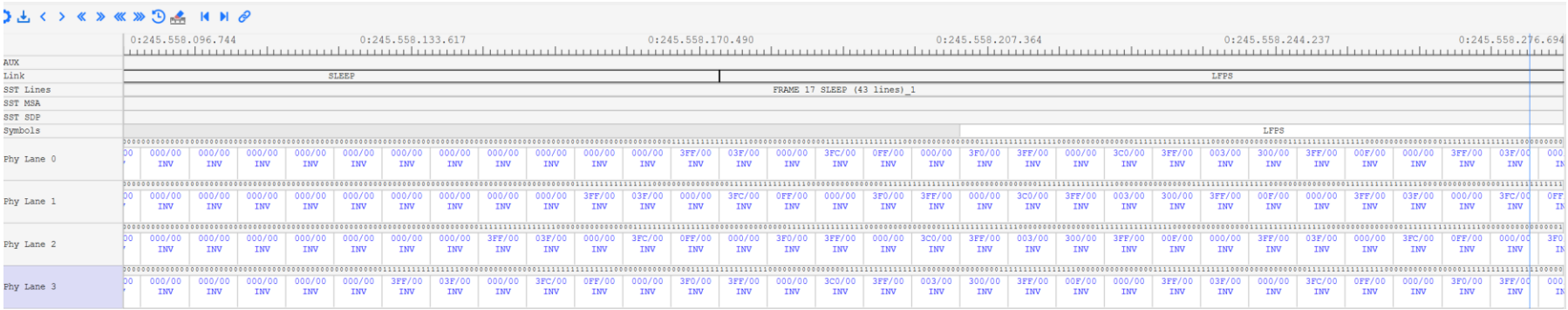
- The Source uses the ML_PHY_WAKE sequence to signal LTTPRs and Sink that the Main Link has been powered back on.
- The ML_PHY_WAKE sequence is composed by LFPS period (square wave at 12.5…50 MHz, at least 16 pulses, no more than 1.6us long) followed by a silence period and ML_PHY_LOCK pattern.
- ML_PHY_LOCK pattern:
  - 8b/10b – same as TPS4
  - 128b/132b – same as 128b_132b_TPS2 but with reduced intervals between LT_SCRAMBLER_RESET symbols (4 logical frames instead of 16)

- LFPS can have different common mode voltage amplitude than the ML data. Switch to ML common mode voltage is performed during the silence period
- The shortest duration of ML_PHY_LOCK is 50us. The Sink must complete EQ adaptation within this time. This is significantly shorter than usual link training



ALPM: Main Link Power-on (cont.)

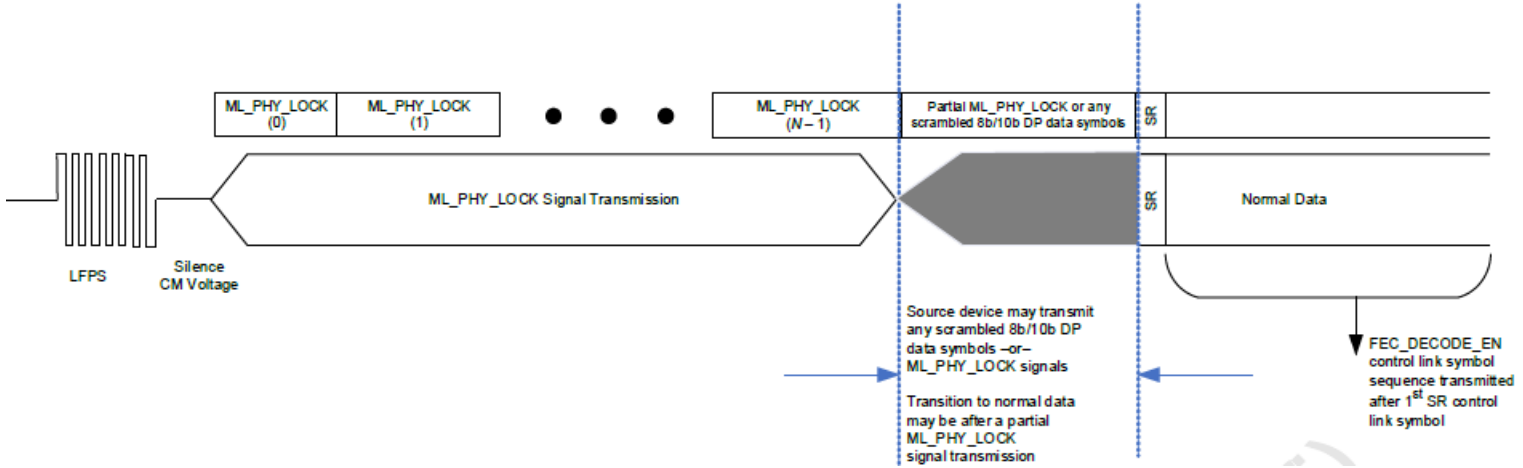




8b/10b FEC support

- In 8b/10b mode, FEC is not mandatory for ALPM. However, it is mandatory for Panel Replay.
- FEC block structure is maintained during the power-off sequence
- On the Sink side, FEC is considered disabled after power-off. Source must re-enable it by transmitting the FEC_DECODE_EN sequence after ML_PHY_LOCK pattern.

- The FEC block containing the final part of power-off sequence's scrambled 0s may be left incomplete. Sink must handle this situation correctly.
- The Sink cannot disable its FEC Decoder right when ML_PHY_SLEEP is detected but needs to wait for the last FEC block data to be decoded, since it could contain e.g. the tale of the last video frame transmitted.

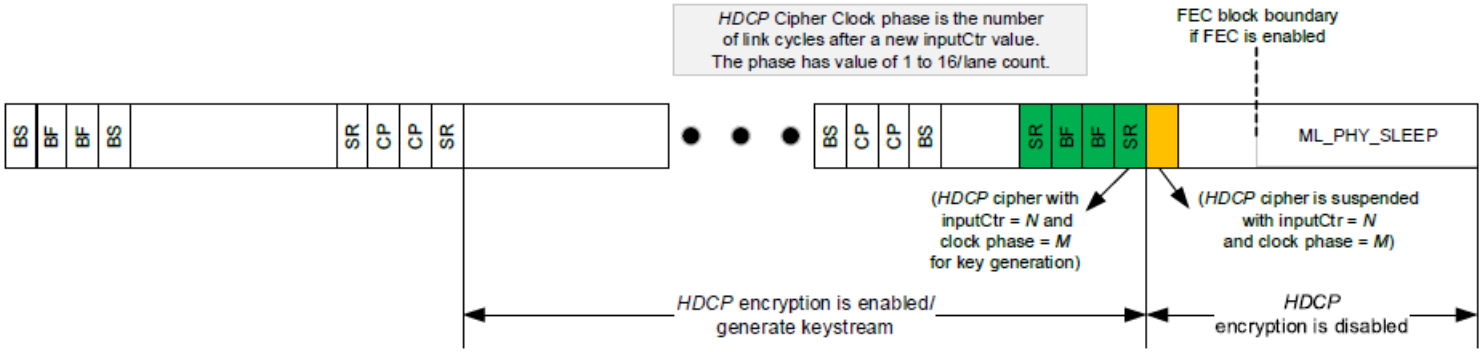


MST support

- During power-off sequence, ML_PHY_SLEEP is transmitted using all time slots.
- Source must be careful not to overwrite important data such as BS and VBID with ML_PHY_SLEEP in allocated slots.
- After power-on sequence, MST framing is started after the ML_PHY_LOCK pattern with an MST SR symbol.

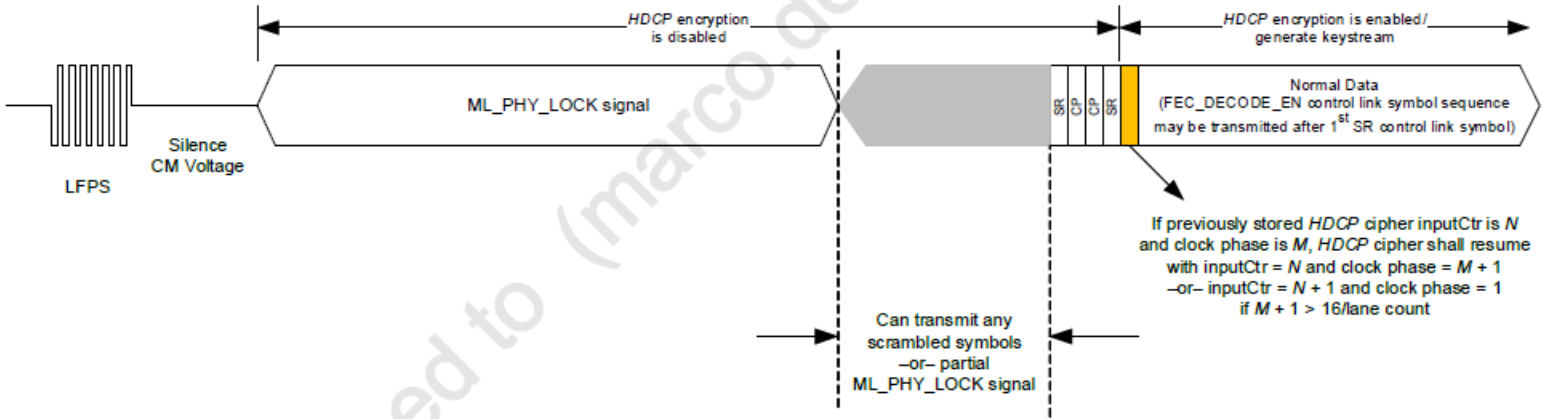
HDCP support

- Only HDCP r2.3 (or higher) is supported with AUX-less ALPM.
- HDCP is suspended before ML_PHY_SLEEP, HDCP cypher is frozen.



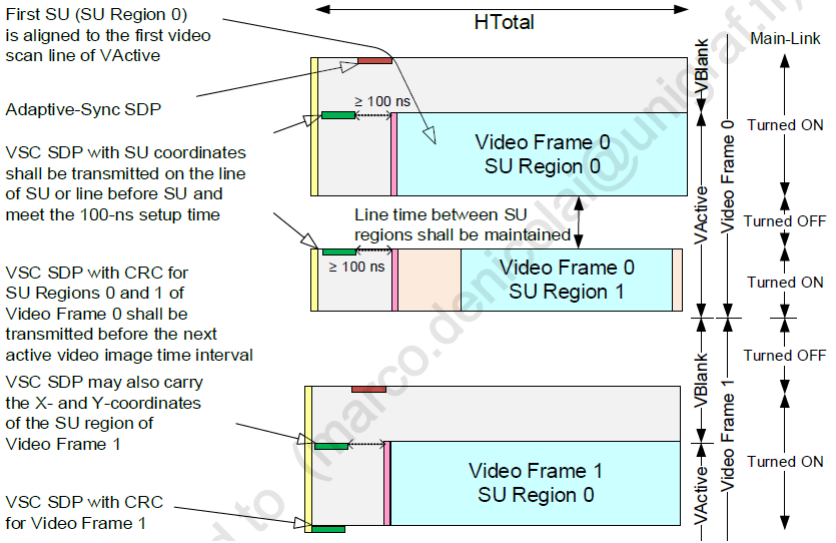
HDCP support (cont.)

- After power-on, HDCP is resumed and decryption continues from the previously frozen state, without the need for re-authentication.
- For 8b/10b SST and 128b/132b, encryption suspend and resume procedure is straightforward. For 8b/10b MST it is more complicated.



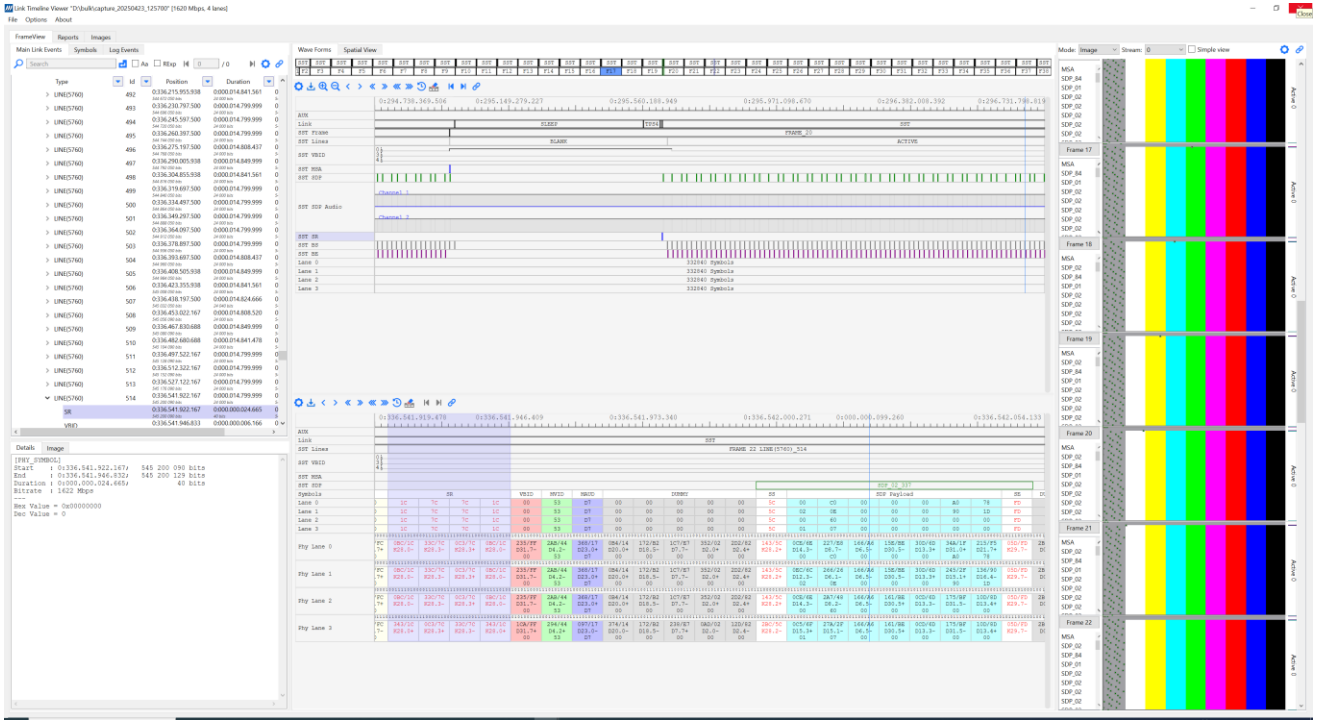
Panel Replay with ALPM

- When PR is in Active state, the Main Link can stay powered (option 1-A) or can be powered-off (option 1-C) using ALPM
- When ALPM is used, Sink and Source video timing synchronization is maintained using Adaptive-Sync SDPs, for each frame and at the same position.
- When ALPM is used, Early Transport is mandatory.
- Power-off is possible between SU regions, but the line interval still must be maintained.



DP Link Analyzer

A Unigraf tool for capturing Main-link Data Events and AUX Transactions. Within each frame, users can have a deep view of the events and metadata that occurs in each line. Measure distances in nanoseconds and symbol size to identify the length of problems in between events. Observe descrambled and scrambled symbols in hexadecimal format in each of the active lanes.



DP LRD Active Cable Testing

Lexus Lee
Allion Labs,Inc
2025/10/28

Overview

- Why The LRD Active Cable development matters
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA DP8K(HBR3) Connector Certification Introduction

Overview

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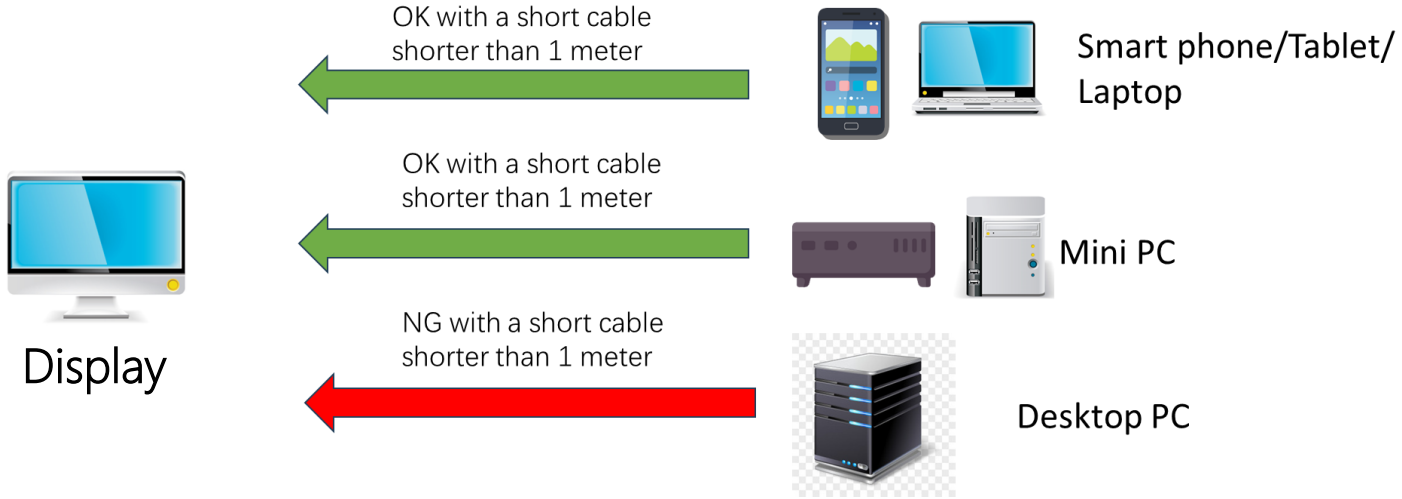
The Current UHBR Passive Cable Status

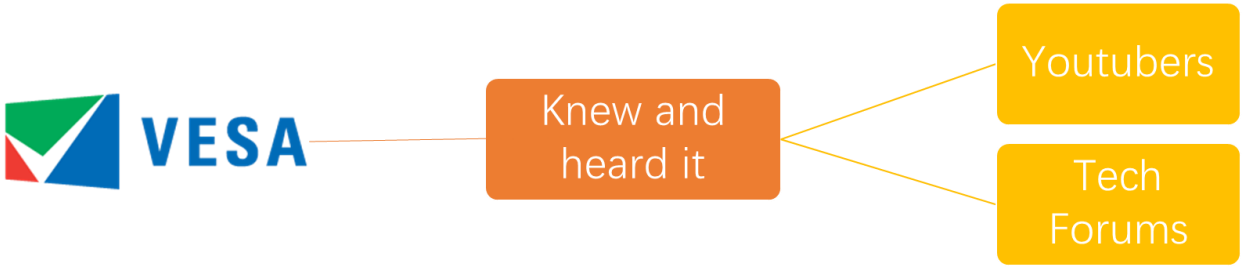
- DP to DP and USB-C to DP Passive cables for UHBR transmission
  - According to DP2.1a spec
    - UHBR 20-Capable Passive cable length: around 1 meter
    - UHBR 13.5-Capable Passive cable length: around 2 meters

- UHBR20 Passive cable in length: Not fitting all use-case

The Current UHBR Passive Cable Status Cont’



DisplayPort LRD Active Cable Solution



- VESA has brought us a solution to the criticism.
  - LRD Active Cable Solution
    - Get UHBR20 transmission to successfully work longer than 2 meter-long cable.
    - Creating a LRD Active Cable CTS

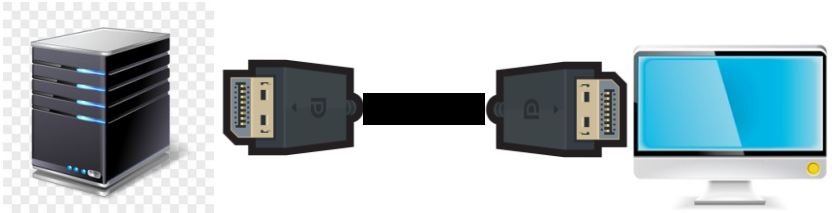
Overview

- Why The LRD Active Cable development matters
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA Legacy Connector Certification Update

CTS Testing Challenges

- Knowledge to get DP LRD cable to work up
  - AUX and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Aux P: Pull down to GND
2. Aux N: Pull high to 2.89~3.6V.
3. DP_PWR:2.89~3.6V
4. Aux transaction if needed

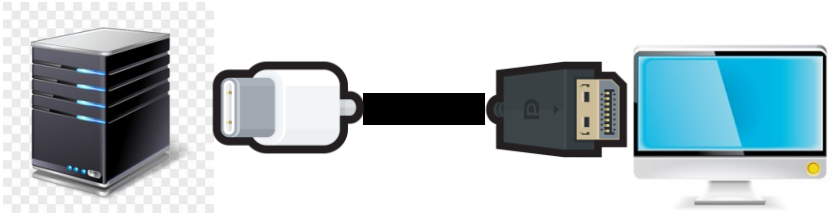


1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull high to 2.25~3.6V
5. Aux transaction if needed

CTS Testing Challenges Cont’

- Knowledge to get C to DP LRD cable to work up
  - Vconn, AUX, and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Vconn:3.0~5.5V
2. DP alt mode exerciser if needed.
3. Aux circuitry if needed.
4. Aux transaction if needed



1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull High to 2.25~3.6V
5. Aux transaction if needed

CTS Testing Challenges Cont’

- Power Consumption Check Before You Start Any Test
  - Do Link Training for
    - 1 Lane
    - 2 Lanes
    - 4 Lanes
  - Observe the current change of Vconn or DP PWR.
    - For example

	1 Lane	2 Lanes	4 Lanes
Current	80mA	170mA	380mA

CTS Testing Challenges Cont’

- Check How to Power up the LRD Cable Before You do Inrush Current Test
  - Supplying power to one end of a cable DUT ?
  - Supplying power to both ends of a cable DUT ?

	One End _Case	Both Ends_Case	Both Ends_but no power line used to connect the two LRD ICs.
Consuming Current	380 mA	190 mA	190mA

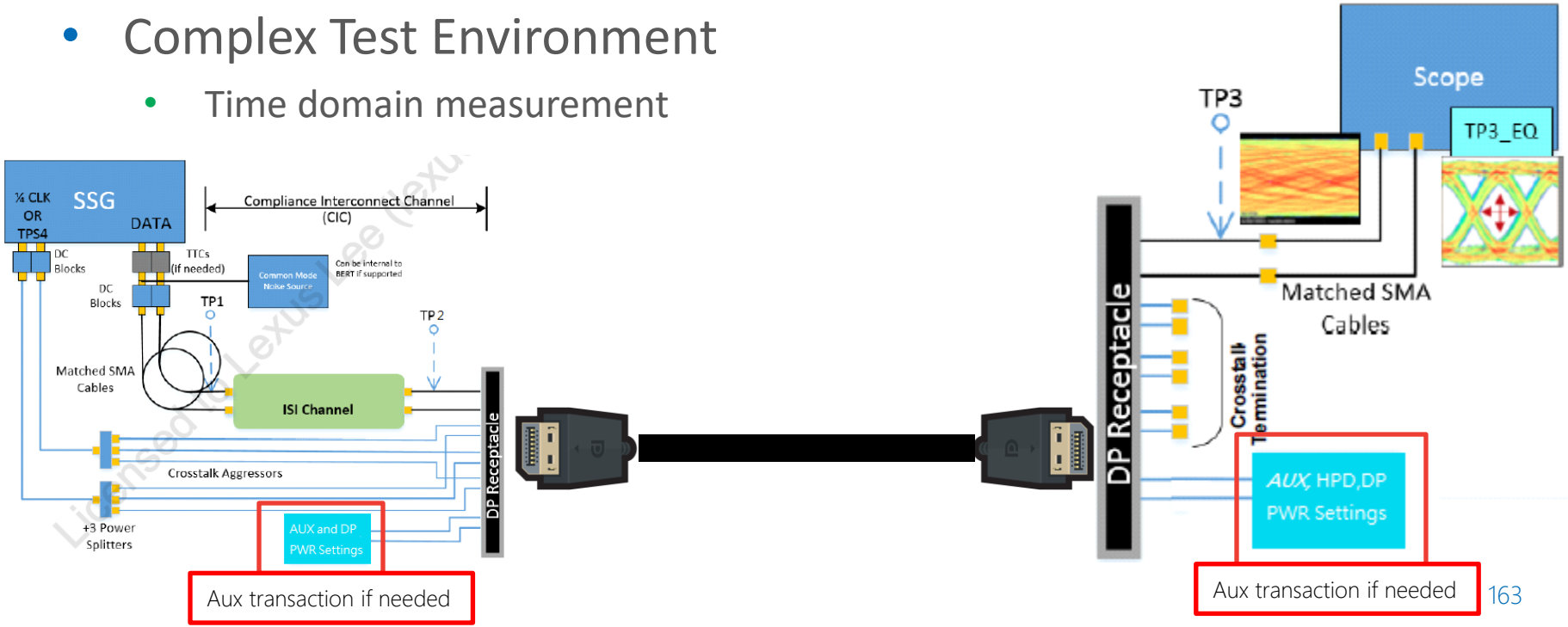
CTS Testing Challenges Cont’

- Why it matters
  - In order to get Maximum Inrush Current Energy

	One End _Case	Both Ends_Case	Both Ends_but no power line used to connect the two LRD ICs.
Measured Inrush Current Energy	4 mJ (wanted)	2 mJ (NOT wanted)	2 mJ (wanted)

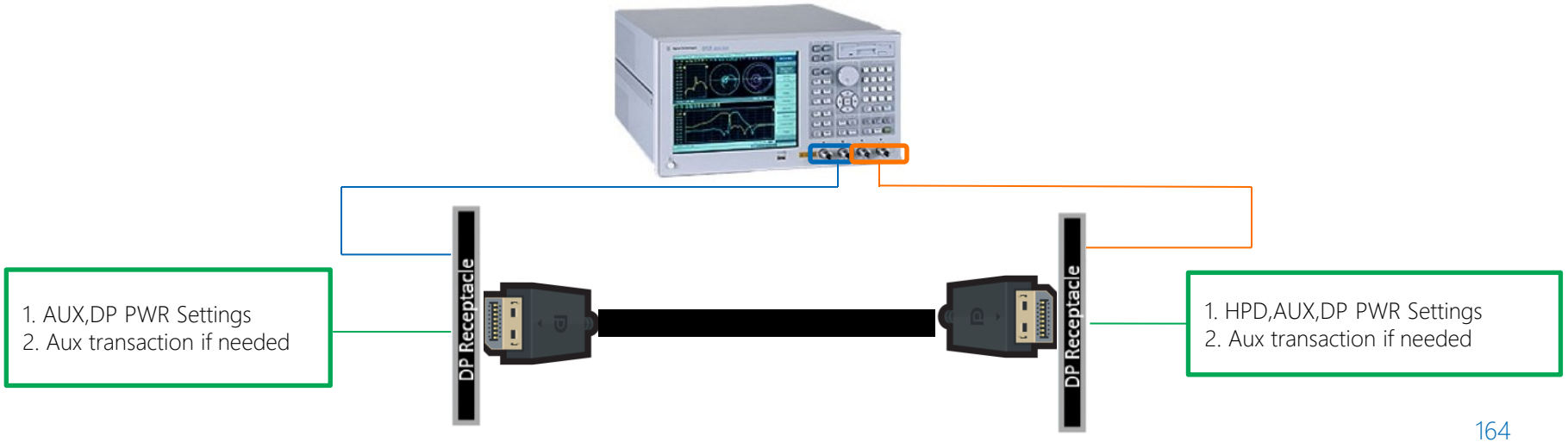
CTS Testing Challenges Cont’

- Complex Test Environment
  - Time domain measurement



CTS Testing Challenges Cont’

- Complex Test Environment
  - Frequency domain measurement

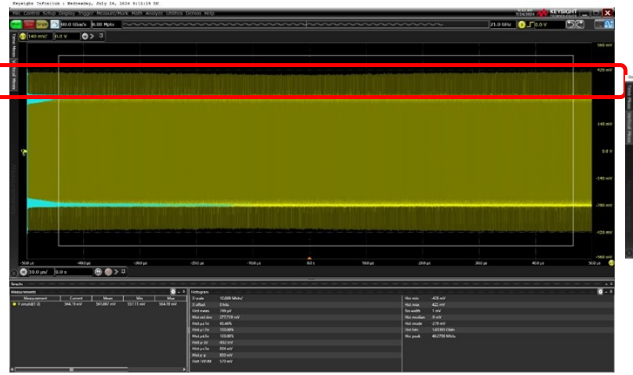


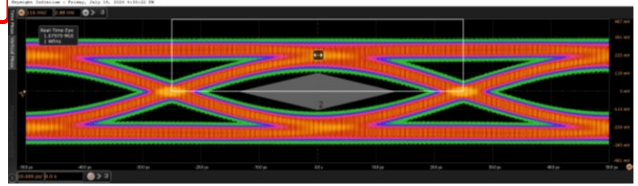
CTS Testing Challenges Cont’

- Stressed Signal Generator
  - Preset Calibration
    - Very important to stressed signal defined by DP spec.
    - Inaccurate preset number gets your stressed signal to highly not meet the expected ISI jitter, Eye Height, and Eye width.

Table 3-57: Preset FFE Coefficients[a] [b]

Preset Configuration #	Preshoot (dB)	De-emphasis (dB)	Informative Filter Coefficients		
			C_{-1}	C_0	C_{+1}
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0

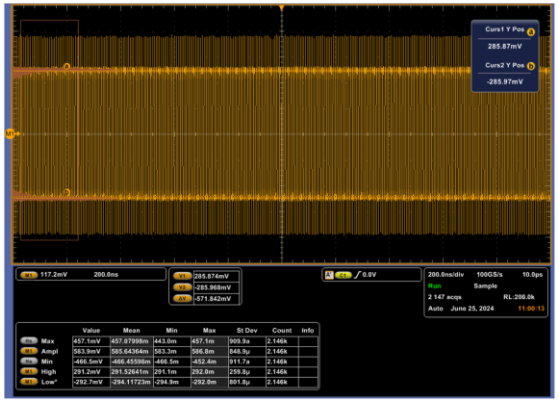


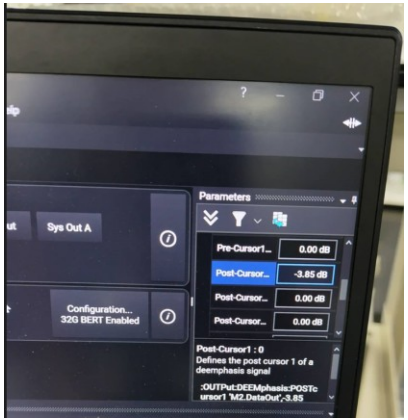


CTS Testing Challenges Cont’

- Stressed Signal Generator Cont’
  - Preset Calibration Cont’
    - Do not just enter the number that you want into your SSG FFE setting.

(SQ128) Rough De-emphasis: 20 log(585.6/923.4)=-3.95dB





Overview

- Why The LRD Active Cable development matters
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA Legacy Connector Certification Update

What is inside VESA LRD Cable CTS?

- Functional test
  - Successful Link Training
    - All data rate(from RBR to UHBR20)
    - All lane count (1-Lane, 2-Lane,4-Lane)
    - Bidirectional (Swap Sink/Source end)
    - Power management (Active Power ,Wake/Sleep, Aux-less ALPM)
    - USB-C Orientation (Flip/Normal)
  - SOP/SOP’ Response Check(SVDM2.0/SVDM2.1)

What is inside VESA LRD Cable CTS? Cont'

- Frequency Domain test
  - Insertion Loss Fit

Table 4. Insertion Loss Fit Requirements

Frequency[1]	Insertion Loss Fit[2]	Description	Min	Max	Units
100MHz	*ILatDC*	Defining the ILfit mask for the cable response. Note: The main intention is to keep the cable with LPF characteristic similar to the passive cable.	DP80: -6 DP80LL and DP54: -5	0	dB
Nyquist	*ILFitatNq*		DP80: at 10GHz: -7.5 at 6.75GHz: -6.2 DP80LL: at 10GHz: -6.5 at 6.75GHz: -5.2 DP54: At 6.75GHz: -10.5 At 5GHz: -9	*ILatDC – 1.5*	dB
Nyquist x 1.25	*ILFitatf2*		*ILFitatNq - 3*	*ILFitatNq*	dB
Nyquist x 1.5	*ILFitatf3*		*ILFitatNq - 4*	*ILFitatf2*	dB
100MHz to Nyquist	*ILFitatWB*	Max gain of the cable in the range of DC to Nyquist Frequency		0	dB

What is inside VESA LRD Cable CTS? Cont’

- Time Domain test
  - Eye Diagram
  - Instantaneous Common Mode Voltage
  - CONFIG2 Voltage and No DP_PWR thru Cable
  - AUX-Less ALPM
  - LOS Test
  - Inrush Test
  - AUX Voltage Clamping
  - Preset Distortion Thru the cable

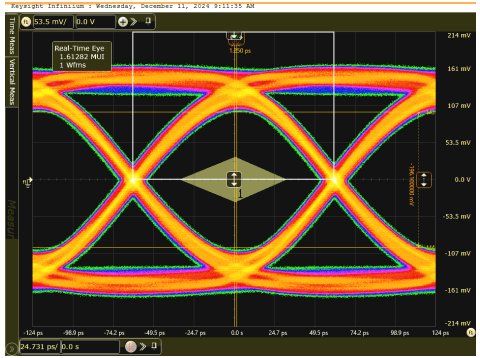
Most Failed Items sharing

- Inrush Current
  - Criteria
    - ResultantENERGY_POWER_CONSUMER < 0.07mJ
    - ResultantPEAK_CURRENT_POWER_CONSUMER <= 13.5A
  - Inactive mode
    - No Data running over Main Link
      - No one fails (All Pass)
  - Active mode
    - Data running over Main Link is on
      - Some cables failed before.

Most Failed Items sharing

- Eye Diagram
  - UHBR20 Criteria
    - TP3_EQ-Inner Eye Height: 100mV
    - TP3_EQ-Eye Width: 560mUI
    - Cannot hit the eye mask
  - Requirement: Need to pass with 3 TxFFE Pesets and average of 5 times.

Preset Configuration #	Preshoot (dB)	De-emphasis (dB)
0	0	0
1	0	-1.9
2	0	-3.6
3	0	-5.0
4	0	-8.4
5	0.9	0
6	1.1	-1.9
7	1.4	-3.8
8	1.7	-5.8
9	2.1	-8.0
10	1.7	0
11	2.2	-2.2
12	2.5	-3.6
13	3.4	-6.7
14	3.6	0
15	1.7	-1.7



Overview

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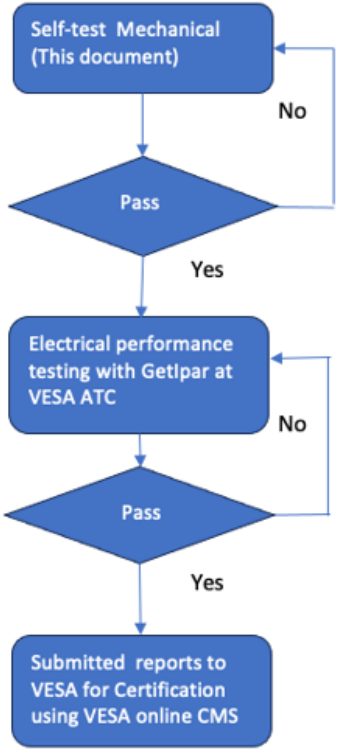
DP Connector Certification Status

- Connector certification
  - Legacy connector(HBR2 and below)
    - Self-test Mechanical only
  - Enhanced Connector(UHBR13.5 and UHBR20)
    - Self-test Mechanical
    - ATC test Electrical Performance

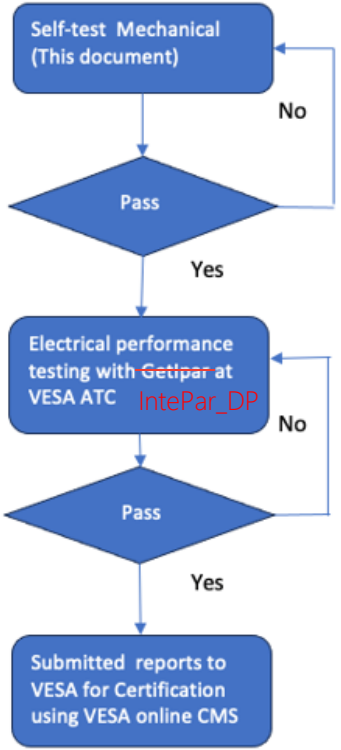
VESA® DisplayPort™ Self-Test Report for Connectors v2.1



DP Connector Certification Status Cont'

- New, This Year
  - DP8K(HBR3) Connector Certification
    - Self-test Mechanical
    - ATC test Electrical Performance

VESA® DisplayPort™ Self-Test Report for DP Connectors Supporting HBR3 Link Rate and DP8K Cables



Thank you

Break

VESA Logos and Marketing Guidelines

VESA Membership Allows Use of VESA Logos

- When your product passes certification company can use VESA logo to show customers proof of quality

Cable Logos include:

DP Product Logos include:

Display Logos include:

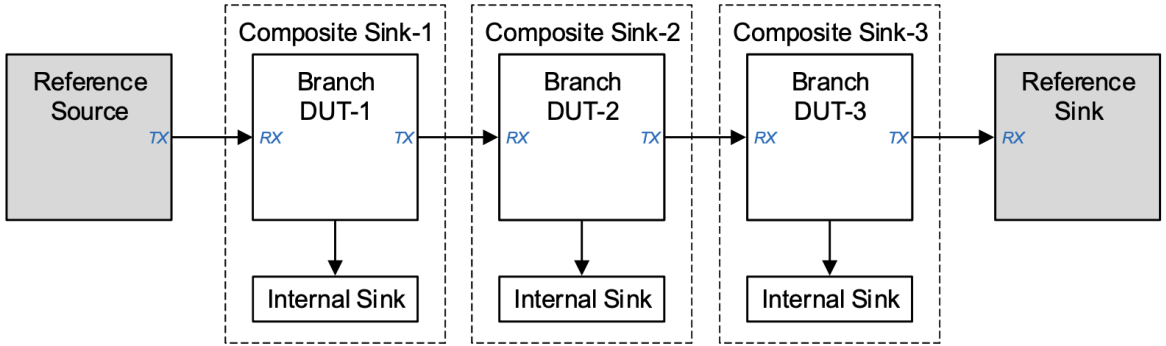
Compliance Testing

VESA PlugTest Events

- Provide significant value to VESA compliance program and member companies, particularly as new capabilities and products are deployed.
- Demonstrate and improve traditional interoperability
- Test Native DP and DP Alt Mode over USB Type-C™ products
  - UHBR rates, DSC, New MST Link Layer Tests, FEC, DisplayHDR and other new capabilities
  - Verify Test Equipment Correlation
- VESA hosted two successful PlugTests in 2024 (Taiwan and US)
- VESA hosts two PlugTests in 2025
  - South San Francisco, CA USA: **Q1 2025 (completed)**
  - Taipei, Taiwan: **Q4 2025 (Oct 20-23rd Taiwan)**

Multi-Stream Transport (MST) Compliance Testing Enhancements

- After over a year of specification and test equipment test development VESA is preparing to release its biggest MST test update since DP 1.2. With the introduction of UHBR20 + DSC, users can now daisy chain multiple 4K/120Hz displays from a single output connector
- The unique DP capability of driving multiple daisy chained displays with a single output connection/cable is increasingly the most popular feature of DP for end users
- To further improve end user experience with MST configurations, VESA's latest DP Link Layer Compliance Test Specification adds dozens of new MST source/sink tests to verify products are implemented according to DP specifications



DP 2.1a LL CTS Composite Sink (Daisy-chainable Sink) Setup 3

DP54, DP80 and DP80LL Cable Specifications and Certification program

- Work on Enhanced DP cable and connector specifications and test requirements started in 2021 to ensure high performance connectors and cables would be available for products supporting UHBR rates
- DP54 and DP80 Certified cables provide added assurance of proper operation at the highest link rates (UHBR10, UHBR13.5 and UHBR20 Gbps).
- DP80LL active LRD cable CTS and certification added to provide UHBR20 Gbps rate support for longer cables (can support ~3 meter cables)
  - Linear Redrivers (LRD) are level boosting amplifiers that boost signal transmission over longer distances
- Over 150 Enhanced DP cables and connectors have been certified since launch of the Enhanced DP cable and connector certification programs

Product certifications* 2023/2024/2025

Products	2023	2024	2025
DP Sources	99	93	133
DP Sinks	277	491	411
DP Cables	59	70	49
DisplayHDR	397	556	560
ClearMR	45	53	69
AdaptiveSync	80	75	105

*Note: Numbers are base model certs not including family models. Updates to Compliance Management System (CMS) will include feature to count family models in the future.

Summary

Summary

- Product shipments and certifications based on VESA technologies continue impressive growth
- DP 2.1 UHBR capable product development and certifications are in mass production
- VESA Enhanced cable and connector certification programs have been very successful with significant numbers of DP54, DP80 and now DP80LL cables certified
- DisplayPort over USB-C is a game changer for small form factor and portable products and is now the defacto standard for laptops, tablets and handheld devices
- MST continues to be a popular DP feature and with UHBR20 + DSC it can be used to drive multiple high resolutions displays at high refresh rates through a single connector
- Display Performance Standards adoption and certification have been extremely successful the last several years
- Development and adoption of new technologies continues to drive increases in VESA membership growth

VESA

THANK YOU

DisplayPort.org
DisplayHDR.org
ClearMR.org
AdaptiveSync.org
VESA.org

Questions?

VESA

Demo Tables

Poster x1

Demo Tester x1

GRL-C2-EPR

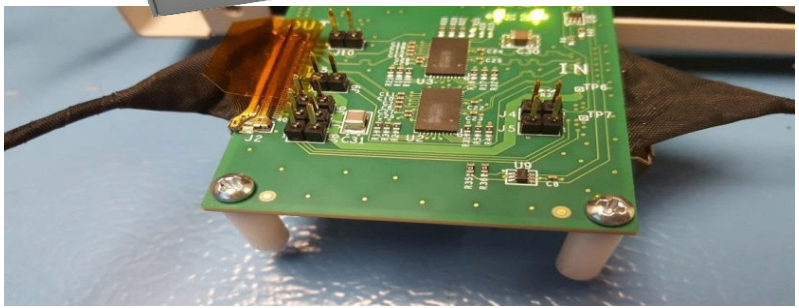
eDP and DisplayPort Protocol Analysis and Validation Real Time *ANY* Source to *ANY* Sink

FuturePlus Systems

Advancing Technology Development

NEW NEW

USB-C Power Delivery Analysis Software for DisplayPort Ask for a Demo!



eDP 1.4b and 1.5a, DP2.1
USB-C and DisplayPort
Probes
UHBR10, UHBR13.5
Up to 4 Lanes
Single Stream Transport and
Multi-Stream Transport
and more....

Something Special? We Like Challenges!

Accelerate Your High-Speed Digital Compliance Testing

KEYSIGHT

Measurement disaggregation solution

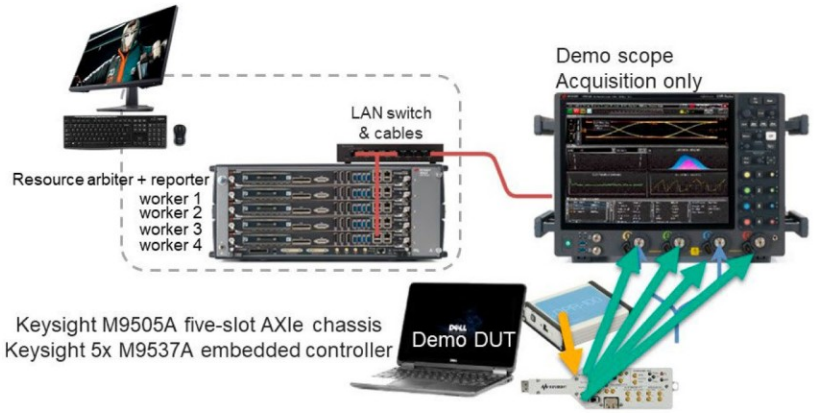


Figure 1. Keysight measurement disaggregation hardware setup

Summary

- Each new generation of high-speed computing standards includes more tests and factors to consider.
- Complex computations slow down overall throughput, and the acquisition hardware stays idle during the analysis.
- Measurement disaggregation offloads measurements and analysis to the cloud speeding up the overall test time.

For more information: Measurement Disaggregation

UNIGRAF

DisplayPort

USB Type-C

sales.asia@unigraf.fi

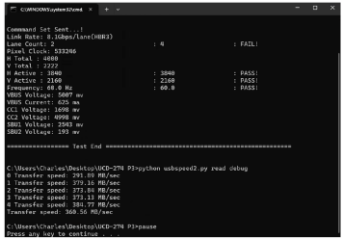
Unigraf DisplayPort and USB-C Test Solutions

UCD-500 Gen2

16K DP 2.1 Generator & Analyzer

- DP 2.1 Link Layer CTS Tool
- DP 2.1 Sinks and Sources up to 8K@60Hz (UHBR 20Gbps / Lane) and 16K@60Hz with DSC
- Featuring Link Analyzer, Panel Replay and eDP test functions

UTC-274



USB-C Test Automation Tool

- Test DP Alt Mode, Power Delivery and USB Speed
- Support EPR function up to 240W Source and Sink
- Test USB-C connector pins soldering and assembly quality with a single cable insertion





UNIGRAF

DisplayPort Alt Mode Compliance Testing and Analysis solutions

SYMBIOSYS ALLIANCE

Ellisys USB/DPAM Test and Analysis Solutions

USB Explorer™ 350

Multi-function USB Type-C®, USB 3.2, and Power Delivery Protocol Test Platform

VESA-Approved Tester for DisplayPort ALT Mode

Type-C Tracker™

Protocol and Electrical Analysis Tool for USB Type-C® Standards

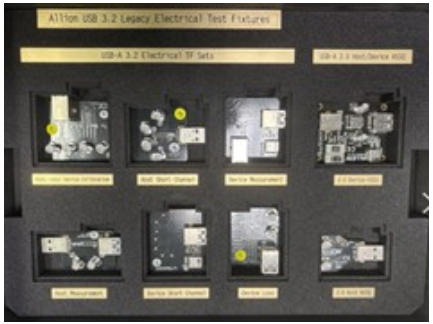
Includes DP AUX and DP ALT Support

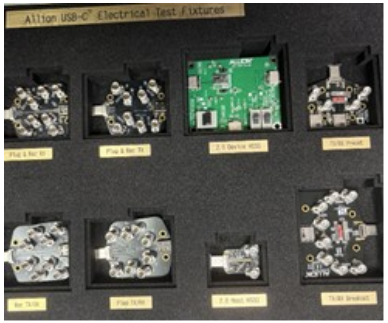
ellisys
Better Analysis

Allion Demo Table

- Test Fixtures
  - Designed for USB-C to (m)DP Cable Compliance Testing
  - Designed for USB 3.2 & USB-C Compliance Testing

- Brochures
  - PCIe 6.0 Test Fixture
  - USB 3.2 Test Fixture
  - DP/HDMI Test Fixture
  - C to DP/mDP Cable Test Fixture





Teledyne LeCroy
Test Solutions for DisplayPort v2.1

M42de 80G Video Analyzer/ Generator

TELEDYNE LECROY
Everywhereyoulook™

Teledyne LeCroy
7F., No. 667, Bannan Rd
Zhonghe Dist, New Taipei City 235
Taiwan
Phone: +886-2-8228-6100

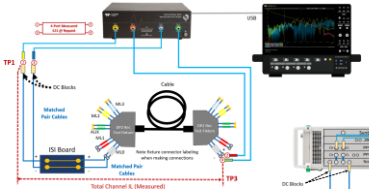
protocolsales@teledynelecroy.com

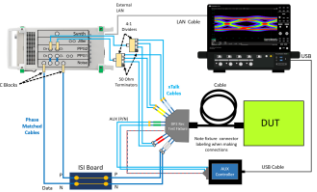
Teledyne LeCroy DisplayPort Test Platforms

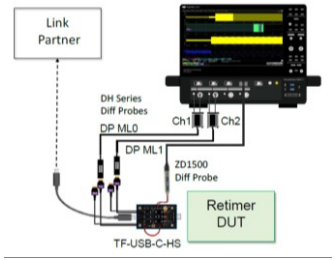
- **Quantumdata M42de Analyzer / Generator**
  - DisplayPort 1.4 & 2.1 (UHBR) Lane Rates
  - DP80 and USB Type-C® connectors
  - Deep Capture / Analysis
  - T.A.P.4™ Passive Monitoring
  - Comprehensive DP 1.4 & 2.1 Compliance Coverage
    - Link, DSC, LTTPR, EDID & MST
  - qdPrime™ Automated Test Suite

- **Quantumdata M21 Analyzer**
  - Portable DP Analyzer & HDMI Analyzer / Generator
  - DisplayPort Source Testing only (up to UHBR 13.5Gb/s)
  - AUX Channel Monitoring

DisplayPort 2.1 PHY Compliance and PHY-Logic Debug



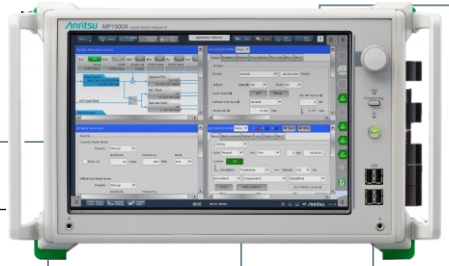




- DisplayPort 2.1 Source (Tx) Compliance
  - WaveMaster/SDA 8000HD with QualiPHY® 2 software
  - SDAX-DP expert analysis – Find Best CTLE/DFE
  - Reduced test times with QPHY2-PC
  - Automated Return Loss with WavePulser 40iX
- DisplayPort 2.1 Sink (Rx) Compliance
  - WaveMaster/SDA 8000HD with QualiPHY 2 software
  - SSG Cal and BER testing using Anritsu MP1900 SQA
  - Automated Channel Cal with WavePulser 40iX
- PHY-Logic (Interop) Debug
  - AUX Triggered + Main Link capture
  - TF-USB-C-HS – probing access
  - DP-AUX, USB-PD TDMP software
  - Clock switch testing on live link

MP1900A Signal Quality Analyzer
High Speed Bus SINK Compliance Solution

MP1900A Standalone
Multi-channel BER Measurement
High-quality PPG
High-input-sensitivity ED
PAM3/4 BER Measurements



Jitter Tolerance Test
SJ/RJ/BUJ Injection
Low-rate estimated BER measurement

Thunderbolt
4/5&DP1.4/2.1 Rx Test
Stressed Signal Calibration and
Stressed Signal Input Test

USB Link Sequence Generation
Transition to Loopback mode

Stressed Signal Calibration
PCI Express Link Sequence Generation
Transition to Loopback Mode
Pass/Fail evaluation using BER measurement

Calibration of stressed signal* → Transition DUT state to Loopback → Stressed Receiver Testing

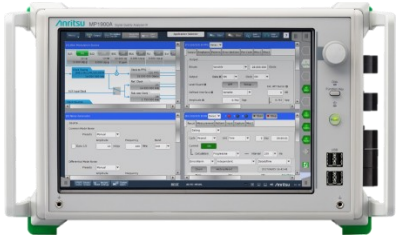
MX183000A Software

Stressed Signal Calibration*	USB Link Sequence Generation Function PCI Express Link Sequence Generation Function	Stressed Signal Input Test Function Jitter Tolerance Test Auto-receiver Test Function

MP1800A Hardware

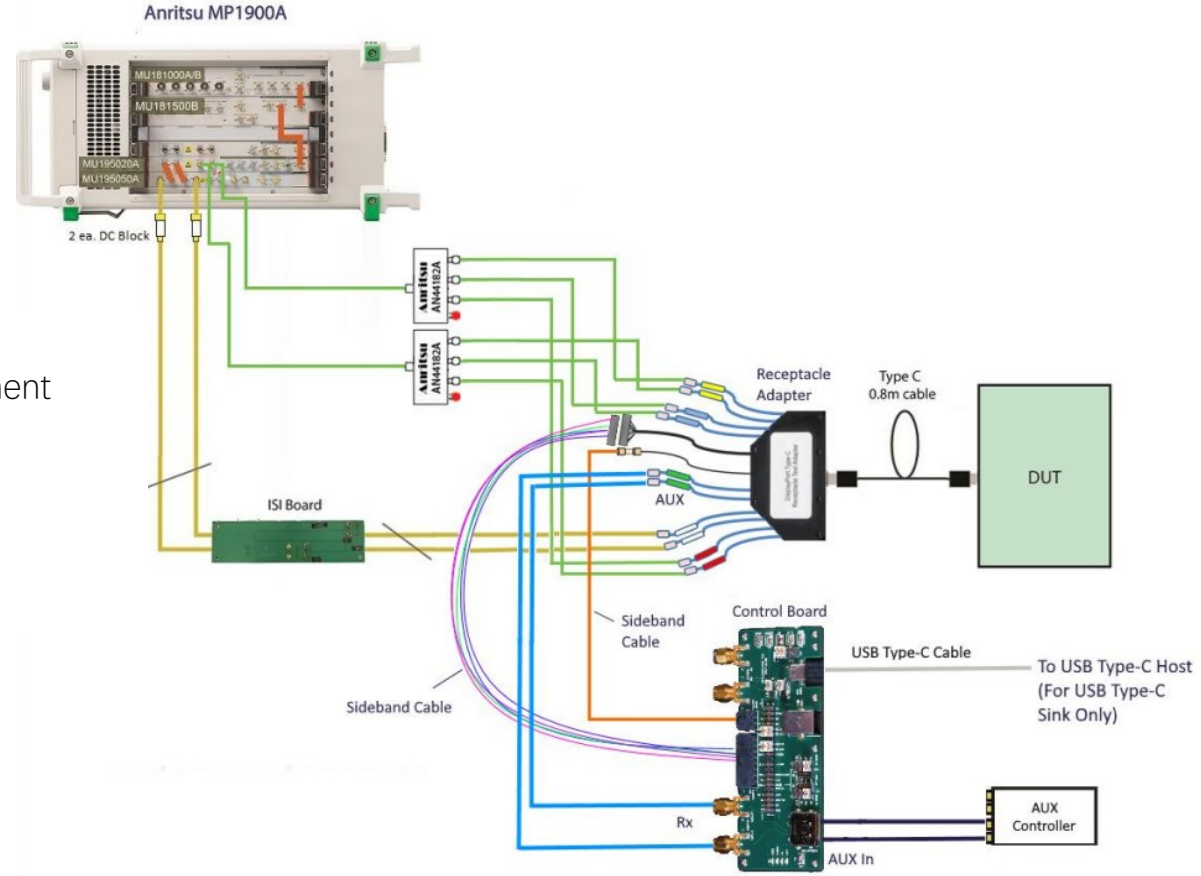
Up to 32 Gbit/s, 8ch	High Quality Signal	Jitter Emphasis

MP1900A Signal Quality Analyzer
DP1.4/2.1 SINK Compliance Test Structure



MP1900A Standalone

- Multi-channel BER Measurement
- High-quality PPG
- High-input-sensitivity ED
- PAM3/4 BER Measurements
- DP1.4/2.1 and USB4v1&v2 Compliance test Support



Thank you for attending the VESA Workshop Shenzhen, China 2025