Welcome
VESA Workshop
Taipei, Taiwan
2025

Time	Topic	Speaker
10:00am	VESA Overview and Standards Updates, Including DisplayPort v 2.1b	Jim Choate, VESA CPM
10:30am	DisplayPort Link Layer CTS v 2.1 MST Updates	Alok Soni, Software Lead, Teledyne LeCroy
11:00am	eDP and DP v 2.1 PHY CTS Overview and Updates	Francis Liu and Victor Chiu, Keysight Technologies
11:30am	DP Alt Mode v 2.1a Overview and CTS Updates	Henry Tsai, Protocol Specialist, Teledyne LeCroy
12:00pm – 1:00pm	Lunch	
1:00pm	DP v 2.1 Panel Replay and Advanced Link Power Management: Implementation and Testing Challenges	Marco Denicolai, Product Owner, IP Cores, Unigraf Oy
1:30pm	VESA Display Panel Standards Overview	Robert Yang, Granite River Labs
2:00pm	Automotive Extension Services	Tung-Sheng Lin, Senior Technical Manager, MediaTek
2:30pm – 2:45pm	Break	
2:45pm	LRD/Active Cable Testing and DP 2.1 Enhanced Connector Certification	Lexus Lee, Technical Program Manager, Allion Labs
3:15pm	VESA Compliance Program	Jim Choate, VESA CPM
3:35pm	Summary, Questions & Answers	Jim Choate, VESA CPM
3:50pm	Demo Stations Overview	

VESA Overview and Standards Updates, Including DisplayPort v 2.1b

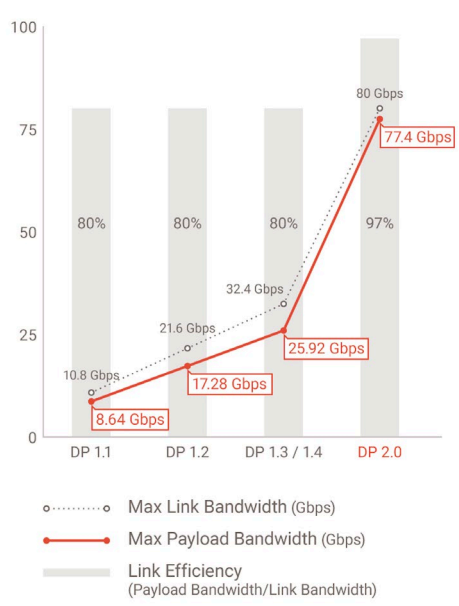
Jim Choate
VESA Compliance Program Manager
17-OCT-2025

Interoperable End-to-End Visual Ecosystem

- Ensuring interoperability of display stream transport from Stream Source (e.g., GPU) to Stream Sink (e.g., Monitor)
  - Stream Transport
    = DisplayPort (DP) via DP, USB-C,
    or USB-C-to-DP cable
  - Stream Compression
    = Display Stream Compression (DSC)
  - Capability/Config Data Structure
    = EDID/DisplayID for Stream
    and DPCD for Transport
- Visual performance accountability
  - Display Performance Metrics
    (DPM)

Stream Transport Headroom Provided by DPv2.x

- UHBR20 added in DPv2.x provides for 3x payload (= usable) bandwidth of HBR3
  - Link rate increase + channel coding efficiency improvement (from 8b/10b to 128b/132b)
- "DSC mandate" added in DPv2.x significantly increases the transportable stream bandwidth
  - 4-lane HBR3 with DSC sufficient for 4K2K240
    - Also, good for 4x 4K2K60 monitors cascaded/via an MST dock
  - 4-lane UHBR20 with DSC sufficient for 12K2K240
    - Also, good for 3x 4K2K240 monitors cascaded/via an MST dock



DP Standard Version Number…

- Only the latest version is active per VESA policy
  - The latest, and, thus, active, version is DPv2.1a released December 2023
  - A new standard version comes with:
    - New features not related to link rate (e.g., Panel Replay, Adaptive-Sync SDP payload extension in v2.x)
    - Interop improvement policy updates
- VESA certification policy will change end of 2025 to only allow product certifications for DP 1.4 and DP 2.1 products.

Two Types of DP Transport

- Native DP Transport
  - Uses DP PHY Layer to transport DP Link Symbols carrying stream data
  - Cable types
    - A DP cable
    - A USB-C cable or a USB-C-to-DP adapter cable: DP/Multi-Function (MF) Alt Mode
      - DP/MF Alt Modes are Native DP transport as they use DP PHY Layer to transport DP Link Symbols
- Tunneled DP Transport
  - Uses USB4 PHY Layer to transport Tunneled DP USB4 packets encapsulating DP Link Symbols carrying stream data
  - Cable type
    - A USB-C cable

	DP1.4x		DP2.x			
	DP1.4 (FEB 2016)	**DP1.4a (APR 2018)**	**DP2.0 (JUN 2019)**	**DP2.1 (OCT 2022)**	**DP2.1a (DEC 2023)**	**DP2.1b (Target: Summer 2025)**
Link Rates	HBR3, HBR2, HBR, and RBR (8.1/5.4/2.7/1.62 Gbps/lane, respectively). *HBR3 and HBR2 DPTX Voltage Swing and Pre-emphasis Monotonicity spec updated in DP1.4a*		**Addition UHBR rates** (UHBR20, UHBR13.5, UHBR10, having 3x/2x/1.5x of HBR3 link usable bandwidth). The maximum commonality with USB4 Gen2/Gen3 PHY: 128b/132b channel coding, RS(198,194) 8-bit symbol FEC, 16x TX FFE presets, RX reference CTLE/DFE			
Channel Coding and Pixel Data Mapping	8b/10b DP SST (Single Stream Transport) /MST (Multi-Stream Transport)		**Addition of 128b1/32b DP.** The common pixel data mapping to Link Layer symbols for both single- and multi-stream transport			
LTTPR	Added LTTPR (Link Training Tunable PHY Repeater) spec		Mandated LTTPR Non-Transparent Mode for UHBR rates	LTTPR Spec Clarification: (1) AUX transaction handling (2) 8b/10b DP LT in Non-LTTPR Mode and LLTPR Transparent Mode		
Link Training Fallback	Link rate reduction before lane count reduction (e.g., 4L HBR3 —> 2L HBR3 —> 4L HBR2)		For 128b/132b DP, fallback is to the next highest BW (e.g., 4L UHBR20 —> 4L UHBR13.5, instead of 2-lane UHBR20). **The next highest BW policy also allowed for 8b/10b DP.** **The repetition of DP Link Training with the same Link Config in case of a Link Training failure allowed up to twice starting from DP2.1a**			
Cables	Defined DP8K cable spec for HBR3 link rate		Detachable cables for UHBR rate limited to USB4 Gen2/Gen3 C-C cables	Addition of **DP40** and **DP80** DP/C-to-DP cables	DP40 cable replaced with **DP54** cable	Addition of **DP80LL** cable. Active DP cables required to meet DP80LL loss budget
FEC	Added RS(254, 250) 10-bit symbol FEC: Mandated for DSC bitstream, Optional for uncompressed		No change to 8b/10b DP FEC. **RS(198, 194), 8-bit symbol FEC always enabled for UlHBR rates**			
Power Management	AUX write of 02h to DPCD 00600h to prompt DPRX into DP Link Sleep State			Addition of **AUX-less ALPM**		
Video Fallback	640x480p60 (VGA Safe Mode)		1080p60 Video Fallback (enumerated at DPCD 00020h)			
DSC Transport	Added as optional		**Made DSC transport support mandatory for DP devices with UHBR-rate support.** Added **DSC pass-through for DP Branch device** (e.g., DP-to-HDMI PCON) added			
Panel Replay	N/A		**Added as optional for reductions of (1) active power and (2) DP tunneling BW**	**Added "Main Link Off" Panel Replay** for further power reduction leveraging AUX_less ALPM Specified Panel Replay concurrent with Adaptive-Sync operation		
Audio Support	(1) Added Audio Stream SDP as mandatory for DPRX both in single- and multi-stream transport and (2) extended supported audio stream formats to cover up to 32-ch 3D LPCM audio starting from DP1.4					
SDP	Added VSC_EXT chain-able SDP	Added Adaptive-Sync SDP		Expanded Adaptive-Sync SDP payload for an improved Adaptive-Sync (known as VRR in HDMI terminology) operation		
Protocol Converter (PCON) Support	HDMI TMDS Mode support only. Autonomous Mode only; no Source-controlled Mode)		**Added support for HDMI FRL Mode (from DP2.0) and VRR Mode (from DP2.1a). Added Source-controlled Mode**		**Refined Autonomous Mode**	**Updated Autonomous Mode as Regulated Autonomous Mode**
DPRX HBLANK Expansion/Reduction	Added DPRX HBLANK Expansion mainly to support 8K60 HDMI2.1 TV support (8K4K60 (VIC197) with 12bpp DSC requires reduced HBLANK to fit in 4-lane HBR3)			Added DPRX HBLANK Reduction mainly to increase Audio Stream SDP transport BW in UHBR rates in conjunction with DSC bitstream transport		
DP Tunneling	DP Tunneling DPCD registers for proprietary tunneling of DP Link Symbols (e.g., Thunderbolt3)			DP Tunneling DPCD registers for DP tunneling over USB4. **Added (1) DP tunneling BW allocation management and (2) Panel Replay optimization**		

Standard Spec and CTS (Compliance Test Spec)

- A standard specification encourages compliance through a logo certification program
  - A logo certification requires for a product to pass compliance and interop tests
  - Compliance test procedures described in CTS (Compliance Test Spec)
- However, the reality is…
  - A CTS release ends up lagging a standard spec release
  - A CTS keeps evolving to correct shortcomings and improve coverage
    - VESA uses SCR (Spec Change Request)/Errata process to add interim spec updates
    - Interop tests augment compliance test coverage
    - Neither compliance nor interop test reliably catches intermittent failures, but they increase the likelihood of interop of the certified products in the field

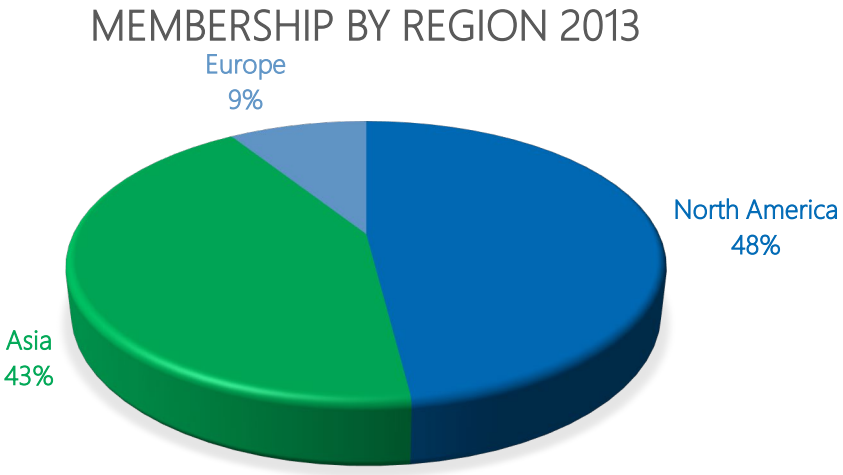
DP Standard and DP CTS

- DP2.1x CTS adds test coverages for UHBR-rate, Panel Replay, LTTPR, DP tunneling, etc.
- However, even those DP products that do not support any new feature in DP2.x need to be compliance tested with DP2.1x CTS with the latest Errata
  - It has added testing of policy updates for interop improvement
- Those compliance test failures caused by inadequacy of compliance test spec and/or implementation of a test equipment may/will be waived

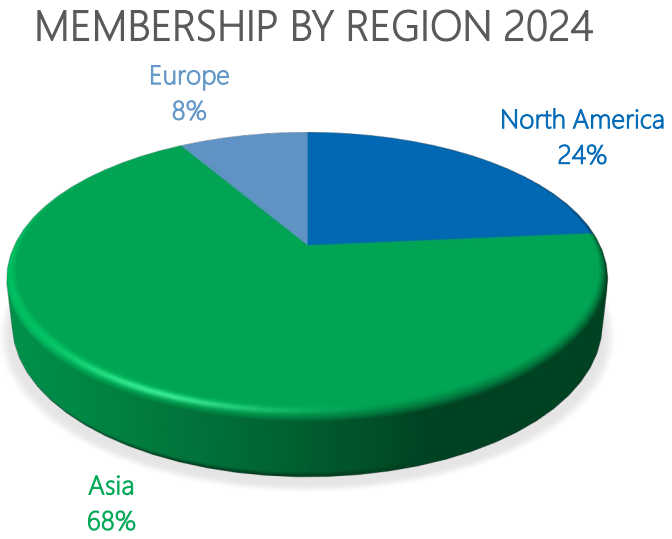
About VESA

- A growing global industry alliance with 366 members. Strong growth in membership.
- Mission to develop, promote and support ecosystem of vendors and certified interoperable products for the electronics industry.
- *Develops OPEN standards, contribution is open to all companies at all stages of development*

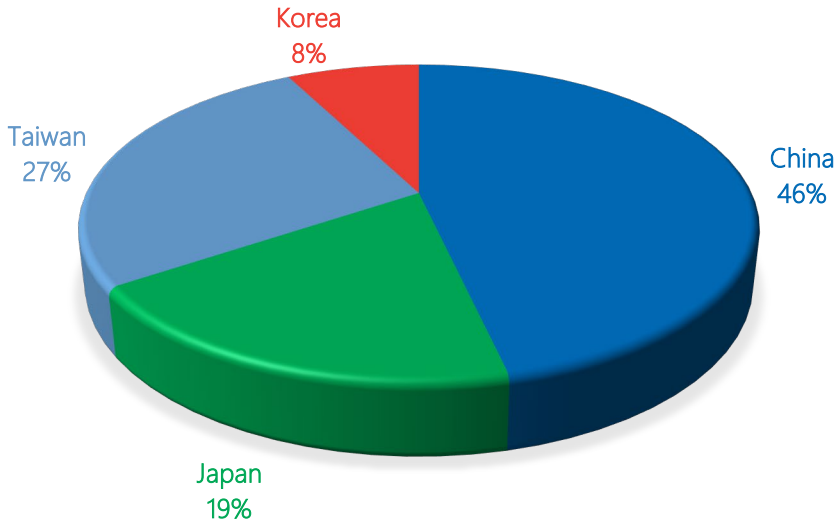
VESA Membership Growth



Changes from 2013:
Asia + 25%
North America – 24%
Europe – 1%



VESA Asia Membership 2024



Many Aspects of Display Technology

Display Interfaces

- DisplayPort
- Embedded DisplayPort
- DisplayPort Alt Mode (Native DisplayPort over USB-C connector)
- DisplayPort Tunneling (USB4 and Thunderbolt)
- Automotive Extensions Services (DP AE specification)
- Multi-Stream Transport (MST)

Display Data Compression

- Display Stream Compression (DSC)
- VESA Display Codec for Mobile (VDC-M)

Display Metrology

- Standardized Display Performance Measurement
- DisplayHDR Certification (High Dynamic Range)
- ClearMR Certification
- AdaptiveSync Display Certification

Display Capability Parameters

- DisplayID
- Extended Display Identification Data (EDID)
- Multi-Display Interface (MST)

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VESA Local Asian Support Capability

- VESA continues to provide local support to Asia to address growing regional membership needs
- China (Mainland) and Taiwan are the fastest growing areas for VESA's membership.
- **Kellen** is VESA's Representative in Asia
- This partnership provide members with a communication option in their native language. Kellen handles membership related activities including, new membership requests, renewals, event support and translation of VESA member messaging, etc.
- AsiaVESA@kellencompany.com or at +86 10 6580 0670

DisplayPort Market Penetration

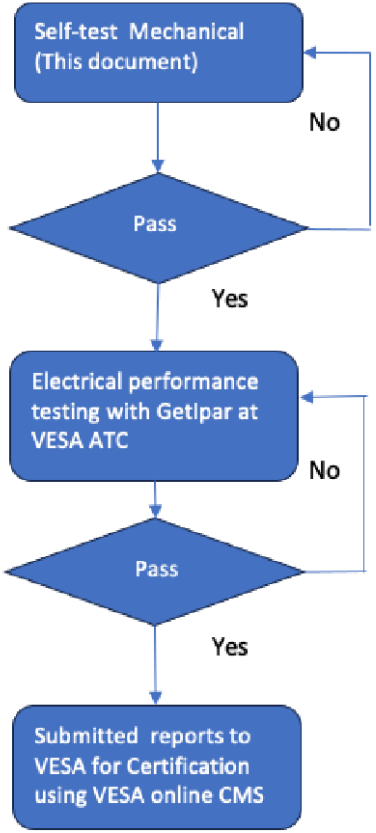
- DisplayPort adoption continues to grow in 2025
- DisplayPort and DisplayPort Alternate Mode over USB-C
  - The common monitor interface for personal computers
  - Supported on the USB-C interfaces
  - Mandated for USB4 and Thunderbolt
  - Automotive integration with DP AE specification
  - Mobile phones with USB-C
- Embedded DisplayPort (eDP)
  - ~95% penetration in notebook PCs, used in many high-end tablets and now automotive

DP54 and DP80 Cable Specification and Certification program

- DP54 and DP80 Certified cables – ensure proper operation at the highest link rates (UHBR10, UHBR13.5 and UHBR20 Gbps)
- Over 150 Enhanced DP cables and connectors have been certified since launch of the Enhanced DP cable and connector certification programs
- DP54 includes and replaces DP40 cable performance tier in 2024
- DP54 cables are required to support UHBR10 and UHBR13.5 link rates, enabling longer cables for sources and sinks that implement 13.5Gbps as highest link rate

Enhanced Connectors

- UHBR rates = the need for high performance DP connectors
- VESA created specification and test requirements for Enhanced DP connectors (fsDP and mDP)
- This includes both right angle and vertical mount connectors



DP80LL (Low Loss) Cable

- To be added in DPv2.1b targeted for 2025 release
- Lower loss than DP80 cable
  - DP80LL: -6.5 dB of loss at 10 GHz
  - DP80: -8.5 dB of loss at 10 GHz
- Feasible of ~ 3-meter LRD active cable
  - Leverages USB4 LRD active cable spec and compliance test methodology
- DP80 cable not deprecated, but LRD active cable required to meet DP80LL budget
  - DP80 passive cable length is limited to ~ 1 meter

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DP2.1 Compliance Tests Update Rev 1.1

Name : Alok K. Soni

Company : Teledyne LeCroy

Date: 10/17/2025 (17-Oct-2025)

Section 4 Source Device Tests :

- 4.2 Source Device Services Test Procedures
- 4.3 Source Device Link Services Test Procedures
- 4.4 Source Device Isochronous Transport Services Test Procedures
- 4.5 Source Device FEC Test Procedures
- 4.6 DSC Source Device Test Procedures
- 4.7 Source Device DisplayPort DisplayID/EDID and Native DisplayID Test Procedures
- 4.8 Source Device DisplayPort Adaptive-Sync Test Procedures
- 4.9 Source Device LTTPR Test Procedures
- 4.10 Source Device MST Compliance Tests
- 4.10.1 Source Device MST Protocol Tests

Section 5 Sink Device Tests :

- 5.2 Sink Device Services Test Procedures
- 5.3 Sink Device Link Services Test Procedures
- 5.4 Sink Device Isochronous Transport Services Test Procedures
- 5.5 Sink Device FEC Test Procedures
- 5.6 Sink DSC Protocol
- 5.7 Sink Device DisplayPort DisplayID/EDID Test Procedures
- 5.8 Sink Device DisplayPort Adaptive-Sync Test Procedures
- 5.9 Sink Device Embedded LTTPR Test Procedures

Section 6 Branch Device Tests :

- 6.1 to 6.9 (Reserved)
- 6.10 Branch Device MST Tests (Normative)
- 6.10.1 Branch Setup 1 Tests
- 6.10.2 Branch Setup 2 Tests
- 6.10.3 Branch Setup 3 Tests
- 6.10.4 Branch Setup 4 Tests
- 6.10.5 Branch Setup 5 Tests
- 6.10.6 Composite Sink (Daisy-chainable Sink) Setup 1 Tests
- 6.10.7 Composite Sink (Daisy-chainable Sink) Setup 2 Tests
- 6.10.8 Composite Sink (Daisy-chainable Sink) Setup 3 Tests
- 6.10.9 Composite Sink (Daisy-chainable Sink) Setup 4 Tests

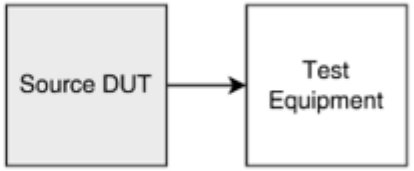
Section 7 LTTPR and DP Tunnel Device Tests :

- 7.1 LTTPR and DP Tunnel Device Test Procedures

VESA Approved DP2.1 Compliance Tests Coverage:

- **Source Device MST tests**
  - Approved Tests with new number (4.10.1.1 to 4.10.1.21)
  - Test setup

Source Setup -1



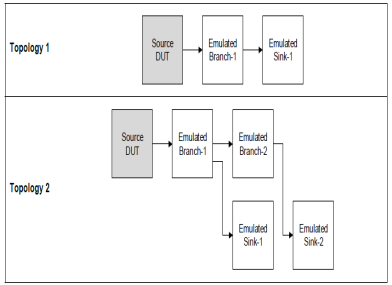


Figure 4-4: Daisy Chain Topologies

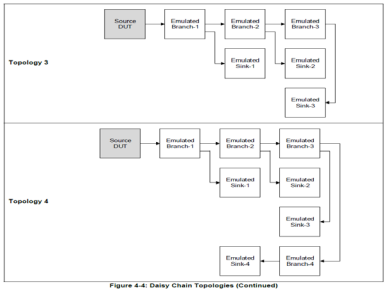


Figure 4-4: Daisy Chain Topologies (Continued)

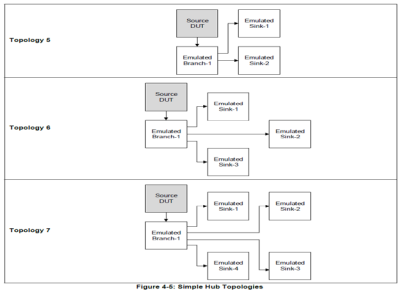


Figure 4-6: Simple Hub Topologies

MST Source CTS CDF entries

S.No	CDF Entry	Default Value
1	MST_TRANSMISSION	Yes
2	MST_MAX_STREAM_COUNT	4
3	MST_UP_REQUEST_SUPPORTED	Yes
4	MST_RSN_REQUEST_SUPPORTED	No
5	MST_MAX_DAISY_CHAIN_SINK_SUPPORTED	4
6	MST_POWER_UP_DOWN_PHY_SUPPORTED	Yes

Source Device MST tests main validation points:

- Capability read, Link Address, Path Enum Resources, Allocate Payload, Video Validation.
- CSN UP Request handling for addition, removal.
- Optional RSN update handling.
- EDID and NDID read, DSC and FEC capability read.
- Handling of error case (Unknow up request, NACK, Incorrect Down Reply or timeout during down reply)
- MST to SST and SST to MST transition.
- In and out of Low Power Mode.
- Writing unique GUIDs.

Source Device MST tests common failure point:

- Variation in AUX Transactions with different Source DUT
- Payload Allocation Calculation Differences
- Handling of CSN Tests during MST Sink or Composite Sink Removal
- Peer Device Type Information in CSN Requests for Removal
- Differences in source DUT behavior during CSN Removal and Addition
- Handling Unknown Up Requests from Branch Devices
- Vendor-Specific Retry Counters for I^2C read/write and remote DPCD operations
- Non-Uniform Timeout Values with different Source DUT
- Source DUT GUID writing behavior differences

VESA Approved DP2.1 Compliance Tests Coverage:

- **Branch Device MST tests**
  - Branch Device Setup1 (loopback to TE with no External Sink) (6.10.1.1 to 6.10.1.12)
  - Branch Device Setup2 (loopback to TE with 1 External Sink) (6.10.2.1 to 6.10.2.10)
  - Branch Device Setup3 (loopback to TE with 2 External Sink) (6.10.3.1 to 6.10.3.14)
  - Branch Device Setup4 (loopback to TE with 3 External Sink) (6.10.4.1 to 6.10.4.14)
  - Branch Device Setup5 (with 4 External Sink) (6.10.5.1 to 6.10.5.4)

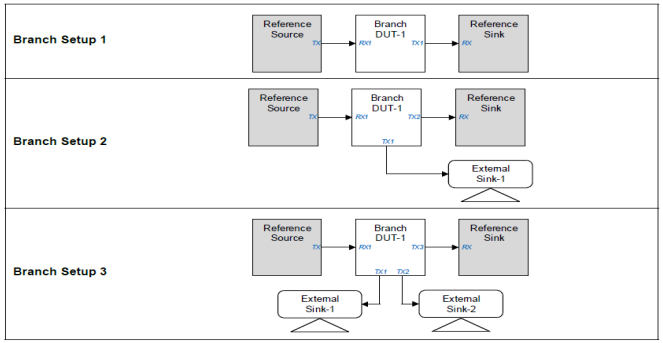


Figure 6-1: MST Branch Device Test Setups

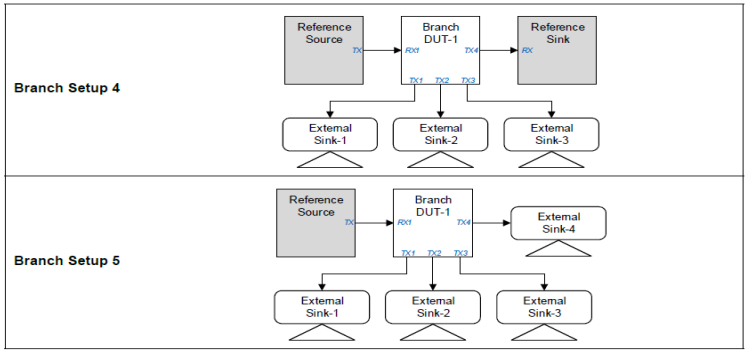


Figure 6-1: MST Branch Device Test Setups (Continued)

Note: External Sinks must be an SST Display that is capable of at least 1,080 p at 60 Hz.

Branch DUT CTS CDF entries

S.No	CDF Entry	Default Value	Range
1	BRANCH_DUT_NO_OF_DFP_DPPORT	0	[1-4]
2	BRANCH_DUT_UFP_PORT_NUM_CONNECTED_TO_TE	0	[1-16]
3	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_TE	0	[1-16]
4	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK1	0	[1-16]
5	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK2	0	[1-16]
6	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK3	0	[1-16]
7	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK4	0	[1-16]
8	BRANCH_DUT_CSN_DFP_BROADCAST	No	Yes/No

Branch DUT tests main validation points:

- Capability validation, forwards up/down request, response for Enum Path Resources, Query Payload, Video Validation for DSC and Non-DSC video.
- Remote DPCD read/write validation via TE internal memory.
- Timeslots calculation and allocations.
- Response for Remote I2C Read, Remote DPCD read/write, link address request.
- Low Power mode enter/exit
- CSN Up/down request generation.
- Time slot increase/decrease/delete/addition

VESA Approved DP2.1 Compliance Tests Coverage:

- **Composite Sink Device MST tests**
  - Composite Sink Device Setup1 (loopback to TE from DP OUT port) (6.10.6.1 to 6.10.6.22)
  - Composite Sink Device Setup2 (loopback to TE from DP OUT port) (6.10.7.1 to 6.10.7.21)
  - Composite Sink Device Setup3 (loopback to TE from DP OUT port) (6.10.8.1 to 6.10.8.5)
  - Composite Sink Device Setup4 (4 DUTs in Daisy chain) (6.10.9.1 to 6.10.9.3)

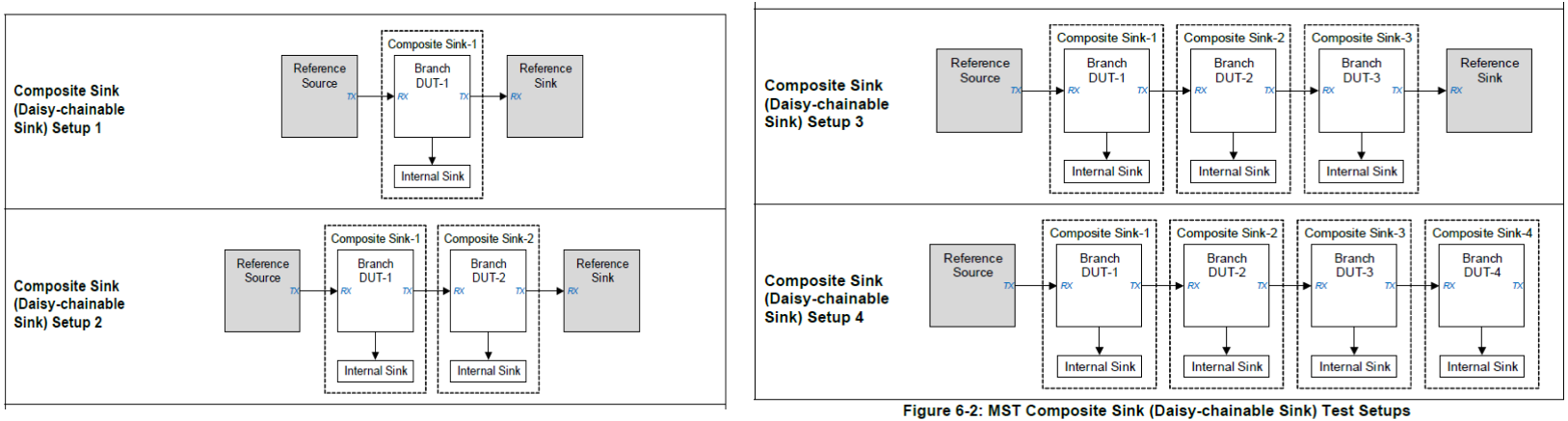


Figure 6-2: MST Composite Sink (Daisy-chainable Sink) Test Setups

Composite Sink DUT tests main validation points:

- Capability validation, forward up/down request, response for Enum Path Resources, Query Payload, Video Validation for DSC and Non-DSC video.
- Remote DPCD read/write validation via TE internal memory.
- Timeslots calculation and allocations.
- Response for Remote I2C Read, Remote DPCD read/write, link address request.
- Low Power mode enter/exit
- CSN Up/down request generation.
- Time slot increase/decrease/delete/addition

Branch Device/Composite Sink common failure point:

- Link Address Reply vs Actual Ports Connected
- Tolerance for PBN value matching and Timeslot allocation
- Query Payload request handling was not implemented by DUTs
- Remote DPCD Read/Write for Branch
- EDID/NDID Read from Branch DUT cache vs “on demand”
- Sideband messaging during Low Power Mode does not work.
- VC Timeslots Increase/Decrease test enhancements

Unique Test numbers for EDID and NDID tests:

- EDID Tests
  - EDID Sink CTS (5.7.15.12) (5.7.16.11)
- NDID Tests
  - NDID Source CTS (4.7.4.5 to 4.7.4.8) (4.7.5.2)
  - NDID Source Adaptive Sync (4.8.1.3 to 4.8.1.4) (4.8.2.4 to 4.8.2.6)
  - NDID Sink CTS (5.4.7.10 to 5.4.7.18) (5.7.5.2) (5.7.6.6 to 5.7.6.10) (5.7.7.7 to 5.7.7.12) (5.7.8.7 to 5.7.8.12) (5.7.9.4 to 5.7.9.6) (5.7.10.4 to 5.7.10.6) (5.7.11.6 to 5.7.11.10) (5.7.12.5 to 5.7.12.8) (5.7.14.9 to 5.7.14.16) (5.7.17.6 to 5.7.17.10)
  - NDID Sink Adaptive Sync (5.8.1.4 to 5.8.1.6)

New Test Additions in Rev 1.1:

- Source Tests:
  - 4.2.2.15 Verification of DPCD 110h Values on USB-C Cable Connect with Source DUT before Link Training
- Sink Tests
  - 5.2.2.11 Verification of DPCD 2217h Values on Upstream Device Disconnect and Power-on Reset

Test Update in Rev 1.1:

- Source Tests:
  - INTRAHOP_AUX_REPLY_INDICATION check before UHBR LT. If set only then Source driver shall write DPCD 102h=00h to clear it, else do not write 102h=00h to clear intra hop as it is already clear. This change affects all UHBR Link Training procedure validation.
  - Same Link Config retry 1 time or 2 times, controlled by CDF and affect all Link Training fallback tests.
  - 4.3.1.21 update for 20 loop or max time budget during EQ loop not able to achieve EQ lock.
  - 4.2.2.13 update check defer after LTTPR discovery.
  - 4.9.1.22 LTTPR discovery check validation handling after HPD may not be the first transaction.
  - 4.3.3.2 Least pack format change for 1L UHBR10 for video test.
  - Minor update in 4.7.5.1
- Sink Tests:
  - 5.2.2.5 do not check vendor Specific fields
  - 5.3.1.5 EQ Done bit validation removed. Only use Symbol lock for validation.
  - Some Sink Tests will be skipped if DP Tunnel is detected.
  - Minor update in 5.7.14.1, 5.6.2.[12/13/14]
- LTTPR Device Tests:
  - 7.1.1.4 test, wait for 10 sec cable unplug before switching to NON LTTPR Mode. Update clarification for Tunnel working as retimer.
  - 7.1.5.1 correction of Symbol error counter setting on LTTPR Address range, not the sink DPCD.

- Q/A

DisplayPort Electrical Testing Overview

Victor Chiu & Francis Liu
Keysight Technologies
10/17/2025

Agenda

- DP2.1 Electrical Compliance Test Requirements
- DP2.1 PHY Updates
- DP2.1 Transmitter Test
- DP2.1 Receiver Test
- eDP PHY Electrical Conformance Testing

DP2.1a Electrical Compliance Test Requirement

DisplayPort Interface

Main Link

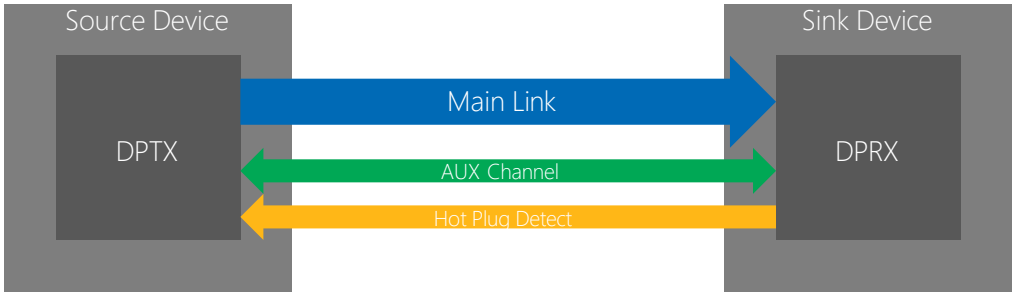
- Display data transfer
- 4 unidirectional high-speed lanes
- Multiple bitrates supported

AUX Channel

- Link management
- Test mode control
- 1 bidirectional low-speed lane

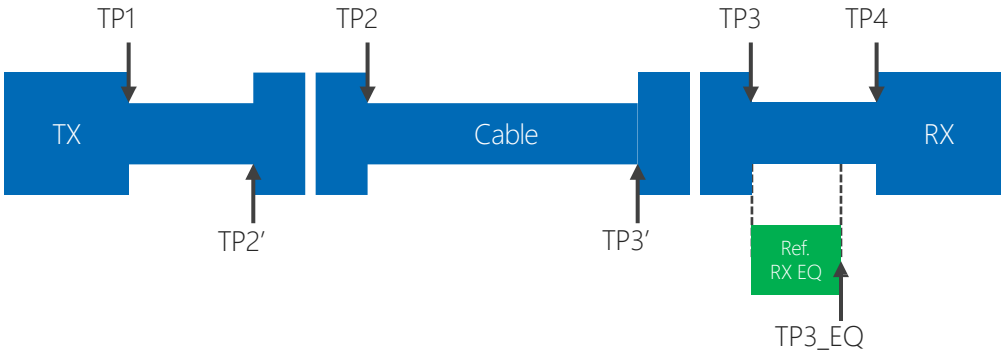
Hot Plug Detect

- Source detects presence of sink
- Sink notifies of status changes via IRQ



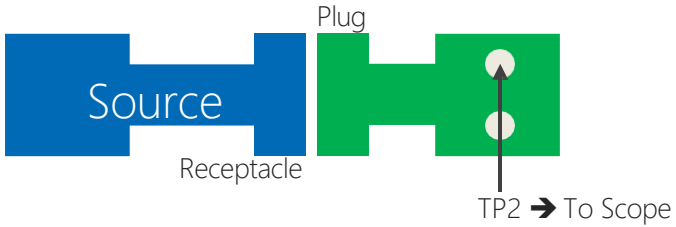
Test Points

Test Point	Definition
TP1	Source transmitter pins.
TP2	Test interface of a TPA, next to mated connection to a DP source.
TP2′	RX JTOL signal injection point for DUTs with plug.
TP2_CTLE	RX JTOL calibration and test point for DUTs with plug.
TP3	Test interface of a TPA, next to mated connection to a DP sink.
TP3′	Signal injection point to a DP sink.
TP3_EQ	TP3 using a defined DP cable model with equalization applied.′
TP3_CTLE	TP3 using a defined HBR3 cable model with CTLE applied.
TP3_DFE	TP3 using a defined HBR3 cable model with CTLE and DFE applied.
TP4	Sink receiver pins.

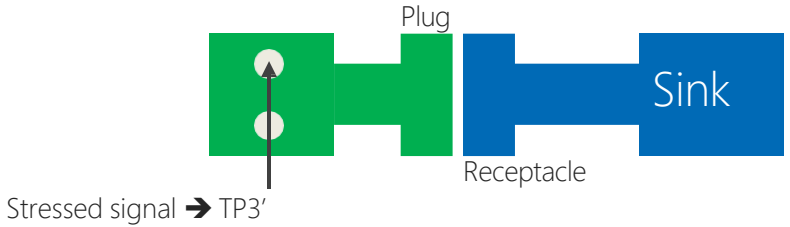


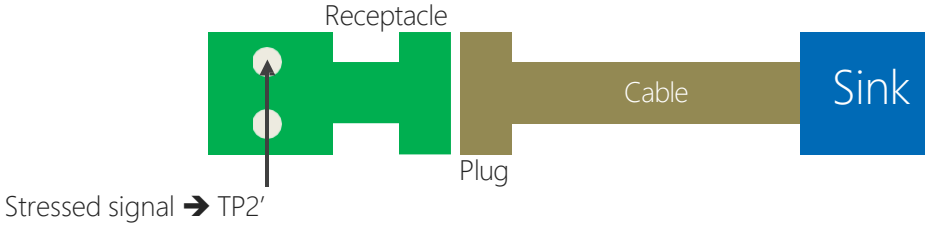
Test Point Access Examples

DPTX Testing



DPRX Testing





How to test the PHY layer?

Source

- Configure the source to output test patterns with certain drive settings ➔ **AUX controller**
- Embed worst-case channels, apply equalization on the oscilloscope
- Run measurements

Sink

- Generate the stress signal with a pattern generator
- Guide the sink through Link Training ➔ **AUX controller**
- Read built-in error counter ➔ **AUX controller**

DP2.1 PHY Updates

Electrical Updates from DP2.1 to DP2.1a to DP2.1b

- There are minimal changes in 8b/10b electrical compliance testing.
- A new DP54 cable has been introduced in DP2.1a for UHBR13.5.
- The UHBR13.5 Source Enhanced FSDP testing will utilize the new DP54 cable model.
- A new DP80LL cable has been introduced in DP2.1b for UHBR20.
- The UHBR20 Source with 9dB loss budget will utilize the DP80LL cable.
- Changes in test limits primarily affect Source Testing.

- UHBR10
  - DPTX TP2
    - Total Jitter =380 mUI
    - Data-Dependent Jitter =160 mUI
    - Eye Width = 600 mUI
    - Eye Height = 242 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 185 mV
  - DPTX TP3_EQ
    - Total Jitter =450 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 115 mV
  - DPRX TP3_EQ
    - Total Jitter =485 mUI
    - Data-Dependent Jitter =240 mUI
    - Eye Width = 540 mUI
    - Eye Height = 112 mV
- UHBR20
  - DPTX TP2
    - Total Jitter =435 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 240 mV
  - DPTX TP3_EQ
    - Total Jitter =455 mUI
    - Data-Dependent Jitter =210 mUI
    - Eye Width = 560 mUI
    - Eye Height = 100 mV
  - DPRX TP3_EQ
    - Data-Dependent Jitter =255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV

- UHBR10
  - DPTX TP2
    - Total Jitter =440 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 550 mUI
    - Eye Height = 162 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 200 mV
  - DPTX TP3_EQ
    - Total Jitter =515 mUI
    - Data-Dependent Jitter =245 mUI
    - Eye Width = 520 mUI
    - Eye Height = 80 mV
  - DPRX TP3_EQ
    - Total Jitter =530 mUI
    - Data-Dependent Jitter =260 mUI
    - Eye Width = 520 mUI
    - Eye Height = 73 mV
- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI

- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI

- UHBR20
  - DPTX TP2 EnhDP DP80
    - Total Jitter = 480 mUI
    - Data-Dependent Jitter = 200 mUI
    - Eye Width =540 mUI
    - Eye Height = 240 mV
  - DPTX TP2 EnhDP DP80LL
    - Total Jitter = 495 mUI
    - Data-Dependent Jitter = 220 mUI
    - Eye Width =530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ for all connector Type
    - Total Jitter = 500 mUI
    - Data-Dependent Jitter = 210 mUI
    - Eye Width =560 mUI
    - Eye Height = 100 mV
  - DPRX TP3EQ for all connector type
    - Data-Dependent Jitter = 255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV

DP2.1 PHY CTS Errata

- Clarification on 8b/10b SSC Modulation Deviation Limit
- Test fixture insertion loss update
- FFE Preset 15 measurement update
- LTTPR Frequency Variation test update
- Eye Height and Mask requirement update for UHBR Rates
- BERT Preset Calibration

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DP2.1 Transmitter Test

Electrical Transmitter Tests

Item	Name	Normative/ Informative
3.1	Eye Diagram Test	Normative
3.2	HBR/RBR Non-PE Level Verification Test	Normative
3.3	HBR/RBR PE Level Verification and Maximum Differential Peak-to-Peak Voltage Test	Normative
3.4	HBR3/HBR2 PE Level and Equalization Verification Test	Normative
3.5	HBR3/HBR2 $V_{TX\_DIFFp\text{-}p\_MAX}$ Test	Normative
3.6	Inter-pair Skew Test	Informative
3.7	Intra-pair Skew Test	Informative
3.8	AC Common Mode Noise Test	Informative
3.9	Non-ISI Jitter Measurement Test	Normative
3.10	HBR3 TX Differential RL Test	Informative
3.11	TJ/RJ/DJ Measurement Tests	Normative
3.12	Main-Link Frequency Compliance Test	Normative
3.13	Spread-spectrum Modulation Frequency Test	Normative
3.14	Spread-spectrum Modulation Deviation Test	Normative
3.15	dF/dT Spread-spectrum Deviation High-frequency Variation Test	Informative
xx	Embedded Re-timer Frequency Variation Test	Normative

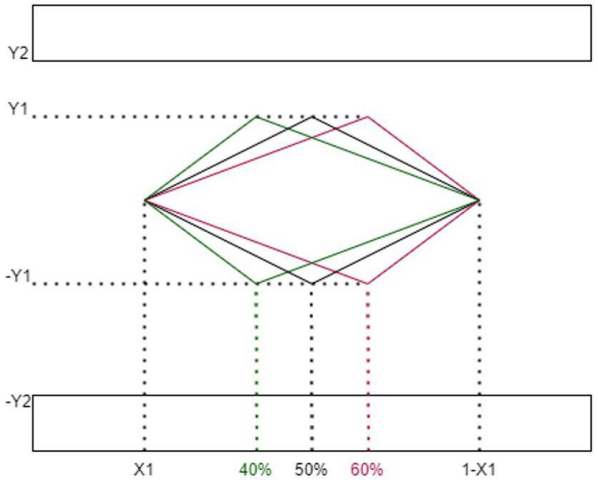
8b/10b

Item	Name	Normative/ Informative
4.2	Preset and CTLE-DFE Declaration	Normative
4.3	UHBR Source Transmitter Equalization	Normative
4.4	UHBR Bit Rate	Normative
4.4	UHBR Unit Interval	Informative
4.5	UHBR SSC Down Spread Range, Rate, Phase Deviation, and Slew Rate	Normative
4.6	UHBR Embedded Re-timer Frequency Variation	Informative
4.7	UHBR TP2 Eye at 1E-6 BER	Normative
4.8	UHBR TP2 Jitter at 1E-9 BER	Normative
4.9	UHBR AC Common Mode Nosie Test	Informative
4.10	UHBR TP3_EQ Eye at 1E-6	Normative
4.11	UHBR TP3_CTLE Jitter at 1E-9	Informative
4.12	UHBR Transmitter Return Loss	Informative

128b/132b

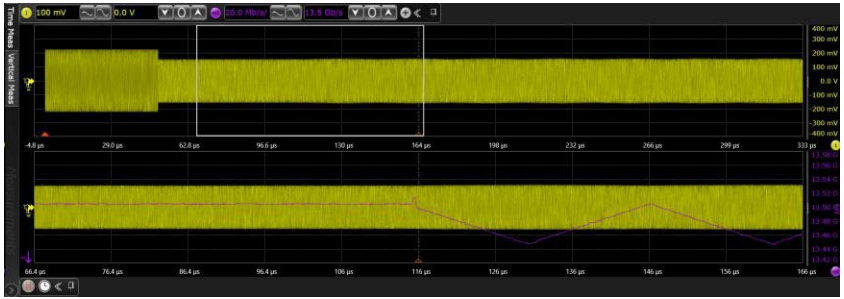
UHBR Eye Mask Update

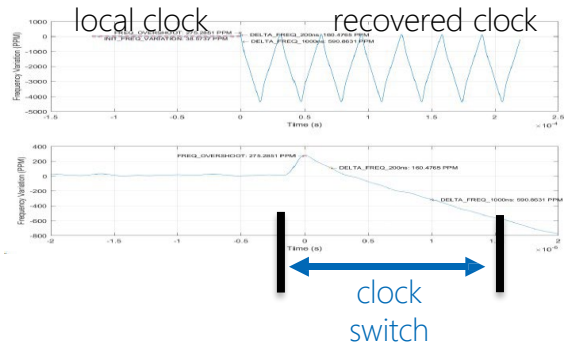
- If original eye mask fails, then modified mask will be used to re-test.
- Modify mask must comply the Y1 and X1 as per the DP 2.1 PHY CTS



LTTPR Frequency Variation Test

- LTTPRs are needed as total channel loss increases with the PHY rate
  - Longer channel
  - More complex link training
- LTTPR Re-timer Clock Switch Test Mode
  - DPCD 0x0010B – 0x0010Eh [7] =1
- Initial Test Challenges
  - Entering Clock Switch test mode
  - Triggering on LTTPR local clock event





DP TX testing challenges

- The test time for DP TX is significant
- DP Source not supporting PHY Test Automation
  - DP Source does not transmit the compliance pattern

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DP2.1 Receiver Test

Electrical Receiver Tests

Item	Name	Normative/ Informative
5.1	8b/10b DP Sink JTOL Test	Normative

Item	Name	Normative/ Informative
6.1	128b/132b DP UHBR Sink JTOL Test	Normative

Item	Calibration Point	Name
5.1.3.1.1	TP1-TP3	HBR3 Jitter Calibration
5.1.3.1.2	TP1-TP3	HBR2 Jitter Calibration
5.1.3.1.3	TP1-TP3	HBR Jitter Calibration
5.1.3.1.4	TP2/TP3	HBR3 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR2 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR Eye Height and Total Jitter Calibration
5.1.3.1.5	TP1/TP3	HBR3/HBR2/HBR Crosstalk Calibration
5.1.3.2	TP2/TP3	RBR Jitter Calibration
5.1.3.2	TP3	RBR Eye Height Calibration
5.1.3.2.1	TP3	RBR Crosstalk Calibration

Item	Calibration Point	Name
6.1.3.1.4.1	TP1	AC Common-Mode Interference Calibration
6.1.3.1.4.2	TP1	Random Jitter Calibration
6.1.3.1.4.3	TP1	Periodic Jitter Calibration
6.1.3.1.4.4	TP1	Total Jitter Calibration
6.1.3.1.4.5	TP1	Eye Height Calibration
6.1.3.1.5	TP3	Insertion Loss Calibration
6.1.3.1.6	TP3	Eye Diagram Calibration

BERT Preset Calibration

- To verify the BERT FFE as outlined in the DP 2.1 PHY CTS specification
- The Preset calibration check can assist in identifying setup problems.

Set Preset []	Expected Preshoot [dB]	Measured Preshoot [dB]	Expected Deemphasis [dB]	Measured Deemphasis [dB]	Coeff_1 []	Coeff0 []	Coeff1 []	Pass/Fail
1	0.00	0.10	-1.90	-1.75	0.030	0.870	-0.100	Pass
2	-3.10	-3.16	-3.60	-3.57	0.130	0.690	-0.180	Pass
3	0.00	0.03	-5.00	-4.81	0.030	0.750	-0.220	Pass
4	0.00	-0.20	-8.40	-8.25	0.030	0.655	-0.315	Pass
5	0.90	1.13	0.00	0.20	-0.035	0.965	0.000	Pass
6	1.10	1.18	-1.90	-1.86	-0.020	0.880	-0.100	Pass
7	1.40	1.35	-3.80	-3.60	-0.020	0.810	-0.170	Pass
8	1.70	1.65	-5.80	-5.61	-0.020	0.750	-0.230	Pass
9	2.10	2.03	-8.00	-7.89	-0.020	0.690	-0.290	Pass
10	1.70	1.82	0.00	0.13	-0.080	0.920	0.000	Pass
11	2.20	2.49	-2.20	-2.24	-0.080	0.820	-0.100	Pass
12	2.50	2.31	-3.60	-3.47	-0.060	0.790	-0.150	Pass
13	3.40	3.57	-6.70	-6.64	-0.070	0.700	-0.230	Pass
14	3.60	3.67	0.00	0.01	-0.170	0.830	0.000	Pass

DP RX testing challenges

- Error count registers not enabled in DP Sink
  - Error count register always report 0 errors
  - USB-C Lane orientation causing failure in error counter and link training
- Calibrations take a significant amount of time
  - Different setup needs for 8b/10b and 128b/132b

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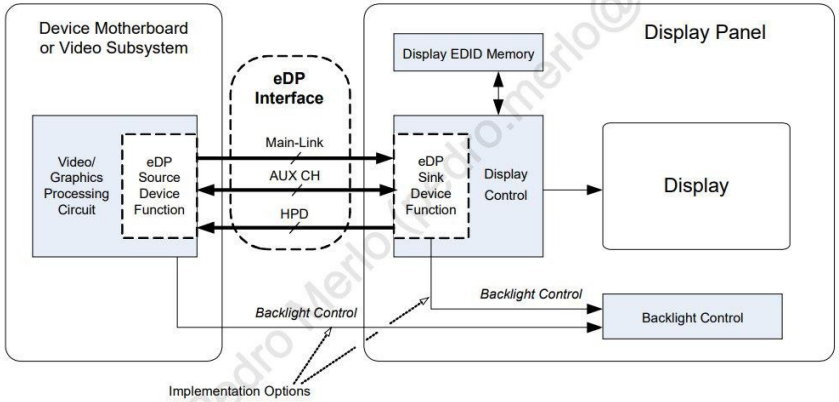
Embedded DisplayPort

eDP

- Standardized features and interoperability guidelines
  - Feature set determined by the system integrator
- Current specification is eDP2.0
  - Based on DP2.1
- No compliance program = Conformance Test!!



eDP2.0 Update

- eDP2.0 v1.0 published in September 2024
- Supports 128b/132b encoding
- Supports UHBR data rates
  - UHBR10, UHBR13.5 and UHBR20
- Leverages worst-case end-to-end link budget from DP2.1

Key Differences eDP2.0 vs DP2.1

Required

- DPCD registers for eDP
- Reduced AUX timing
- Enhanced framing
- Fast link training (sink)
- eDP-specific sink noise/jitter budget, reference EQ

Optional

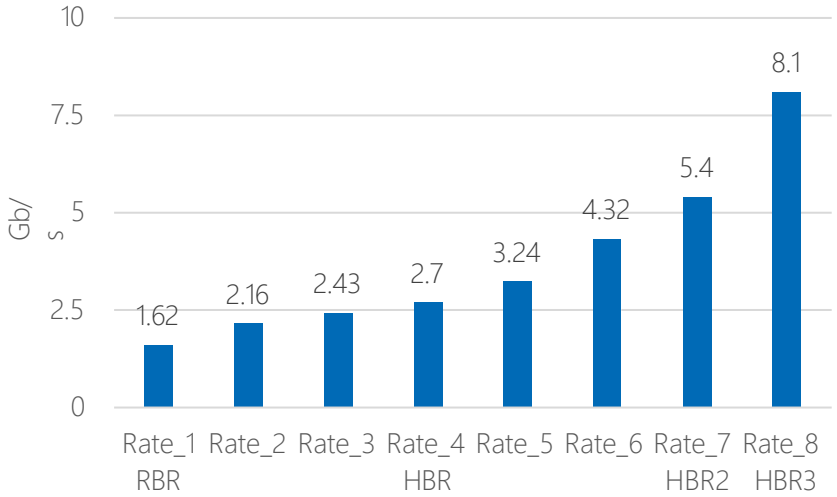
- Low AUX voltage swing
- Source detection by way of AUX CH
- STREAM_STATUS_CHANGED bits support
- GUID registers support
- Fast link training (host)
- Reduced main-link voltage swing level
- EDID
- HPD pin on sink device

Recommended

- Fewest number of lanes possible

Main Link Differences

- Eight 8b/10b rates, and Three UHBR rates
- Custom rates supported



- TP3_EQ total jitter budget
- BER = 10^{-9}

Test Point	Description	I/N	DJ_{MAX}	TJ_{MAX}
TP1	eDPTX package pin	Informative	0.17 UI	0.27 UI
TP2	Source device eDP cable connector	Informative	N/A	N/A
TP3	Sink device (panel) eDP cable connector	-	-	-
TP3_EQ	After reference RX equalizer	Normative	0.41 UI	0.50 UI
TP4	eDPRX package pins	Informative	0.46 UI	0.55 UI

AUX Channel Differences

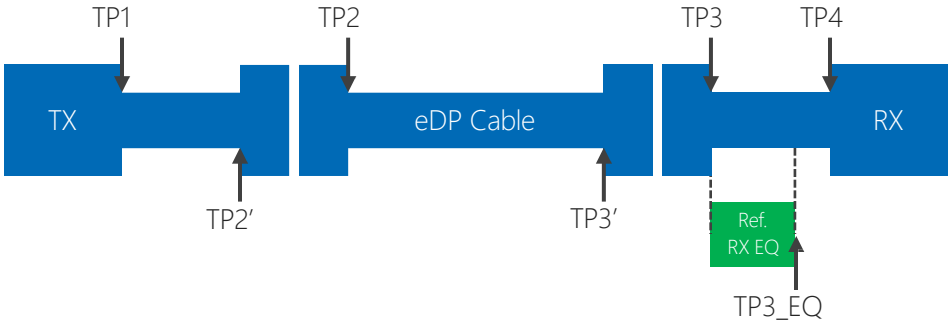
- No AC-coupling capacitors on Sink device side
- No pull-up/-down resistors
- Why?
  - The Sink device does not monitor the common mode voltage on AUX_CH_P and AUX_CH_N for Source device Hot Plug/Unplug and powered/unpowered detection

eDP Electrical Specification

- Low voltage swing levels
- Framework to apply optional customized voltage swings
- Reduced RX differential voltage sensitivity
- New transfer rates
- Framework to apply jitter specifications to optional customized frequencies
- Same Link Training procedures and voltage swing tables like DP, but with lower signal voltages

eDP Transmitter Test

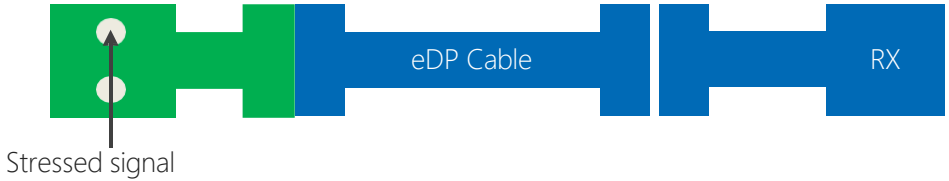
- Test Point/Fixture



Recommended Source Main-Link TX Electrical Specification
Link Rate
Unit Interval
Total Jitter
Residual ISI
Non-ISI
Eye Diagram

eDP Receiver Test

- Test Point/Fixture



RX Test
Sink JTOL Test

Calibration Point	RX Calibration
TP1	Sinusoidal Jitter Calibration
TP1	Random Jitter Calibration
TP3	Residual ISI
TP3	Eye Diagram
TP3	Crosstalk

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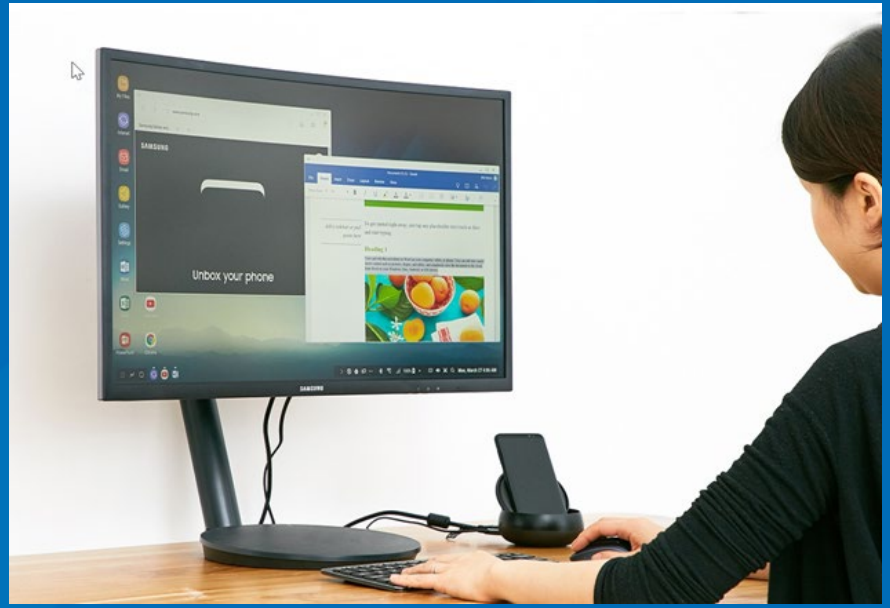
Thank You!

DP Alt-Mode 2.1: A Closer Look



Henry Tsai
Teledyne LeCroy
October 2025

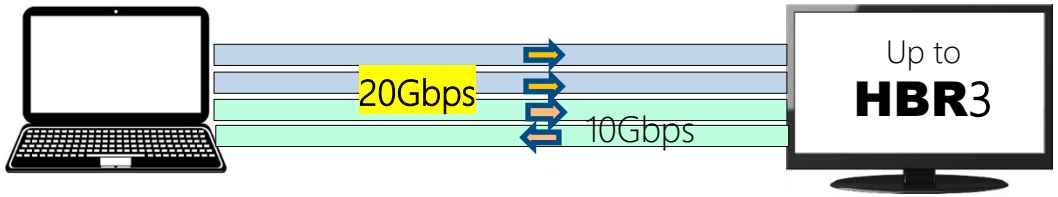
A Closer Look at DP Alt-Mode 2.1

- Agenda
  - DisplayPort 2.1 & Alt Mode Updates (Late 2023)
    - DP Alt Mode Overview
    - Type-C pin configurations
  - DPAM 2.1 Version Resolution
  - DPAM 2.1 Cable Discovery
  - DPAM 2.1 Configuration walk-through
  - DPAM 2.1 Compliance Overview

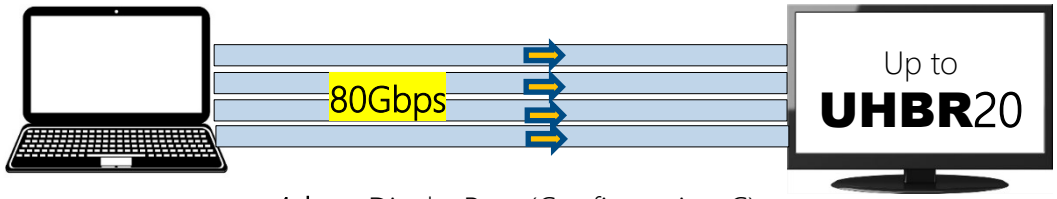
Alternate-Mode Usage Cases

- Alternate Modes
  - Goal – Leverage multi-lane Type-C cable to support alternate communications standards over a single physical cable
- Applications
  - DisplayPort 1.4 / 2.1
  - Thunderbolt™ 3

DP Alt-mode Lane Configurations



2-lane DisplayPort & 2-lane USB (Configuration D)



4-lane DisplayPort (Configuration C)

USB 3.2 DisplayPort Native

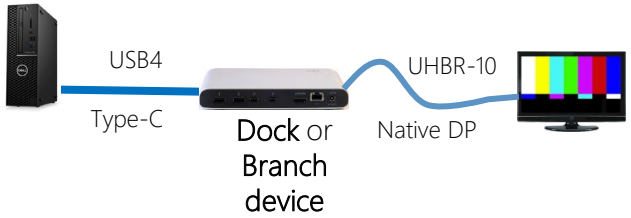
- Two diff pairs allow up to HBR3 (config: D)
- Four diff pairs allow up to UHBR20 (config: C, E)

DisplayPort 2.1 & DPAM 2.1 Updates

What is new in DisplayPort 2.1 Base Spec

- **DP56/DP80 –** Allows UHBR20 ‘native’ DP cables/connectors
- **Active Cables** (LTTPR Retimer / Linear Redriver

- **USB4 PHY** Electrical specification alignment (IR-loss…etc)
  - USB4 tunnel changes for UHBR rates
- **Revised Link Training -** DPCD registers as LTTPR “Intra-Hop AUX”
- **AUX-less ALPM** - Power management control over high-speed lines
- **CableID** allows DP-Tx/DP-Rx to identify DP56 / DP80 cables
- Lots of Clarifications and improvements



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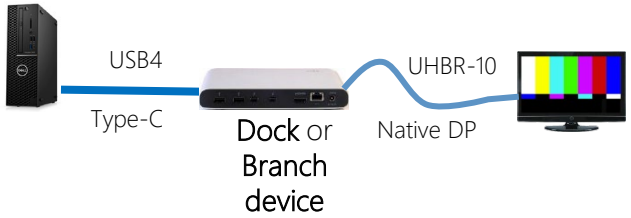
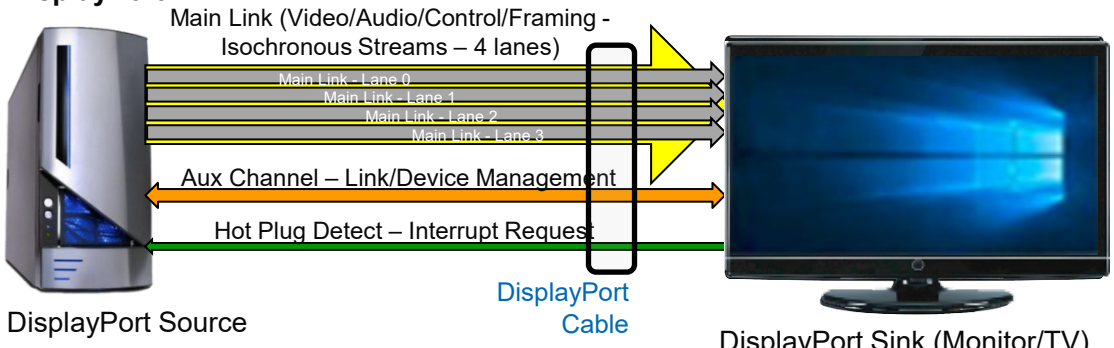


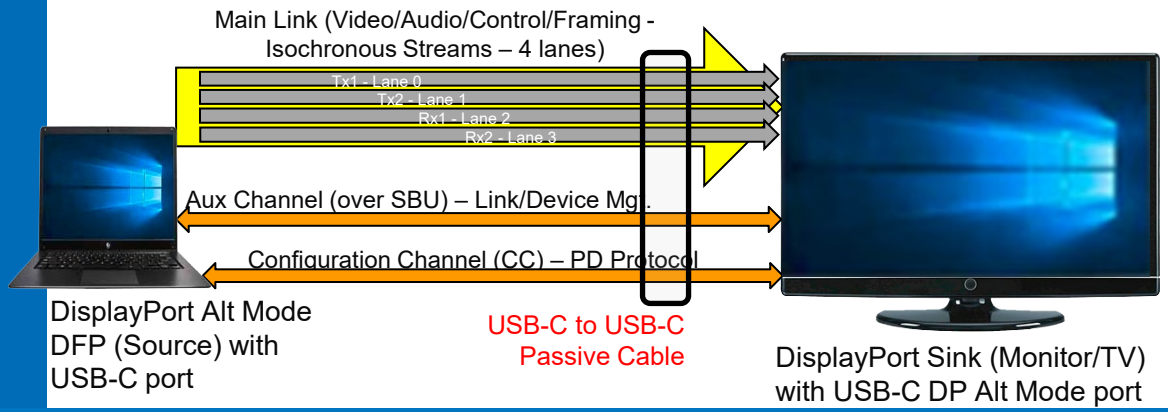
USB-C DP Alt Mode Signaling

DisplayPort



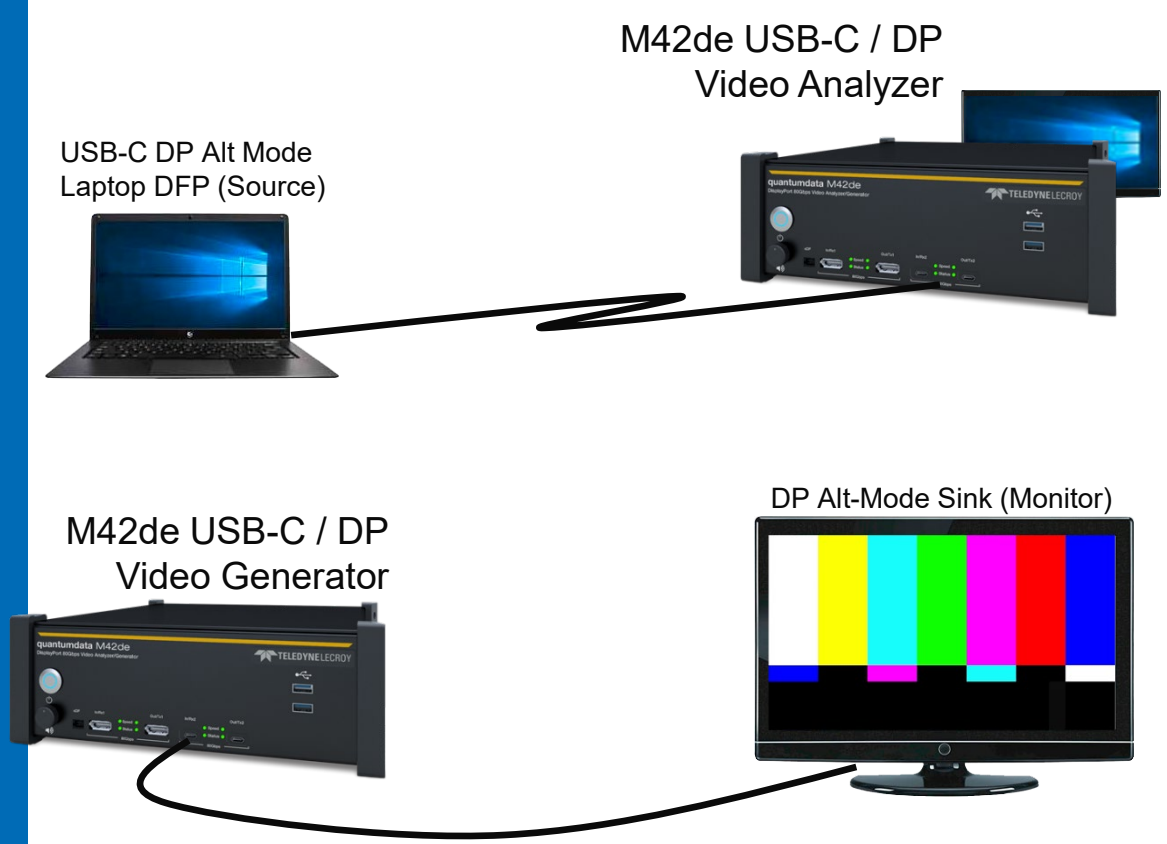
- Main Link: high-bandwidth channel used to transport video/audio
  - 1, 2 or 4 Lane Configurations
  - Link rates:1.62Gbps – 20Gbps
- Aux Channel:
  - Bidirectional 1Mbps
- Hot plug signal:
  - Connection Detection
  - Interrupt mechanism

USB-C DP Alt Mode



- Repurposes USB-C differential pairs as high-bandwidth channel for video/audio
  - 1, 2 or 4 Lane Configurations.
  - Link rates:1.62Gbps – 20Gbps
- USB-C Sideband Use (SBU)
  - Bidirectional
  - DP Aux transactions
- USB-C Configuration Channel (CC)
  - Bidirectional, half duplex
  - Used for PD Power negotiation and Alt Mode entry

M42de Supports DP Alt-Mode SRC/SNK Testing

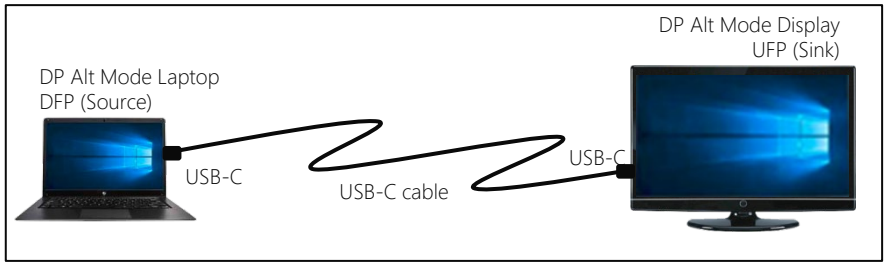


- Protocol Analysis - Source Testing
  - Sink emulation EDID, DPCD.
  - Protocol Analysis – Main Link & Aux
  - Compliance Testing - Link Layer, (including FEC), DSC, HDCP.
- Video Generation - Sink Testing
  - Source emulation and Link Training control.
  - Video Pattern Testing –generation of Display Stream Compression (DSC) Panel Replay and FEC.
  - Compliance Testing (Link Layer, FEC, HDCP).
- DP Alt Mode Testing
  - Run all VESA source and sink testing through the USB-C DP Alt Mode ports.

USB-C DP Alt Mode – High Level Overview

Key roles for PD/CC messages:

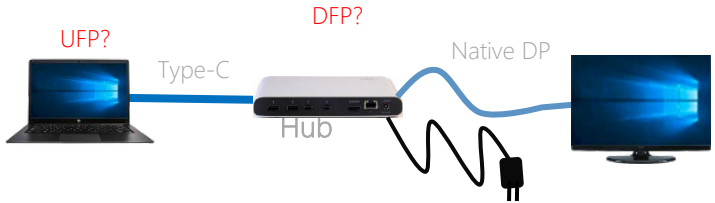
1. Discovery DP Alt Mode Capabilities
2. Decide which Pin Configuration to use
   - DP Sink
   - Active cables

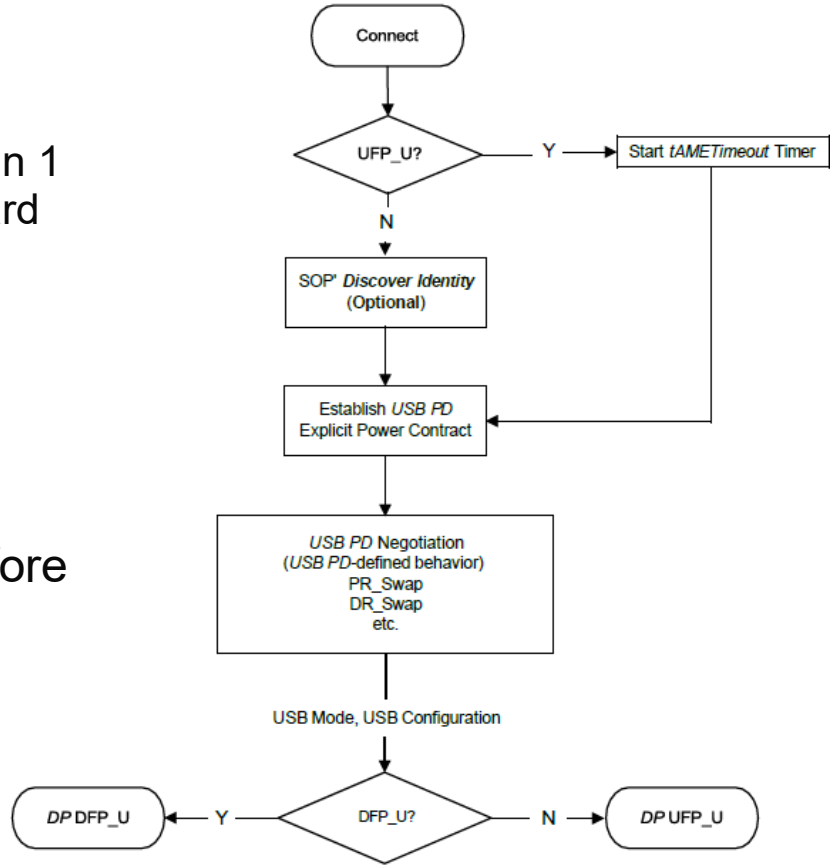


- Captures PD and AUX–
  - Sequential list of transactions
  - Shows full DP-Alt Mode entry flow
  - Captures all AUX channel transactions
  - Real-time

Getting Ready for DP Alt Mode…

- Initial Type-C State Detection
  - ***Starts tAMETimeout*** timer
    - If Sink does not enter DP Alt Mode within 1 Sec UFP_U shall present a USB billboard
- Negotiate initial PD Power Contract
- Establish port's data role
  - Port assumes the role of either:
    - DFP_U
    - UFP_U
- Complete any other PD transactions before starting DisplayPort Alt Mode (ie: PR_Swap)





DPAM 2.1 Version Resolution

Key Changes: DISCOVER MODE Response

DPAM Version[j]	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

SOP

SOP'

DPAM2.0

Table 5-5: DP Capabilities (VDO in the Responder *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED. 01b = DP Sink device-capable (including DP Branch device). 10b = DP Source device-capable (including DP Branch device). 11b = Both DP Source and Sink device-capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP Standard* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = DP interface is presented on a USB-C plug. 1 = DP interface is presented on a USB-C receptacle.
7	*USB 2.0* Signaling Not Used	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)	00000000b = DP Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c][d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	00000000b = DP Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c][g] XXX1XXXXb = Pin Assignment E is supported.[b] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
31:24	RESERVED	RESERVED (always 00b).

DPAM2.1

Table 5-5: DP Capabilities (VDO in the Responder USB PD *Discover Modes*

Bit(s)	Description	Values[a]
1:0	**Port Capability**	00b = RESERVED 01b = *DP* Sink device-capable (including *DP* P… device). 10b = *DP* Source device-capable (including … device). 11b = Both *DP* Source and Sink device-cap…
5:2	**Signaling for Transport of DisplayPort Protocol**	XXX1b = Supports *DP* bit rates and electri… gs (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	**Receptacle Indication**	0 = *DP* interface is presented on … plug. 1 = *DP* interface is presented … C receptacle.
7	**USB 2.0 Signaling Not Used**	0 = *USB 2.0* may be needed … A7 –or– B6 – B7 while in DisplayPort Configura… 1 = *USB 2.0* is not needed … – A7 –or– B6 – B7 while in DisplayPort Configu…
15:8	**DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)**	00000000b = *DP* Sou… e pin assignments are not supported. XXXXXXX1b = R… ED. XXXXXX1Xb = R… ED. XXXXX1XXb … Assignment C is supported.[b] XXXX1XXXb … in Assignment D is supported.[c][d] XXX1XXXXb … Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	**DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)**	0000…00b = *DP* Sink device pin assignments are not supported. XX…XXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c][g] XXX1XXXXb = Pin Assignment E is supported.[b] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
29:24	**RESERVED**	RESERVED (always 00b).
31:30	**DPAM Version[j]**	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

DPAM2.0

SOP' Cable DP Capabilities (DPAM2.0)		
Bits	Field	CTS Value
B31-24	Reserved	0000 0000b
B23-16	DP Sink Device Pin Assignment Supported	0000 1100b
B15-8	DP Source Device Pin Assignment Supported	0000 1100b
B7-6	Reserved	00b
B5-2	Signal for Transport of DP Protocol	0001b
B1-0	Reserved	00b

DPAM2.1

Bit(s)	Description	Values
1:0	**RESERVED**	RESERVED (always 00b).
5:2	**Signaling for Transport of DisplayPort Protocol[b]**	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[c]
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**DP Source Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported. 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
23:16	**DP Sink Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
25:24	**RESERVED**	RESERVED (always 00b).
26[d]	**UHBR13.5**	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[e]
27	**RESERVED**	RESERVED (always 0).
29:28[f]	**Active Component**	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30	**DPAM Version**	00b = Original version. 01b = Version 1.

Discover Modes Response from UFP

Discover Modes Response from Cable

Key Changes: DISCOVER MODE Response

Discover ID and *Discover Modes* (DP Capabilities) Response

will be identified by having a non-zero value in bits 31:24 of the VDO. The DFP_U shall examine the list of modes returned until it finds 0s in bits 31:24 of the VDO and a non-zero value in bits 23:0 of the VDO (i.e., DisplayPort capabilities). The DFP_U and UFP_U shall use the corresponding offset (indexed from 1) as the Object Position in the Enter Mode, DisplayPort Configure, DisplayPort Status Update, Attention, and Exit Mode commands.

SOP

DPAM2.0

Table 5-5: DP Capabilities (VDO in the Responder *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED. 01b = DP Sink device-capable (including DP Branch device). 10b = DP Source device-capable (including DP Branch device). 11b = Both DP Source and Sink device-capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP Standard* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = DP interface is presented on a USB-C plug. 1 = DP interface is presented on a USB-C receptacle.
7	*USB 2.0* Signaling Not Used	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)	00000000b = DP Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c,d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	00000000b = DP Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[f,g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
31:24	RESERVED	RESERVED (always 00b).

DPAM2.1

Table 5-5: DP Capabilities (VDO in the Responder USB PD *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	**Port Capability**	00b = RESERVED 01b = *DP* Sink device-capable (including *DP* Branch device). 10b = *DP* Source device-capable (including *DP* Branch device). 11b = Both *DP* Source and Sink device-capable.
5:2	**Signaling for Transport of DisplayPort Protocol**	XXX1b = Supports *DP* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1Xb = RESERVED. 1Xb = RESERVED.
6	**Receptacle Indication**	0 = *DP* interface is presented on a *USB-C* plug. 1 = *DP* interface is presented on a *USB-C* receptacle.
7	**USB 2.0 Signaling Not Used**	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	**DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)**	00000000b = *DP* Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c,d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	**DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)**	00000000b = *DP* Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[f,g] XXX1XXXXb = Pin Assignment E is supported.[h] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
29:24	**RESERVED**	RESERVED (always 00b).
31:30	**DPAM Version**[i]	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Discover Modes Response from UFP

SOP'

DPAM2.0

SOP' Cable DP Capabilities (DPAM2.0)		
Bits	Field	CTS Value
B31-24	Reserved	0000 0000b
B23-16	DP Sink Device Pin Assignment Supported	0000 1100b
B15-8	DP Source Device Pin Assignment Supported	0000 1100b
B7-6	Reserved	00b
B5-2	Signal for Transport of DP Protocol	0001b
B1-0	Reserved	00b

DPAM2.1

Bit(s)	Description	Values
1:0	**RESERVED**	RESERVED (always 00b).
5:2	**Signaling for Transport of DisplayPort Protocol**[b]	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1Xb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[c]
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**DP Source Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported. 10b = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
23:16	**DP Sink Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10b = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
25:24	**RESERVED**	RESERVED (always 00b).
26[d]	**UHBR13.5**	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[e]
27	**RESERVED**	RESERVED (always 0).
29:28[f]	**Active Component**	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30	**DPAM Version**	00b = Original version. 01b = Version 1.

Discover Modes Response from Cable

Structured VDM Version

- SVDM Version Revised in Power Delivery Spec (Revision 1.3; Version 1.6)
  - Adds Major & Minor “VDM” version fields

12:11	**Structured VDM Version (Minor)[a]**	Version number (Minor) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier 01b = Version 2.1 All other values are RESERVED.
14:13	**Structured VDM Version (Major)[a]**	Version number (Major) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier. 01b = Version 2.x. (x indicates SVDM minor version) All other values are RESERVED.

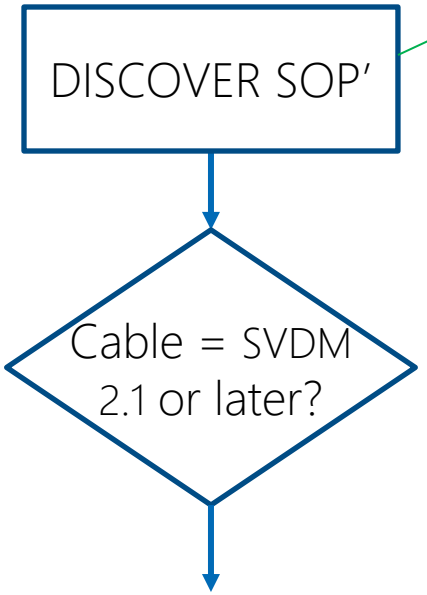
Table 5-4: SVDM Header

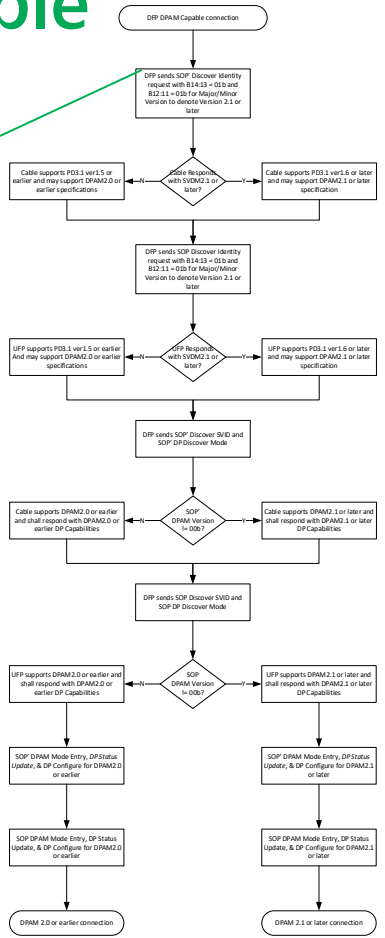
Bit(s)	Description	Values
4:0	**Command**	0h = RESERVED, shall not be used. 1h = *USB PD* ***Discover Identity***. 2h = *USB PD* ***Discover SVIDs***. 3h = *USB PD* ***Discover Modes***. 4h = ***Enter Mode***. 5h = ***Exit Mode***. 6h = *USB PD* ***Attention***. 7h – Fh = RESERVED, shall not be used. 10h = ***DisplayPort Status Update***. 11h = ***DisplayPort Configure***. 12h – 1Fh = RESERVED for DP_SID use.
		RESERVED (always 0).
		00b = REQ (Request from Initiator Port). 01b = ACK (*USB PD* Responder ACK response). 10b = NAK (*USB PD* Responder NAK response). 11b = BUSY (*USB PD* Responder BUSY response).
		For ***Enter Mode*** Command requests/responses, ***Exit Mode*** Command requests/responses, and *USB PD* ***Attention*** Command requests: • 000b = RESERVED. • 001b – 110b = Index into the list of Vendor Defined Objects (VDOs) to identify the needed Mode VDO. • 111b = Exit all Active Modes (equivalent of a power-on reset). Shall only be used with an ***Exit Mode*** Command request. For *USB PD* ***Discover Identity***, ***Discover SVIDs***, and ***Discover Modes*** Command requests/responses: • 000b. • 001b – 111b = RESERVED.
12:11	**Structured VDM Version (Minor)[a]**	Version number (Minor) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier 01b = Version 2.1 All other values are RESERVED.
14:13	**Structured VDM Version (Major)[a]**	Version number (Major) of the SVDM (not the *USB PD* version number). 00b = Version 2.0 or earlier. 01b = Version 2.x. (x indicates SVDM minor version) All other values are RESERVED.
15	**VDM Type**	1 = SVDM.
31:16	**Standard or Vendor ID (SVID)**	Base SID (for a *USB PD* ***Discover SVIDs*** Command request) or DP_SID, a 16-bit unsigned integer, assigned by the USB-IF.

- SVDM Minor: 2.0 = *DP Alt mode 2.0*
- SVDM Minor: 2.1 = *DP Alt mode 2.1*

SVDM Version Resolution Example

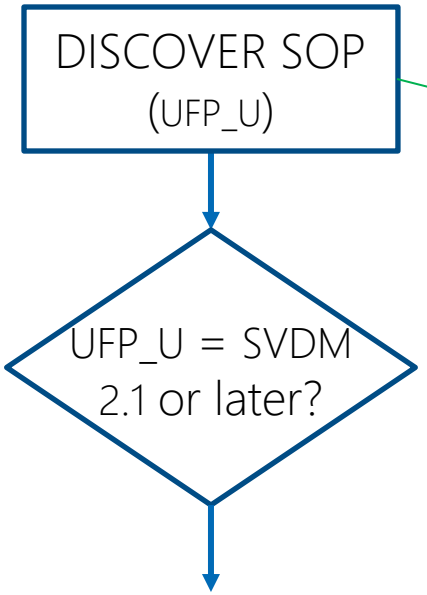
- SVDM Version resolution
  - DISCOVER IDENTITY (SOP'/ UFP)
  - DISCOVER SVIDs (SOP'/ UFP)
  - DISCOVER MODES (SOP'/ UFP)
    - DFP_U sends Discover Modes IF response "SVDM version = 2.1" then use "DPAM 2.1"
    - Else must use "DPAM 2.0"
  - ENTER MODE (SOP'/ UFP)
  - DP CONFIGURE (SOP'/ UFP)

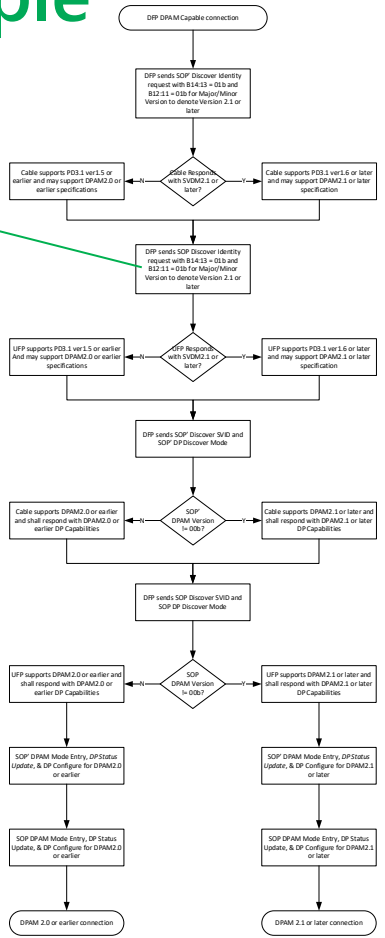




SVDM Version Resolution Example

- SVDM Version resolution
  - DISCOVER IDENTITY (SOP'/ UFP)
  - DISCOVER SVIDs (SOP'/ UFP)
  - DISCOVER MODES (SOP'/ UFP)
    - DFP_U sends Discover Modes
      IF response "SVDM version = 2.1"
      then use "DPAM 2.1"
    - Else must use "DPAM 2.0"
  - ENTER MODE (SOP'/ UFP)
  - DP CONFIGURE (SOP'/ UFP)





SVDM Version Resolution Example

- SVDM Version resolution
  - DISCOVER IDENTITY (SOP'/ UFP)
  - DISCOVER SVIDs (SOP'/ UFP)
  - DISCOVER MODES (SOP'/ UFP)
    - DFP_U sends Discover Modes IF response "SVDM version = 2.1" then use "DPAM 2.1"
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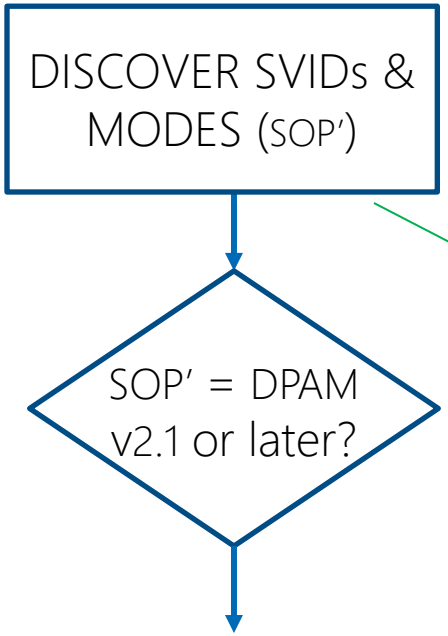
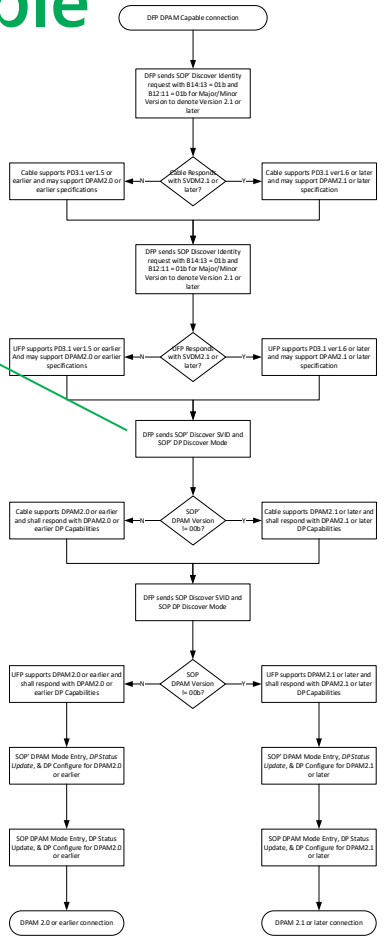
  - DP CONFIGURE (SOP'/ UFP)





SVDM Version Resolution Example

- SVDM Version resolution
  - DISCOVER IDENTITY (SOP'/ UFP)
  - DISCOVER SVIDs (SOP'/ UFP)
  - DISCOVER MODES (SOP'/ UFP)
    - DFP_U sends Discover Modes
      IF response "SVDM version = 2.1"
      then use "DPAM 2.1"
    - Else must use "DPAM 2.0"
  - ENTER MODE (SOP'/ UFP)
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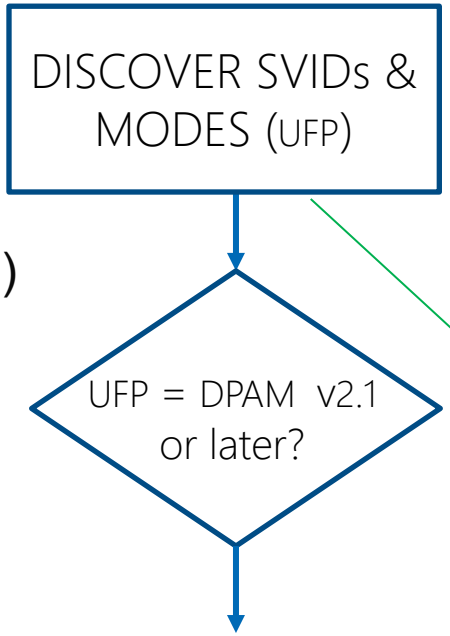

SVDM Version Resolution Example

- SVDM Version resolution
  - DISCOVER IDENTITY (SOP'/ UFP)
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    - DFP_U sends Discover Modes IF response "SVDM version = 2.1" then use "DPAM 2.1"
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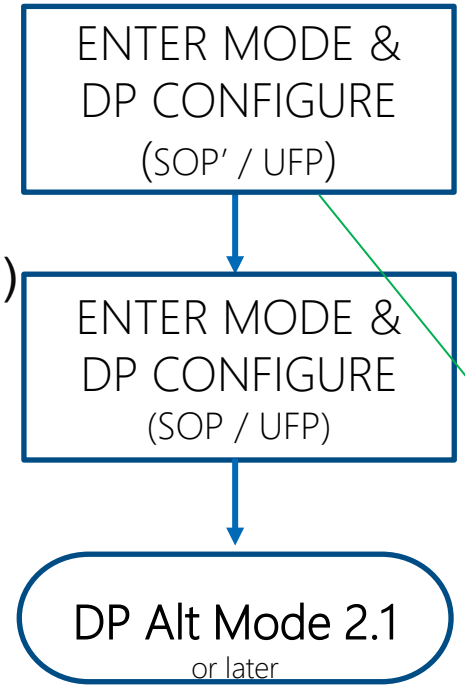
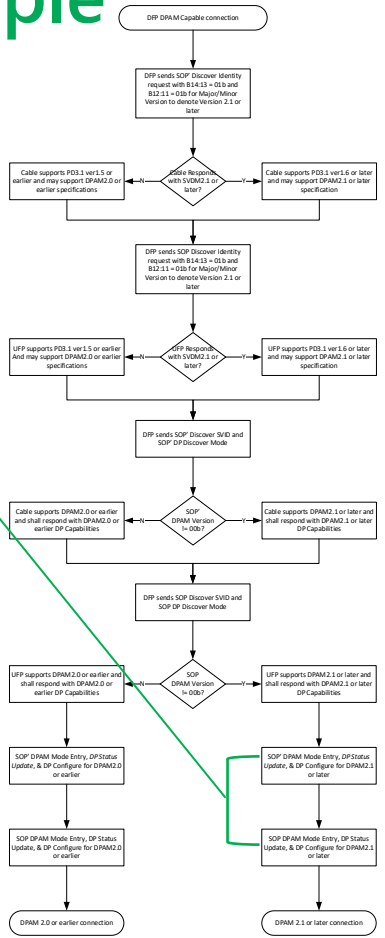
  - ENTER MODE (SOP'/ UFP)
  - DP CONFIGURE (SOP'/ UFP)





Key Field Changes: DISCOVER MODE Response

SOP

DPAM2.0

Table 5-5: DP Capabilities (VDO in the Responder *Discover Modes* VDM)

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED. 01b = DP Sink device-capable (including DP Branch device). 10b = DP Source device-capable (including DP Branch device). 11b = Both DP Source and Sink device-capable.
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP Standard* bit rates and electrical settings (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = DP interface is presented on a USB-C plug. 1 = DP interface is presented on a USB-C receptacle.
7	*USB 2.0* Signaling Not Used	0 = *USB 2.0* may be needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration. 1 = *USB 2.0* is not needed on A6 – A7 –or– B6 – B7 while in DisplayPort Configuration.
15:8	DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)	00000000b = DP Source device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[b] XXXX1XXXb = Pin Assignment D is supported.[c,d] XXX1XXXXb = Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	00000000b = DP Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c,g] XXX1XXXXb = Pin Assignment E is supported.[b] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
31:24	RESERVED	RESERVED (always 00h).

DPAM2.1

Table 5-5: DP Capabilities (VDO in the Responder USB PD *Discover Modes*

Bit(s)	Description	Values[a]
1:0	Port Capability	00b = RESERVED 01b = *DP* Sink device-capable (including *DP* [illegible]vice). 10b = *DP* Source device-capable (including [illegible] device). 11b = Both *DP* Source and Sink device-cap[illegible]
5:2	Signaling for Transport of DisplayPort Protocol	XXX1b = Supports *DP* bit rates and electri[illegible]gs (shall always be set apart from diagnostic purposes). XX1Xb = RESERVED. X1XXb = RESERVED. 1XXXb = RESERVED.
6	Receptacle Indication	0 = *DP* interface is presented on [illegible] plug. 1 = *DP* interface is presented [illegible]-C receptacle.
7	USB 2.0 Signaling Not Used	0 = *USB 2.0* may be needed [illegible] A7 –or– B6 – B7 while in DisplayPort Configura[illegible] 1 = *USB 2.0* is not needed [illegible] – A7 –or– B6 – B7 while in DisplayPort Configu[illegible]
15:8	DP Source Device Pin Assignments Supported (reported by a DP Source device receptacle or DP Sink device (direct-attach) plug)	00000000b = *DP* Sou[illegible]ce pin assignments are not supported. XXXXXXX1b = R[illegible]VED. XXXXXX1Xb = R[illegible]VED. XXXXX1XXb = [illegible]Assignment C is supported.[b] XXXX1XXXb = [illegible]in Assignment D is supported.[c,d] XXX1XXXXb = [illegible] Pin Assignment E is supported.[e] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
23:16	DP Sink Device Pin Assignments Supported (reported by a DP Sink device receptacle or DP Source device (direct-attach) plug)	00000000b = *DP* Sink device pin assignments are not supported. XXXXXXX1b = RESERVED. XXXXXX1Xb = RESERVED. XXXXX1XXb = Pin Assignment C is supported.[f] XXXX1XXXb = Pin Assignment D is supported.[c,g] XXX1XXXXb = Pin Assignment E is supported.[b] XX1XXXXXb = RESERVED. X1XXXXXXb = RESERVED. 1XXXXXXXb = RESERVED.
29:24	RESERVED	RESERVED (always 00b).
31:30	DPAM Version[f]	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Discover Modes Response from UFP

29:28[d]	Active Component	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
	Signaling for Transport of DisplayPort Protocol[b]	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20).
	UHBR13.5	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[e]

SOP'

DPAM2.0

SOP' Cable DP Capabilities (DPAM2.0)		
Bits	Field	CTS Value
B31-24	Reserved	0000 0000b
B23-16	DP Sink Device Pin Assignment Supported	0000 1100b
B15-8	DP Source Device Pin Assignment Supported	0000 1100b
B7-6	Reserved	00b
B5-2	Signal for Transport of DP Protocol	0001b
B1-0	Reserved	00b

DPAM2.1

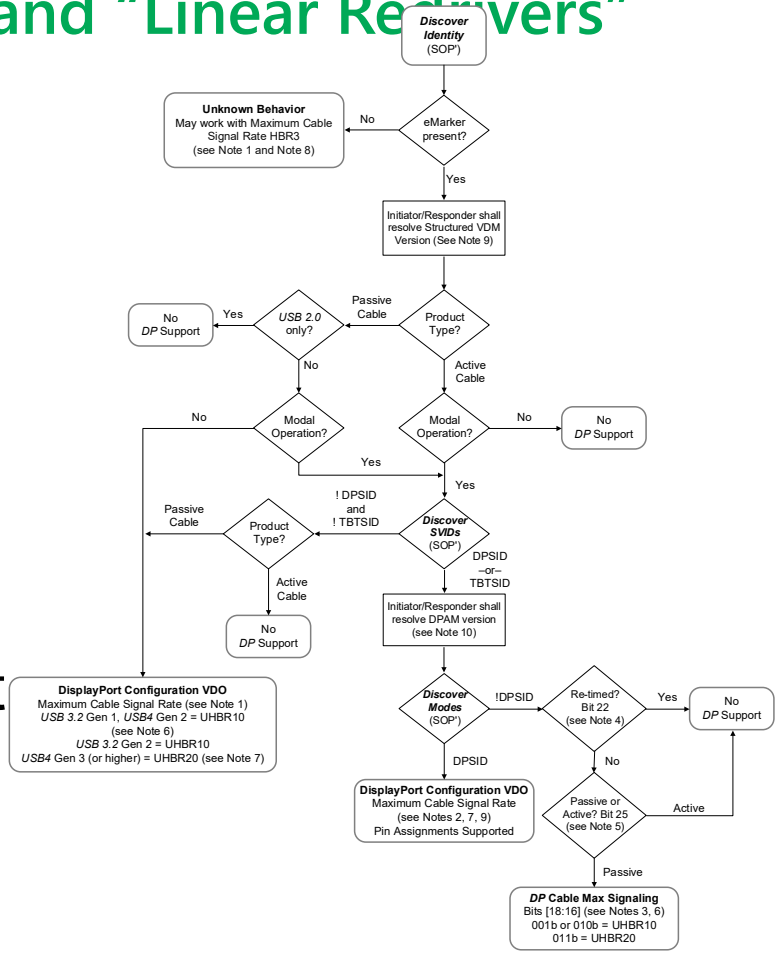
	RESERVED	RESERVED (always 00b).
	Signaling for Transport of DisplayPort Protocol[b]	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[c]
7:6	RESERVED	RESERVED (always 00b).
15:8	DP Source Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported. 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
23:16	DP Sink Device Pin Assignments Supported	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
24	RESERVED	RESERVED (always 00b).
25	UHBR13.5	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[e]
27	RESERVED	RESERVED (always 0).
29:28[d]	Active Component	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30	DPAM Version	00b = Original version. 01b = Version 1.

Discover Modes Response from Cable

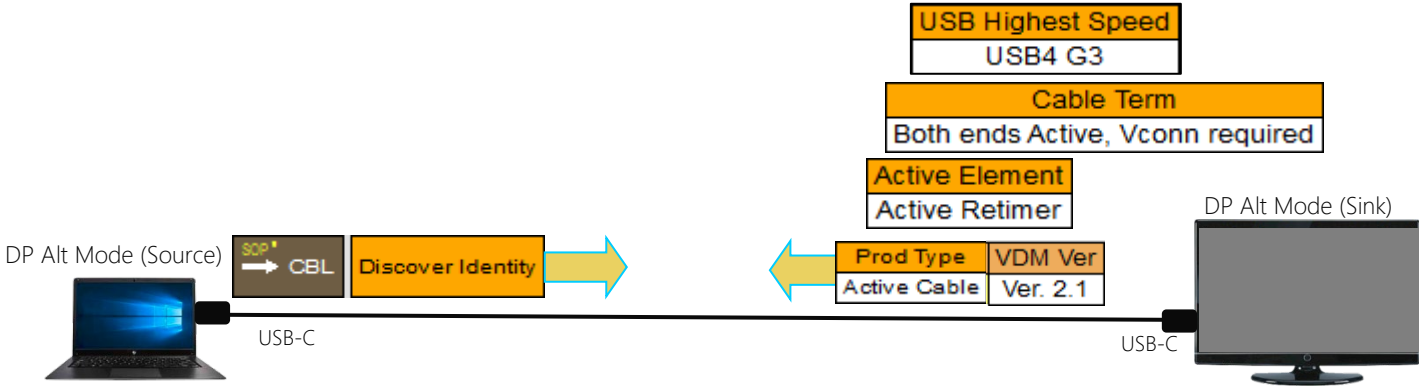
DP Alt Mode 2.1
Configuration with Active Cable

Active Cables: “Retimers” and “Linear Redrivers”

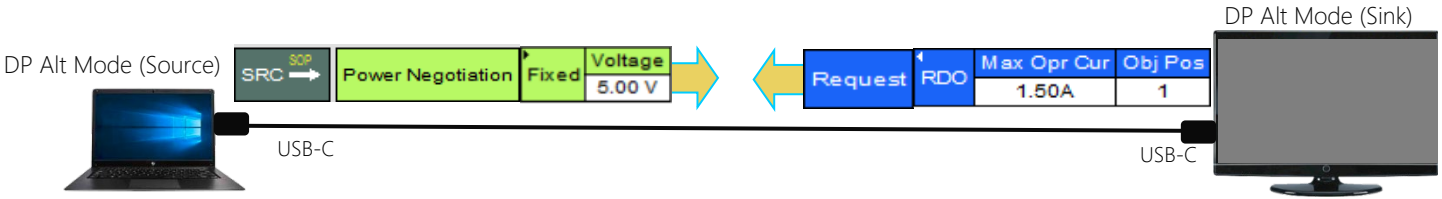
- DFP_U Must send ENTER MODE to the Cable
- C-to-DP Adapters: should support “reversible” operation
  - if not, visually indicate which direction they support
- Active Type-C Cables must support one bidirectional USB 3.2 link



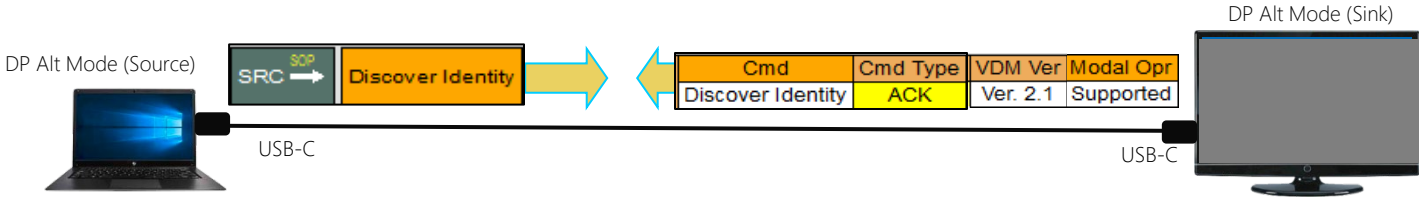
DFP Sends Discover Identity to the Cable (SOP')



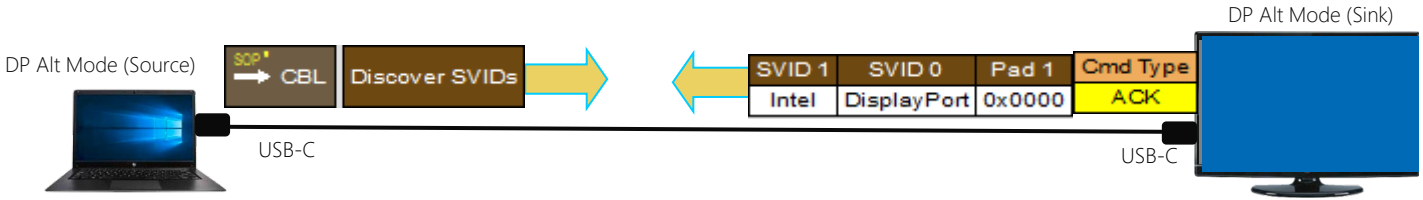
DFP Negotiates Initial Power Delivery Contract



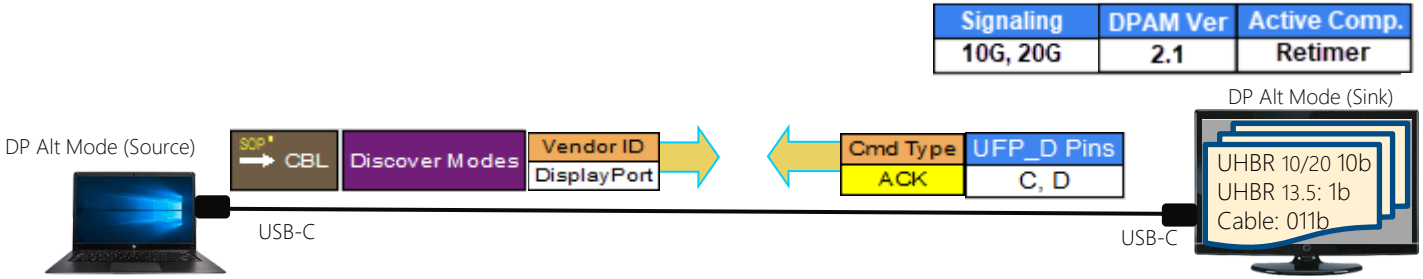
DFP Sends Discover Identity to the Sink (SOP)



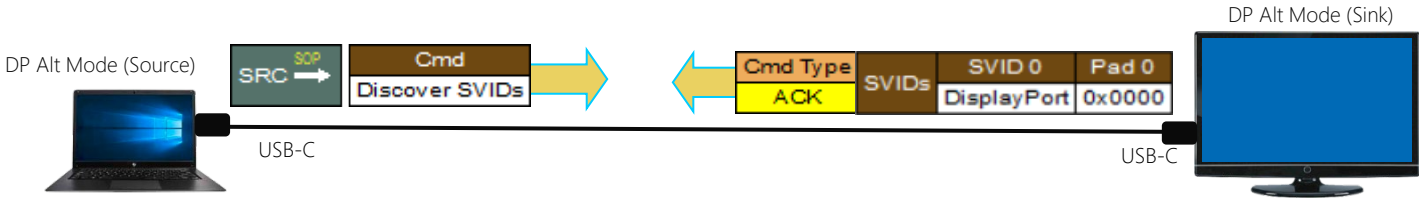
DFP Sends Discover SVIDs to the Cable (SOP')



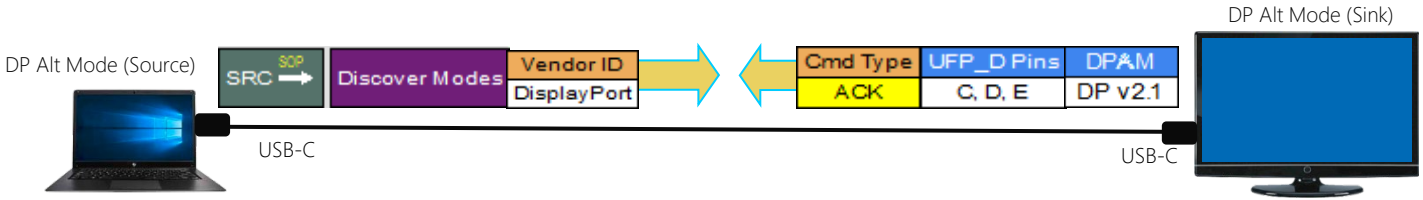
DFP Sends Discover Modes to the Cable (SOP')



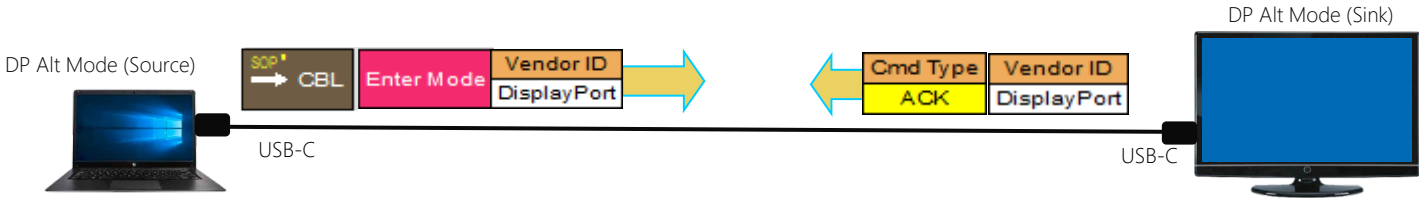
DFP Sends Discover SVIDs to the Sink (SOP)



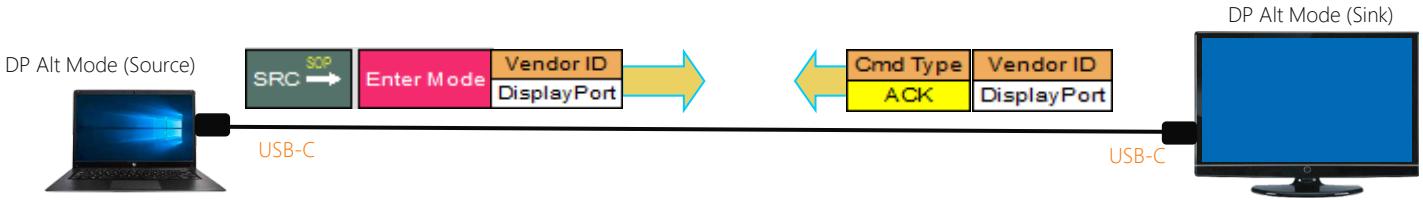
DFP Sends Discover Modes to the Sink (SOP)



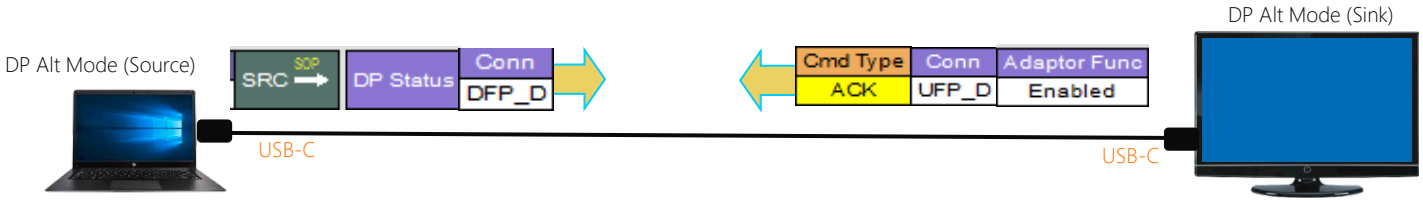
DFP Sends Enter Mode to the Cable (SOP')



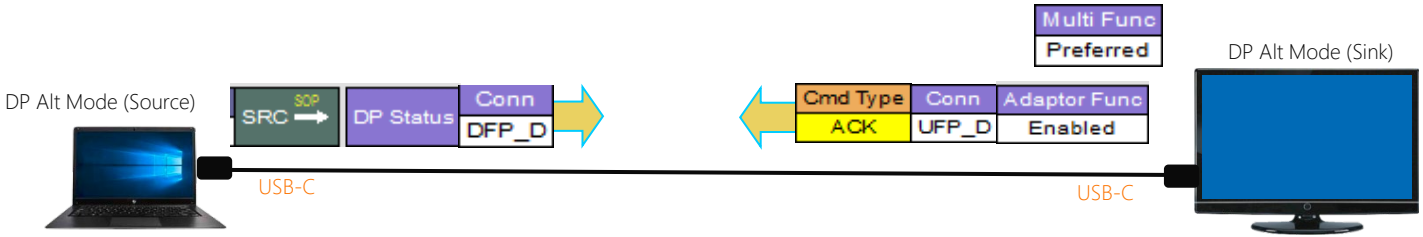
DFP Sends Enter Mode to the Sink (SOP)



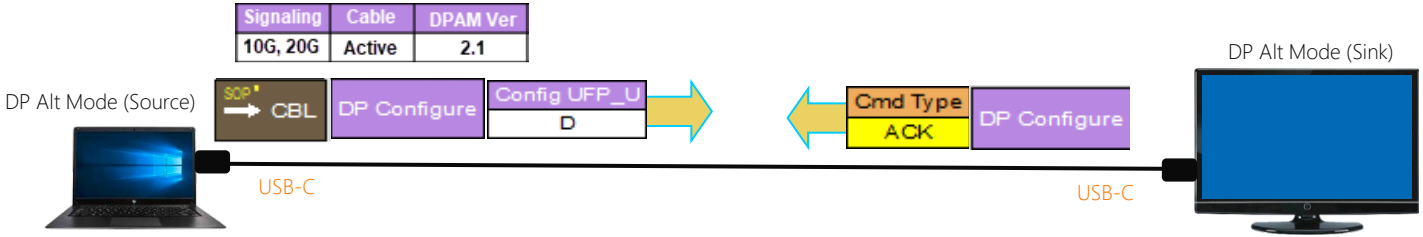
DFP Sends DP Status to the Sink (SOP)



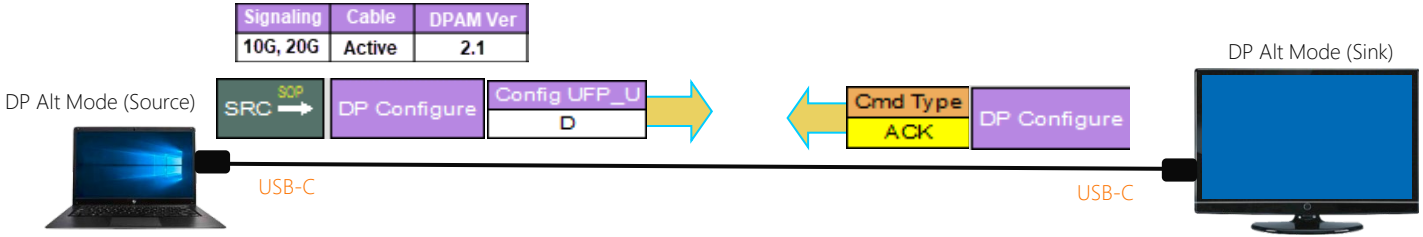
DFP Sends DP Status to the Sink (SOP)



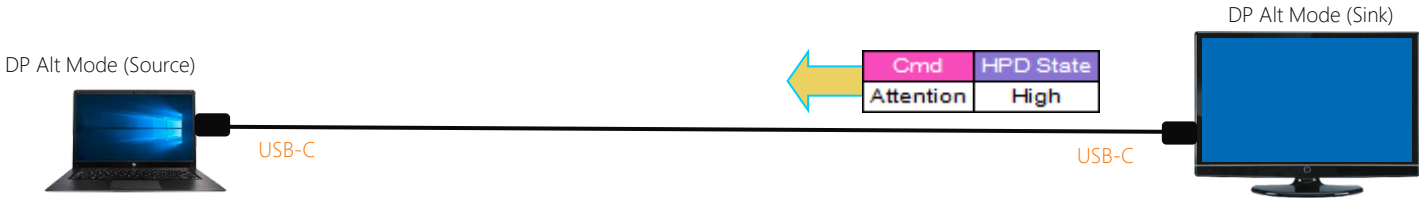
DFP Sends DP Configure to the Cable (SOP')



DFP Sends DP Configure to the Sink (SOP)

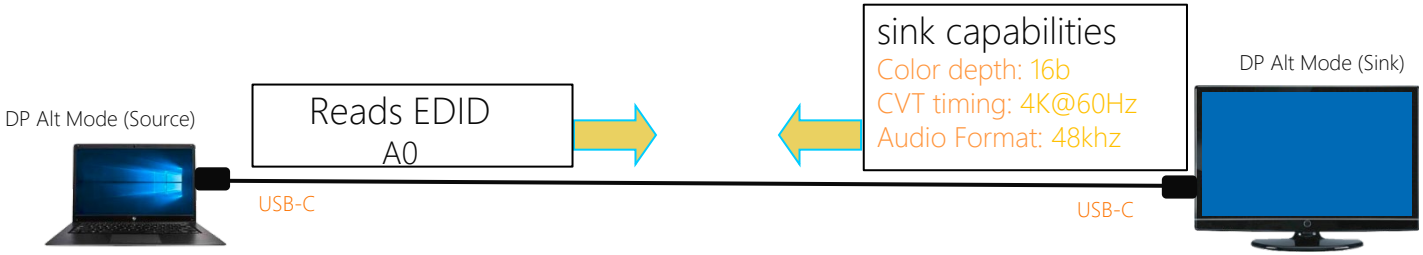


UFP Sends Attention Message to the DFP

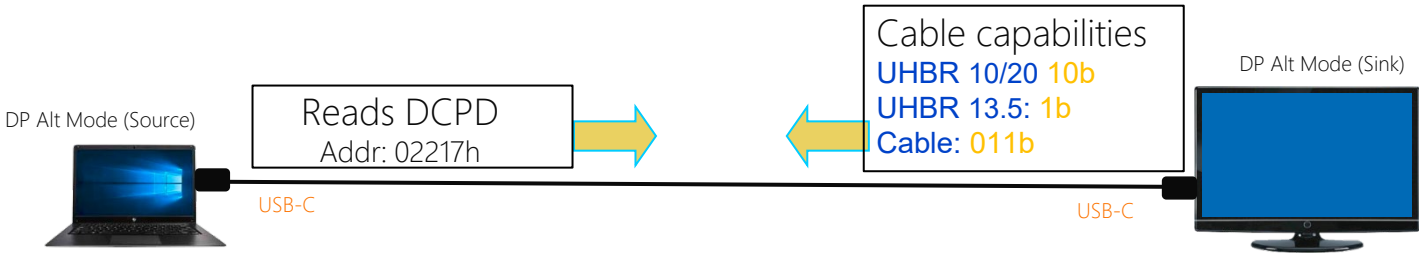


Link Training (Aux): Read DisplayID or legacy EDID

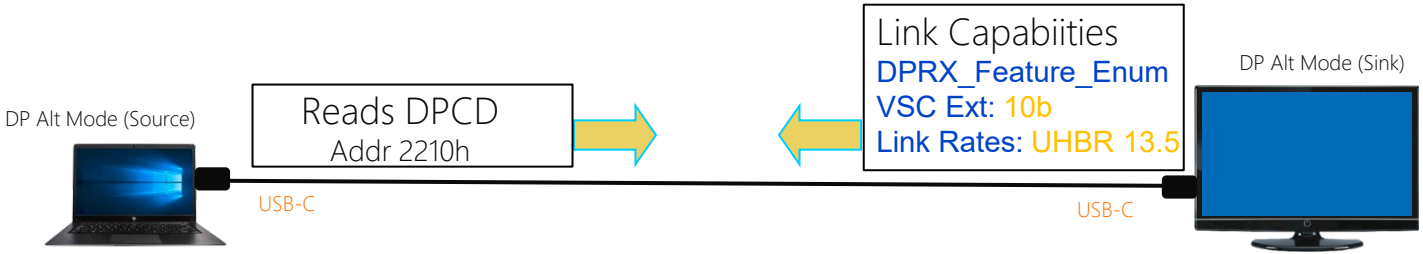
Now this is all over Aux not PD



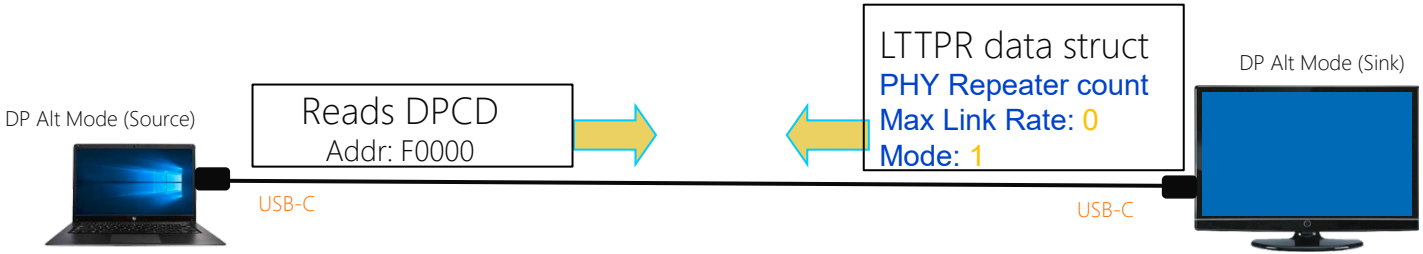
Link Training: Read Cable Capabilities



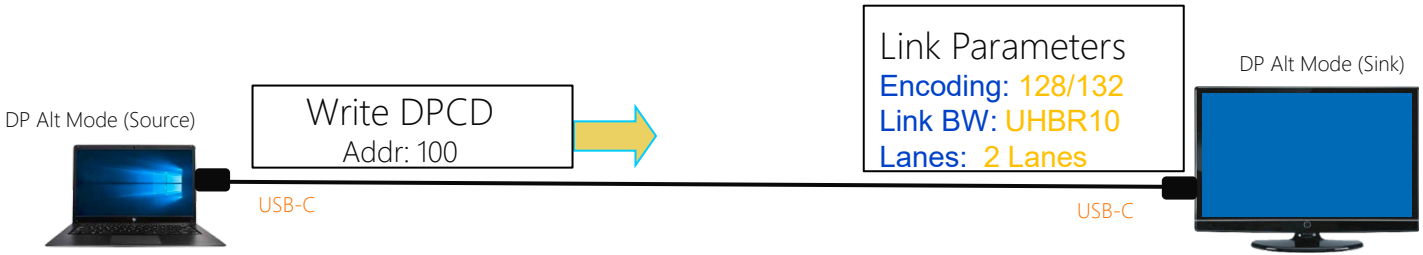
Link Training: Read Link Capabilities



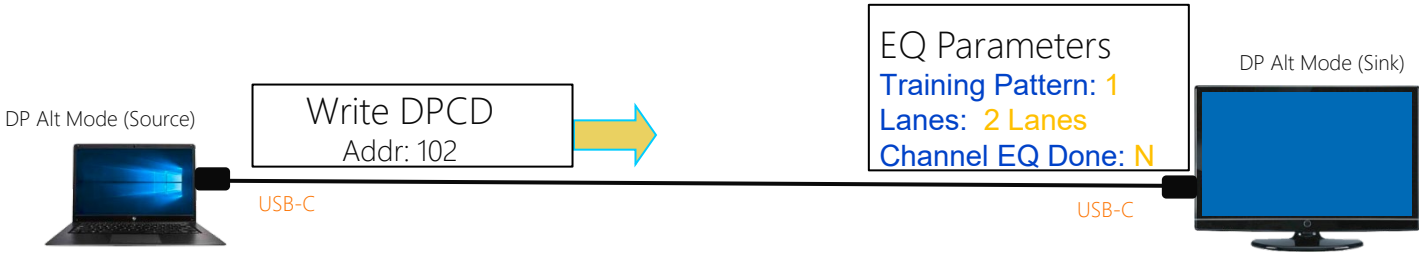
Link Training: Read LTTPR Data



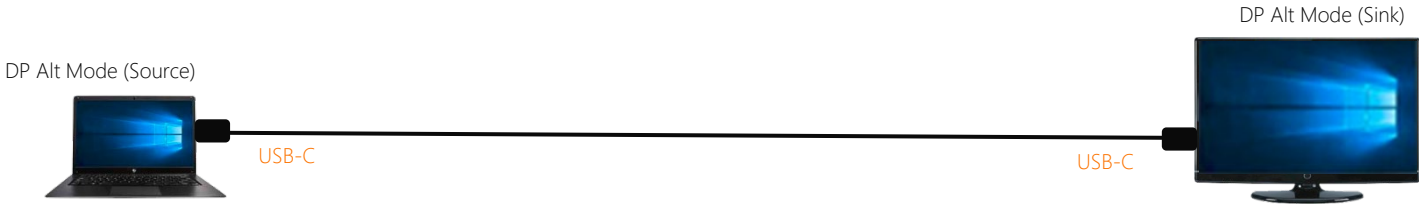
Link Training: Lanes & Link Bandwidth Set



Link Training: Equalization & Clock Domain Switch

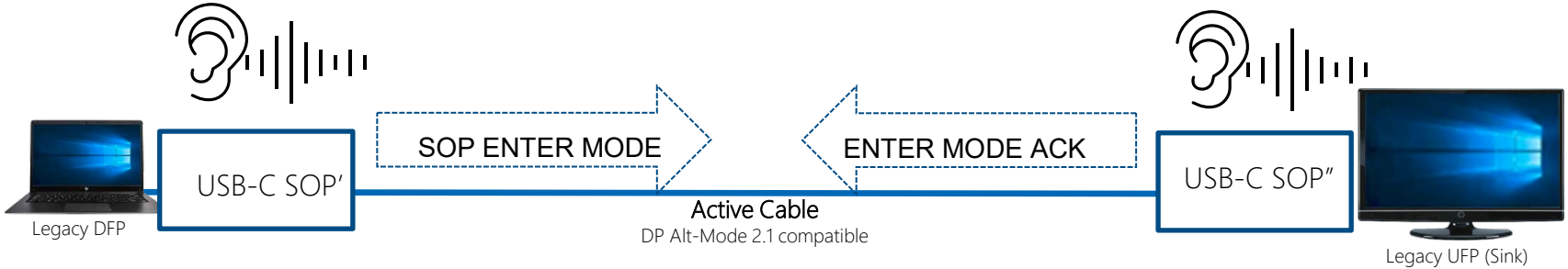


Link Training: Equalization & Clock Domain Switch

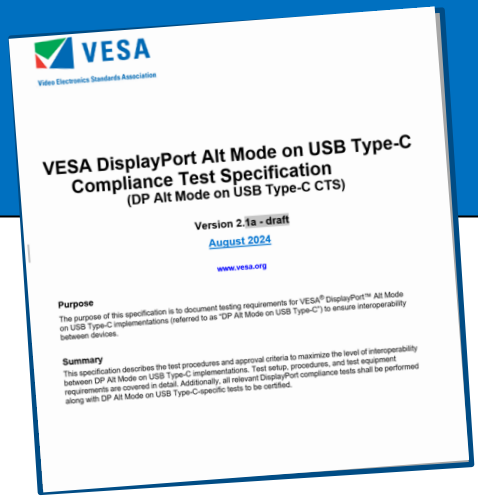


DP 2.1 Active Cable “Snoop” mode

- **Special Situation**: Legacy DP_Sources that do not send ENTER MODE to the cable:
  - **DP Alt Mode 2.1** Active cables are required to snoop SOP commands and silently perform the same on SOP’ & SOP” for:
    - ENTER MODE
    - CONFIGURE
    - EXIT MODE



DP Alt-Mode v2.1a
Compliance Test Specification


VESA
Video Electronics Standards Association

VESA DisplayPort Alt Mode on USB Type-C
Compliance Test Specification
(DP Alt Mode on USB Type-C CTS)

Version 2.1a - draft
August 2024

www.vesa.org

Purpose

The purpose of this specification is to document testing requirements for VESA® DisplayPort™ Alt Mode on USB Type-C implementations (referred to as "DP Alt Mode on USB Type-C") to ensure interoperability between devices.

Summary

This specification describes the test procedures and approval criteria to maximize the level of interoperability between DP Alt Mode on USB Type-C implementations. Test setup, procedures, and test equipment requirements are covered in detail. Additionally, all relevant DisplayPort compliance tests shall be performed along with DP Alt Mode on USB Type-C-specific tests to be certified.

TELEDYNE LECROY
Everywhereyoulook™

DP Alt Mode v2.1 Compliance Test Specification

- Contents
  - Ch:3 Physical Layer
  - Ch:4 Cables
  - Ch:5 Type-C-to-DP Plug Connector
  - Ch:6 DP Alt Mode Protocol Converter
  - Ch:7 DP Alt Mode Type-C Source
  - Ch:8 DP Alt Mode Type-C Sink
  - Ch:9 AUX and HPD
  - Ch:10 Discovery and USB PD
  - Ch:11 VBUS and VCONN

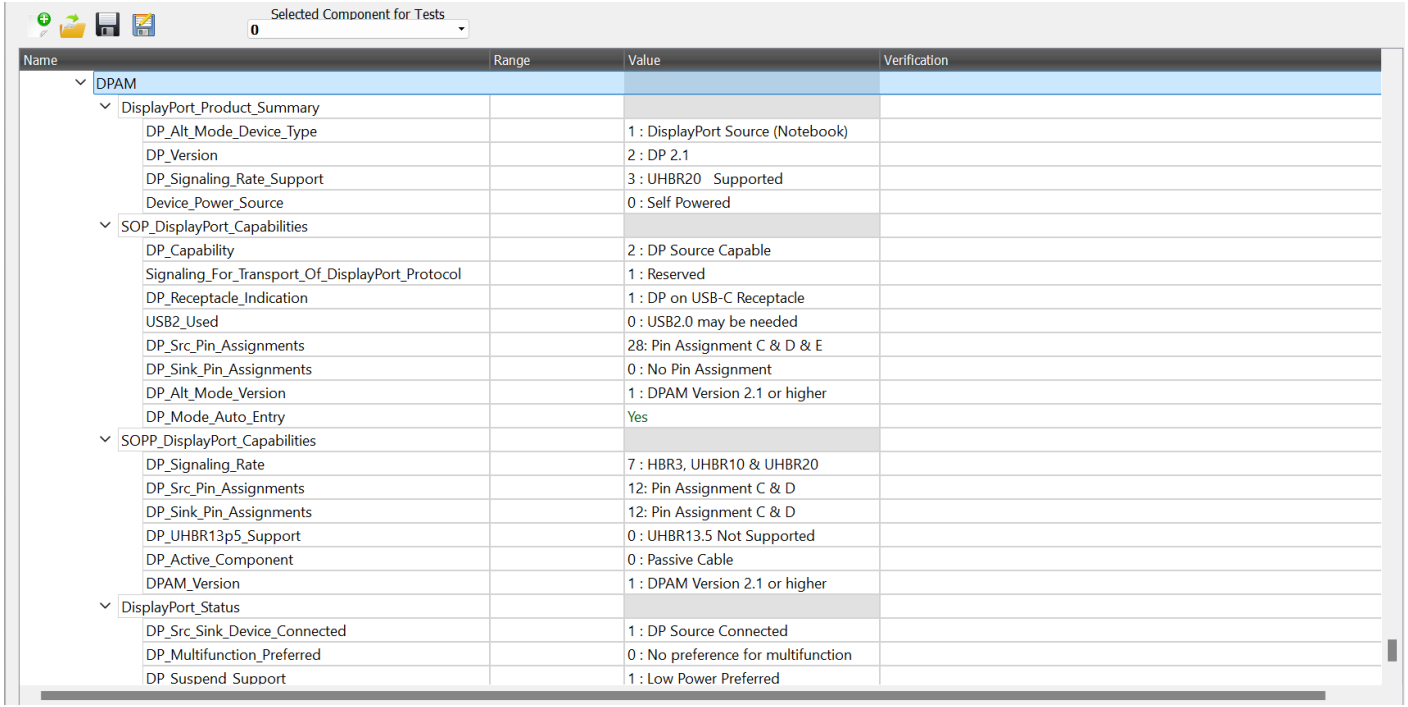
LabMaster 10Zi A

Quantumdata M42de
DP 2.1 Compliance Tester

Voyager M310e USB-C
Compliance Tester

DP Alt Mode VIF

- Utilizes USB.org VIF: Optional Content fields
- Allows efficient testing of DPAM devices
- Download latest revision: www.VESA.org
-



Name	Range	Value	Verification
DPAM			
DisplayPort_Product_Summary			
DP_Alt_Mode_Device_Type		1 : DisplayPort Source (Notebook)	
DP_Version		2 : DP 2.1	
DP_Signaling_Rate_Support		3 : UHBR20 Supported	
Device_Power_Source		0 : Self Powered	
SOP_DisplayPort_Capabilities			
DP_Capability		2 : DP Source Capable	
Signaling_For_Transport_Of_DisplayPort_Protocol		1 : Reserved	
DP_Receptacle_Indication		1 : DP on USB-C Receptacle	
USB2_Used		0 : USB2.0 may be needed	
DP_Src_Pin_Assignments		28: Pin Assignment C & D & E	
DP_Sink_Pin_Assignments		0 : No Pin Assignment	
DP_Alt_Mode_Version		1 : DPAM Version 2.1 or higher	
DP_Mode_Auto_Entry		Yes	
SOPP_DisplayPort_Capabilities			
DP_Signaling_Rate		7 : HBR3, UHBR10 & UHBR20	
DP_Src_Pin_Assignments		12: Pin Assignment C & D	
DP_Sink_Pin_Assignments		12: Pin Assignment C & D	
DP_UHBR13p5_Support		0 : UHBR13.5 Not Supported	
DP_Active_Component		0 : Passive Cable	
DPAM_Version		1 : DPAM Version 2.1 or higher	
DisplayPort_Status			
DP_Src_Sink_Device_Connected		1 : DP Source Connected	
DP_Multifunction_Preferred		0 : No preference for multifunction	
DP_Suspend_Support		1 : Low Power Preferred	

DP Alt-Mode 2.1 Cable Discovery Tests (for DFPs)

Verify UUT identifies cable speed, type, DPAM ver w/ SOP **DP CONFIGURE** message

Test	Description
10.3.3	Alt Mode Entry with USB Type-C to USB Type-C Passive non-emarked
10.3.4	Alt Mode Entry with USB Type-C to USB Type-C Passive TBT3 cable
10.3.5	Alt Mode Entry with Type-C to Type-C Passive USB4 Gen3 cable
10.3.6	Alt Mode Entry with Type-C to Type-C Active LRD DP2.0 cable
10.3.7	Alt Mode Entry with Type-C to Type-C Active Retimer DP2.0 cable
10.3.8	Alt Mode Entry with Type-C to Type-C Active Redriver DP2.1 cable
10.3.9	Alt Mode Entry with Type-C to Type-C Active Non - DP2.1/0 cable
10.3.10	Alt Mode Entry with Type-C to Type-C USB2.0 Only cable
10.3.11	Alt Mode Entry with Type-C to DP2.1 cable

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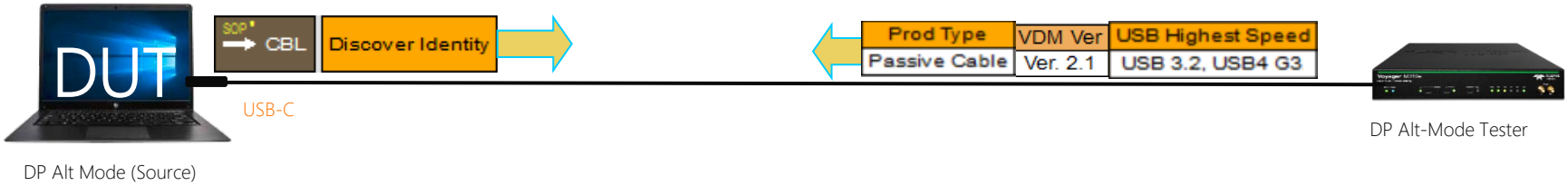
10.3.6	Alt Mode Entry with Type-C to Type-C Active LRD DP2.0 cable
10.3.7	Alt Mode Entry with Type-C to Type-C Active Retimer DP2.0 cable
10.3.8	Alt Mode Entry with Type-C to Type-C Active Redriver DP2.1 cable
10.3.9	Alt Mode Entry with Type-C to Type-C Active Non - DP2.1/0 cable
10.3.10	Alt Mode Entry with Type-C to Type-C USB2.0 Only cable
10.3.11	Alt Mode Entry with Type-C to DP2.1 cable



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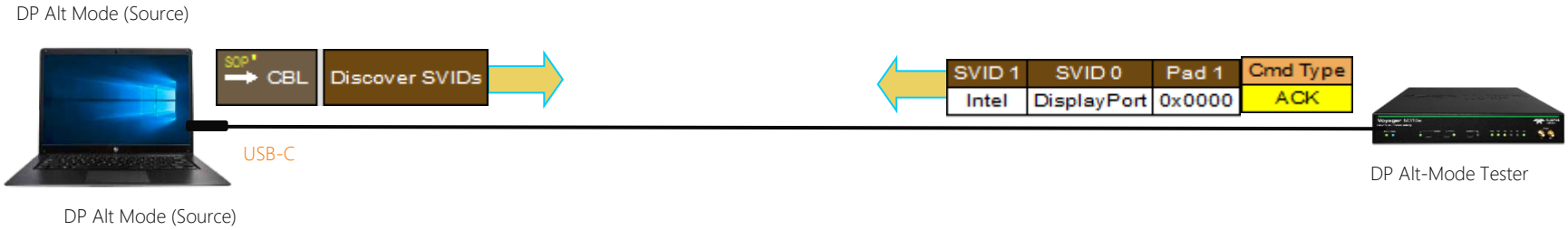

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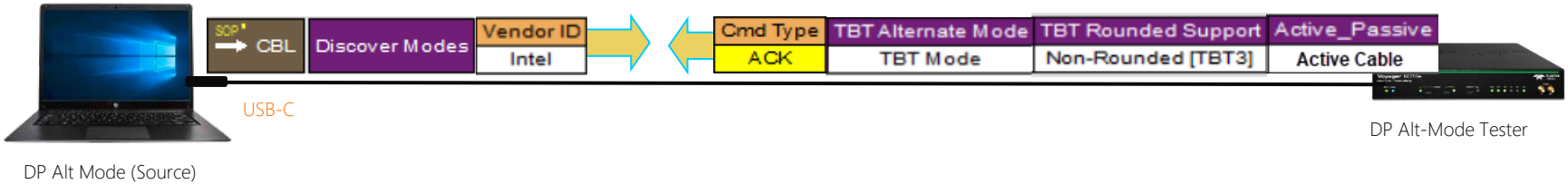

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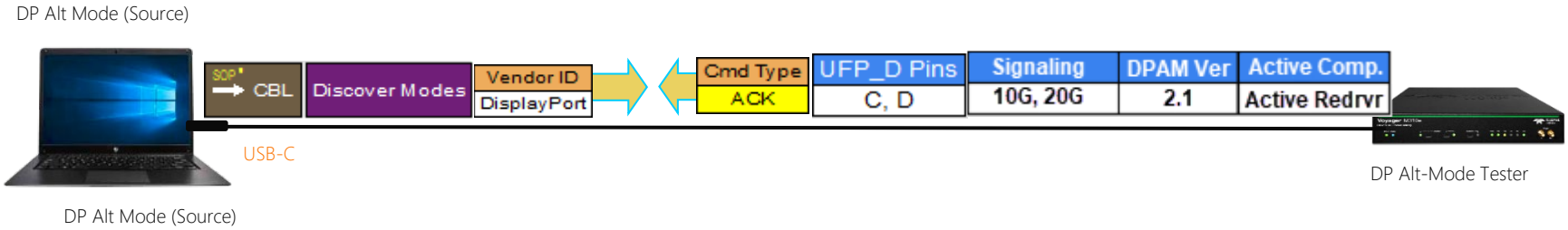
10.3.5	Alt Mode Entry with Type-C to Type-C Passive USB4 Gen3 cable
10.3.6	Alt Mode Entry with Type-C to Type-C Active LRD DP2.0 cable
10.3.7	Alt Mode Entry with Type-C to Type-C Active Retimer DP2.0 cable
10.3.8	Alt Mode Entry with Type-C to Type-C Active Redriver DP2.1 cable
10.3.9	Alt Mode Entry with Type-C to Type-C Active Non - DP2.1/0 cable
10.3.10	Alt Mode Entry with Type-C to Type-C USB 2.0 Only cable
10.3.11	Alt Mode Entry with Type-C to DP2.1 cable



DP Alt-Mode 2.1 Cable Discovery Tests (for DFPs)

Verify UUT identifies cable speed, type, DPAM ver w/ SOP **DP CONFIGURE** message

Test	Description
10.3.3	Alt Mode Entry with USB Type-C to USB Type-C Passive non-emarked
10.3.4	Alt Mode Entry with USB Type-C to USB Type-C Passive TBT3 cable
10.3.5	Alt Mode Entry with Type-C to Type-C Passive USB4 Gen3 cable
10.3.6	Alt Mode Entry with Type-C to Type-C Active LRD DP2.0 cable
10.3.7	Alt Mode Entry with Type-C to Type-C Active Retimer DP2.0 cable
10.3.8	Alt Mode Entry with Type-C to Type-C Active Redriver DP2.1 cable
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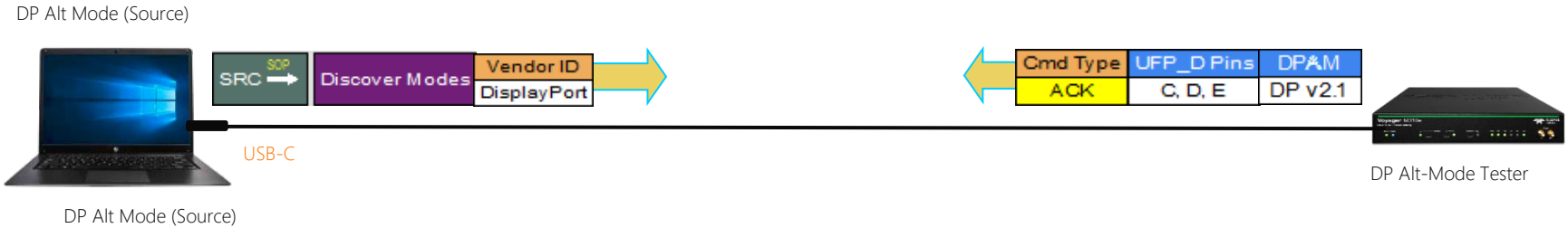

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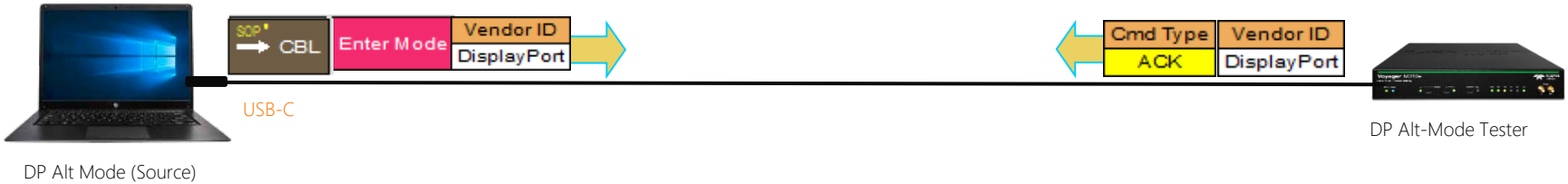

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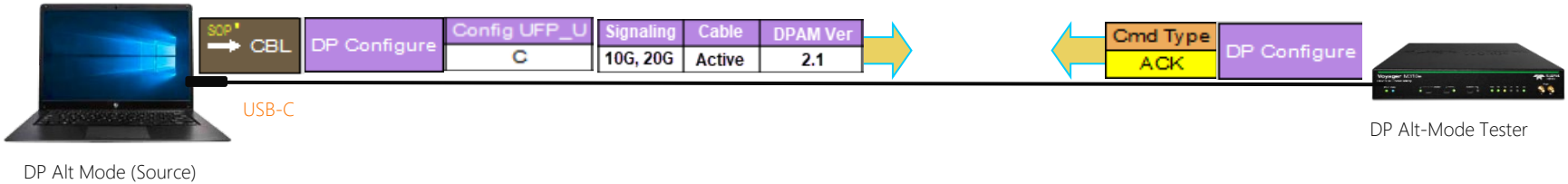


VESA

Thank You

DP2.1 Panel Replay and Advanced Link Power Management: Implementation and Testing Challenges

Marco Denicolai
Unigraf Oy
October 2025

Agenda

- Saving power with Panel Replay (PR)
- Saving power with Advanced Link Power Management (ALPM)
- Interaction with FEC, MST and HDCP

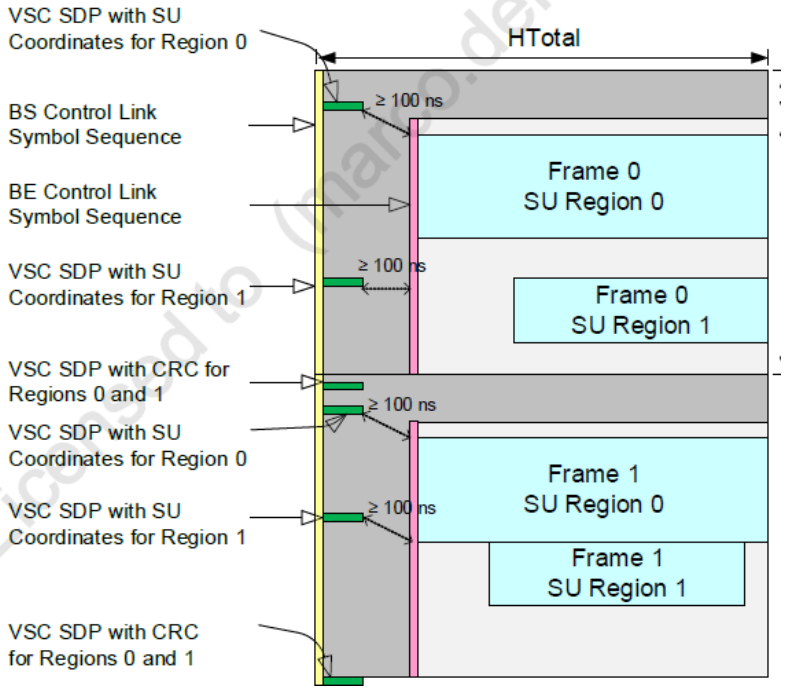
The Devil is in the details…

DisplayPort system-level power conservation

- Optional Panel Replay (PR) can be enabled to turn the Main Link off when no data is being transferred and save power.
- When PR is in Active state, the Sink will use the image captured in its Remote Frame Buffer (RFB) to refresh the display.
- During PR Active state, the Source can either continue to transmit a frame-rate-governed video timing (discarded by the Sink) or, optionally, turn the Main Link off.
- Optional Main Link power on/off management uses Advanced Link Power Management (ALPM) in AUX-less mode.

Panel Replay overview

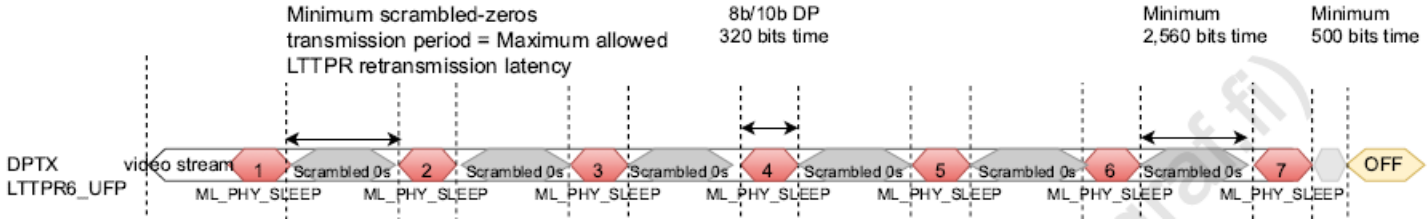
- Transitions between Live Frame mode and PR Active state happen using VSC SDPs.
- The Source can transmit a Full Frame update, or one or more smaller Selective Update (SU) Regions, each starting at their respective video scan line position.
- SU Region coordinates and dimensions are defined using a VSC SDP transmitted at least 100ns before the start of the SU region.
- After a SU Region, the Source may optionally transmit a VSC SDP containing the CRC accumulated for all of the SU Regions of the frame.
- Optional SU Region Early Transport support: the first SU Region is transmitted starting from the first active video scan line instead of its real position. The following regions are transmitted preserving the relative distance between them.



ALPM: Main Link Power-off

- The Source uses the ML_PHY_SLEEP sequence followed by scrambled zeroes to signal LTTPRs and Sink that the Main Link will be powered-off.
- The ML_PHY_SLEEP sequence consists of:
  - 8b/10b: a sequence of [K28.5, K27.7, K28.5, K27.7, K28.5, K28.5, K28.5, K28.5], with correct disparity
  - 128b-132b: a special 129-bit supersymbol [CDI=1 + 89898989h, 89898989h, 89898989h, 89898989h]. CDI is XORed according to standard rules, then precoded
- The Source transmits four consecutive ML_PHY_SLEEP sequences followed by scrambled 0s:
  - Once for each connected LTTPR
  - Once for the Sink

- The ML_PHY_SLEEP sequence must not overwrite BS+VBID, MSA, SDP data or FEC control link symbols.
- The Sink must look for two consecutive ML_PHY_SLEEP sequences and allow for max 4 symbol errors within them.
- Mandatory minimum ALW_SLEEP time after power-off sequence: 15us

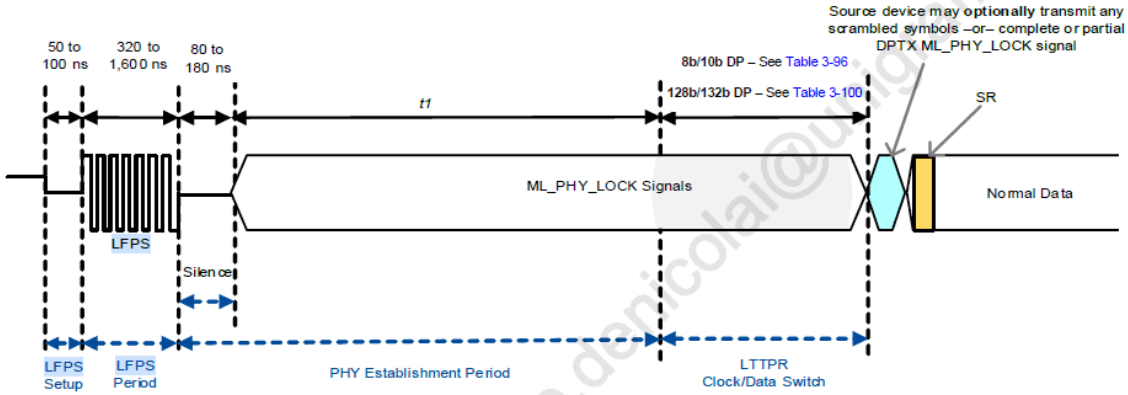


ALPM: Main Link Power-off (cont.)

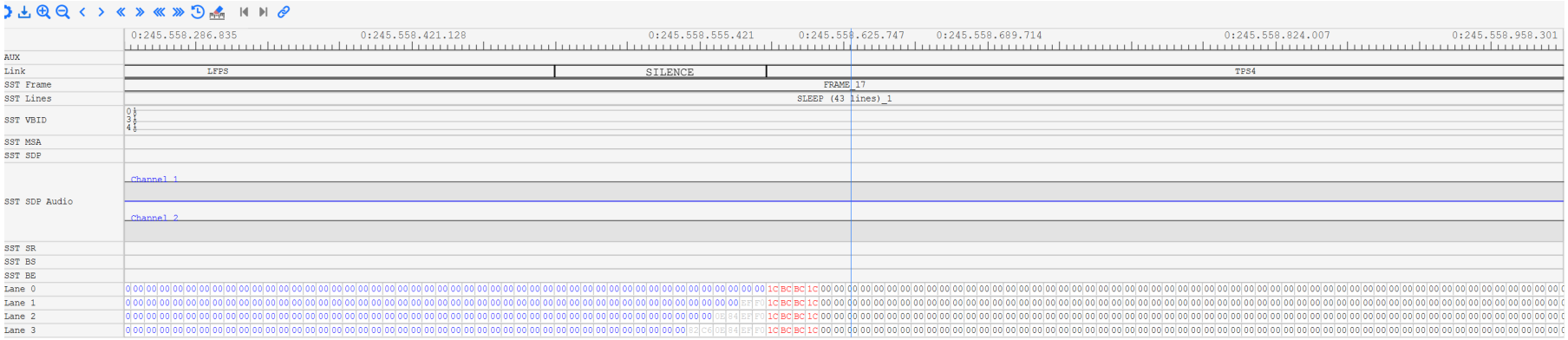
ALPM: Main Link Power-on (aka “wake”)

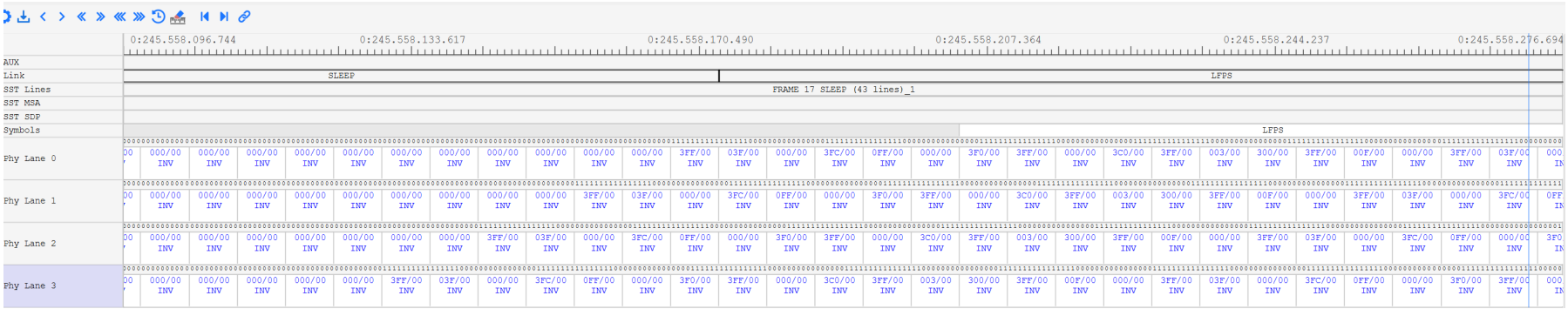
- The Source uses the ML_PHY_WAKE sequence to signal LTTPRs and Sink that the Main Link has been powered back on.
- The ML_PHY_WAKE sequence is composed by LFPS period (square wave at 12.5…50 MHz, at least 16 pulses, no more than 1.6us long) followed by a silence period and ML_PHY_LOCK pattern.
- ML_PHY_LOCK pattern:
  - 8b/10b – same as TPS4
  - 128b/132b – same as 128b_132b_TPS2 but with reduced intervals between LT_SCRAMBLER_RESET symbols (4 logical frames instead of 16)

- LFPS can have different common mode voltage amplitude than the ML data. Switch to ML common mode voltage is performed during the silence period
- The shortest duration of ML_PHY_LOCK is 50us. The Sink must complete EQ adaptation within this time. This is significantly shorter than usual link training



ALPM: Main Link Power-on (cont.)

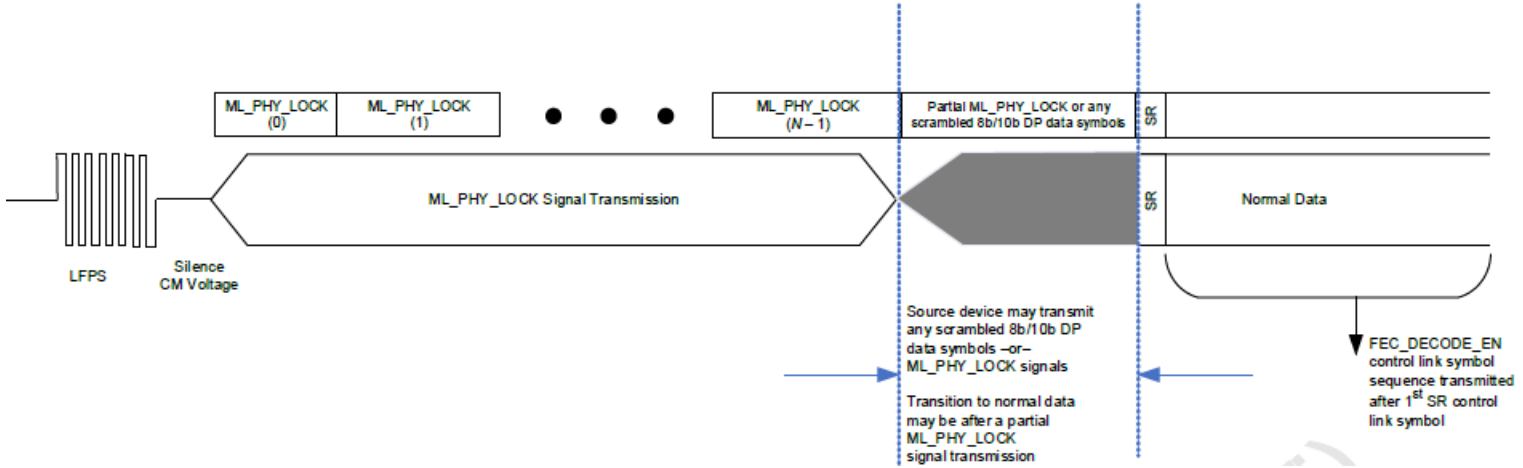




8b/10b FEC support

- In 8b/10b mode, FEC is not mandatory for ALPM. However, it is mandatory for Panel Replay.
- FEC block structure is maintained during the power-off sequence
- On the Sink side, FEC is considered disabled after power-off. Source must re-enable it by transmitting the FEC_DECODE_EN sequence after ML_PHY_LOCK pattern.

- The FEC block containing the final part of power-off sequence's scrambled 0s may be left incomplete. Sink must handle this situation correctly.
- The Sink cannot disable its FEC Decoder right when ML_PHY_SLEEP is detected but needs to wait for the last FEC block data to be decoded, since it could contain e.g. the tale of the last video frame transmitted.

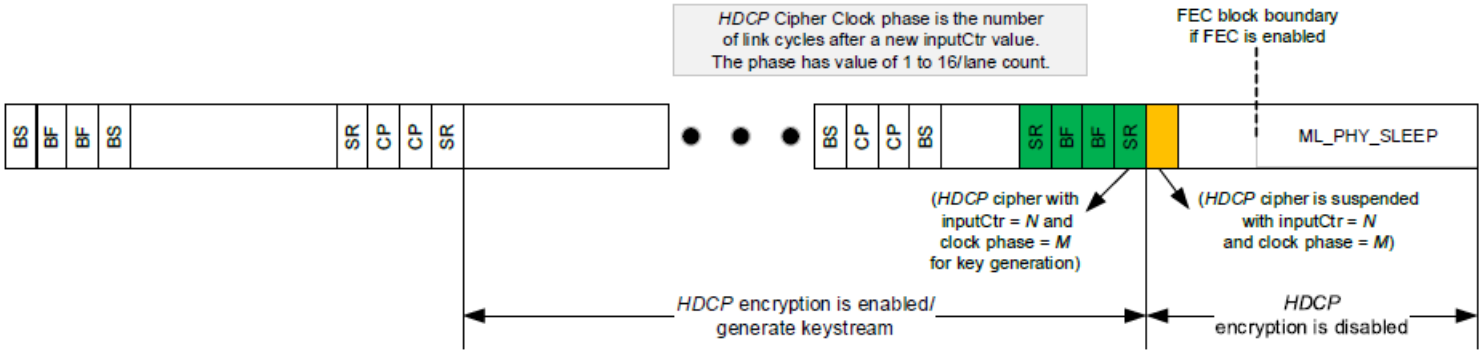


MST support

- During power-off sequence, ML_PHY_SLEEP is transmitted using all time slots.
- Source must be careful not to overwrite important data such as BS and VBID with ML_PHY_SLEEP in allocated slots.
- After power-on sequence, MST framing is started after the ML_PHY_LOCK pattern with an MST SR symbol.

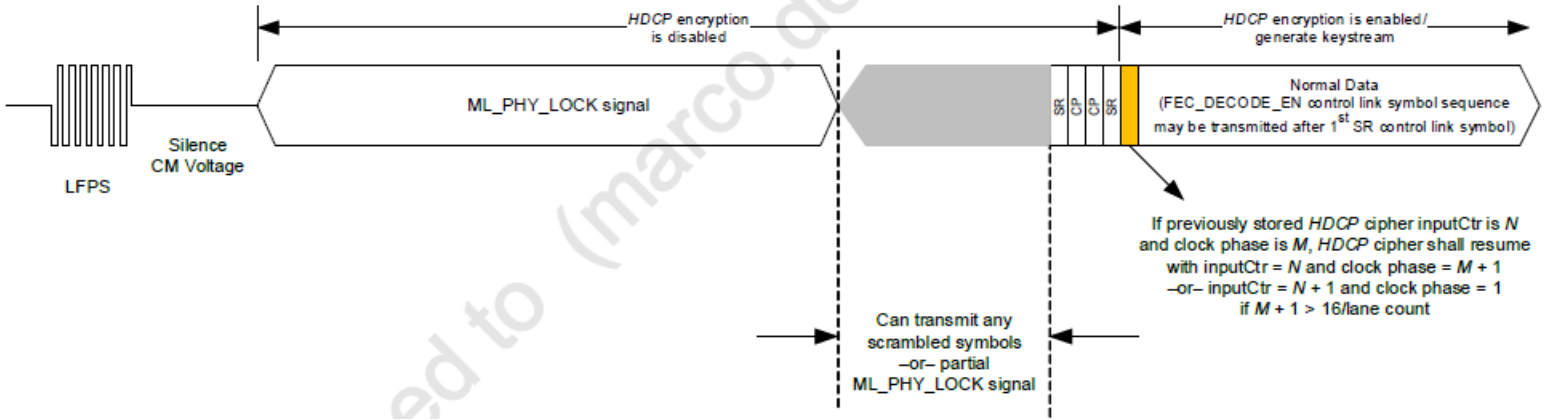
HDCP support

- Only HDCP r2.3 (or higher) is supported with AUX-less ALPM.
- HDCP is suspended before ML_PHY_SLEEP, HDCP cypher is frozen.



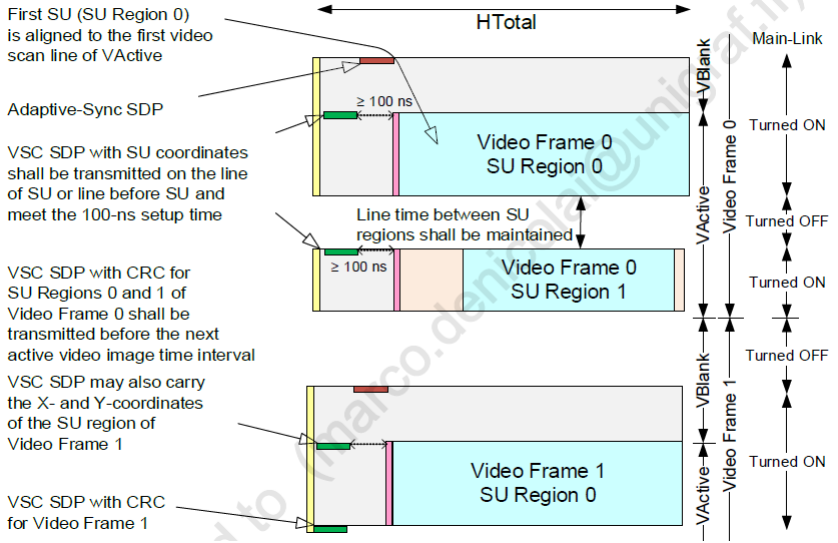
HDCP support (cont.)

- After power-on, HDCP is resumed and decryption continues from the previously frozen state, without the need for re-authentication.
- For 8b/10b SST and 128b/132b, encryption suspend and resume procedure is straightforward. For 8b/10b MST it is more complicated.



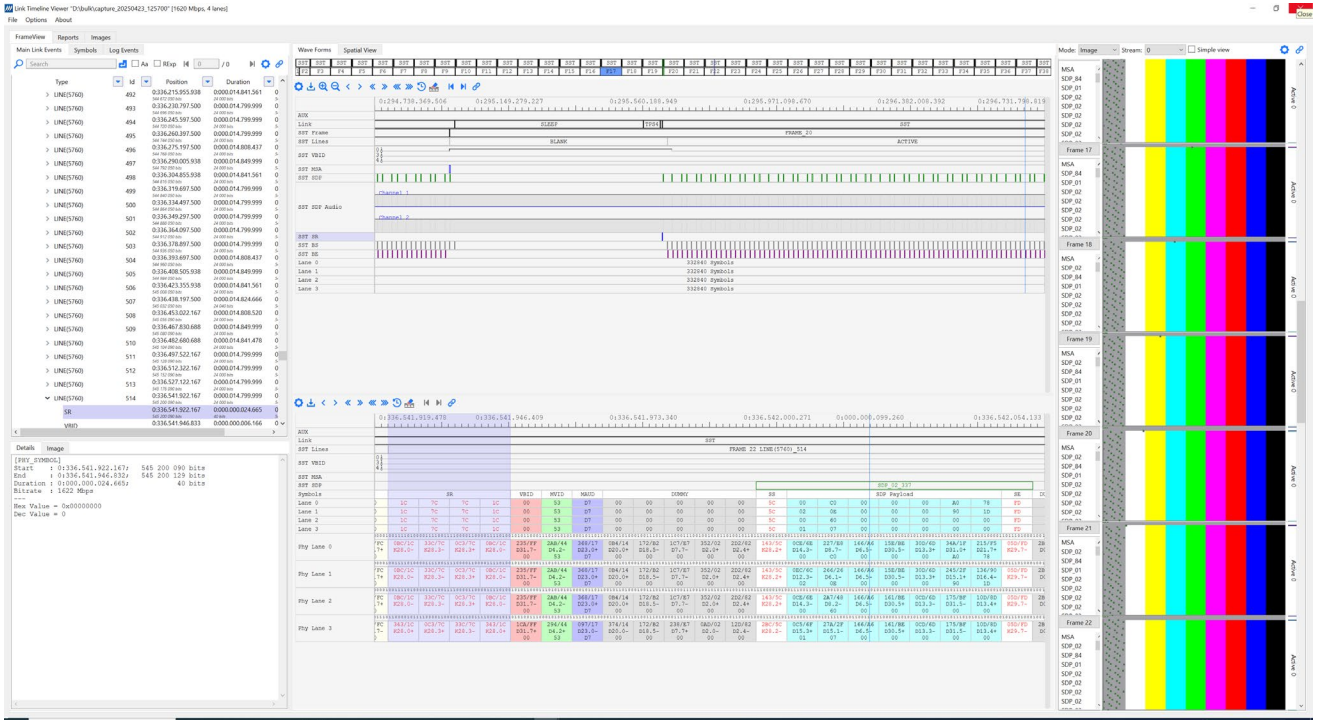
Panel Replay with ALPM

- When PR is in Active state, the Main Link can stay powered (option 1-A) or can be powered-off (option 1-C) using ALPM
- When ALPM is used, Sink and Source video timing synchronization is maintained using Adaptive-Sync SDPs, for each frame and at the same position.
- When ALPM is used, Early Transport is mandatory.
- Power-off is possible between SU regions, but the line interval still must be maintained.



DP Link Analyzer

A Unigraf tool for capturing Main-link Data Events and AUX Transactions. Within each frame, users can have a deep view of the events and metadata that occurs in each line. Measure distances in nanoseconds and symbol size to identify the length of problems in between events. Observe descrambled and scrambled symbols in hexadecimal format in each of the active lanes.



VESA
Display Performance Metrics

Robert Yang

Granite River Labs

2025 / 10 / 17

Tables

- VESA DPM Introduction
- VESA Certified — DisplayHDR – CTS1.2 Update
- VESA Certified — AdaptiveSync
- VESA Certified — ClearMR
- Common Issues
- Policy & Next Steps

VESA

VESA DPM Introduction

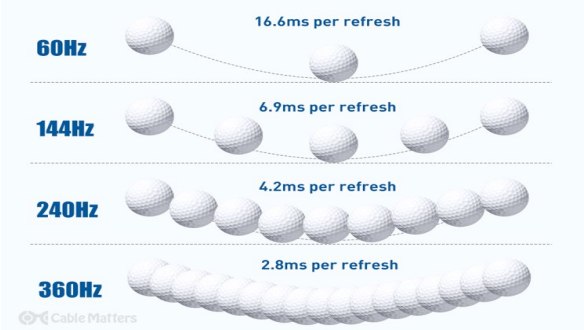
VESA Display Performance Metrics (DPM)

VESA CERTIFIED DisplayHDR™

- ✔Better brightness & contrast
- ✔Accurate color reproduction

VESA CERTIFIED AdaptiveSync DISPLAY 144

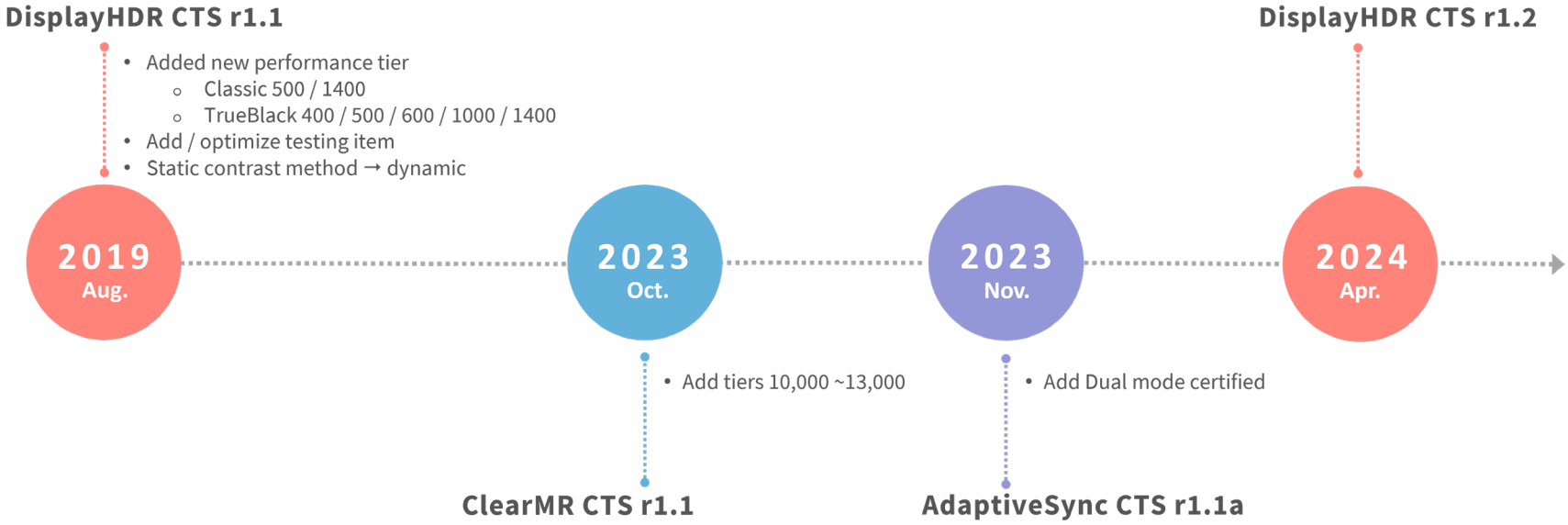
- ✔Dynamic refresh rate
- ✔Prevents tearing & stuttering



VESA CERTIFIED ClearMR

- ✔Motion clarity
- ✔Ratio of clear vs. blurry pixels

VESA DPM CTS Timeline



- The implementation deadline for the DisplayHDR CTS r1.2 specification:
  By the end of May **2025 for monitors.**
  By the end of May **2026 for laptops.**

VESA

VESA Certified — DisplayHDR

The Higher Standard for HDR Monitors

DisplayHDR CTS r1.1 vs r1.2

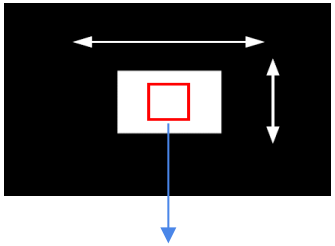
CTS No.	Test Tool No.	item
-	Reported Panel Characteristics	EDID.MaxLuminance
5.1.1	1a	10% Center Luminance Patch
5.1.2	2a	Flash Luminance Test
5.1.3	3a	Full Screen Luminance Test
5.2.1	4	Dual Corner Test
5.2.2	5 / 5.1 / 5.2	CheckerBoard Test
6	6	Color Gamut & Luminance Test
7	7	DisplayHDR Bit Depth
8	8	Rise Time measurements
9	9	Delta-ITP
10	1.2.1	Static Contrast Ratio Test
11	1.2.2	HDR vs. SDR Black Level Test
12	v1.2.3	Black Crush Test
13	1.2.4	Subtitle Luminance Flicker Test
14	1.2.5	XRite Color Square Test

CTS r1.2 New Item

Criteria update New Item

5.1.1 Center Luminance Patch

Test Pattern changed



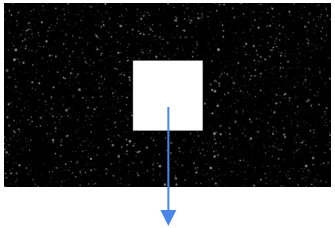
CTS 1.1: **10%** Center Patch

6. Color Gamut & Luminance Test

For HDR400: From 95% → 99% (sRGB)
For HDR500~1000: From 90% → 95% (DCI-P3)

7. DisplayHDR Bit Depth

For HDR400: From 8b → 8b+2b(w/ FRC)



CTS 1.2: 8% Center Patch+
Star field pattern

9. Delta-ITP

CTS1.1 : 5 cd/m^2 to 50% of Tier Level (6 step)
CTS1.2 : 1 cd/m^2 to 100% of Tier Level (8 step)

DisplayHDR r1.2 – Key Updates

Test / Specification		Performance Tier				
Test item	**Test Pattern**	**400**	**500**	**600**	**1000**	**1400**
10 Static Contrast Ratio Test	1D pattern for 400 / 500 / 600 2D pattern for 1000 / higher	1300:1	7000:1	8000:1	30k:1	50k:1
11 HDR vs. SDR Black Level Test	Black and white split-screen image	>90%				
12 Black Crush Test	Full screen black and dark-gray	5				

Ch10 Test Pattern

1D pattern: For DisplayHDR-400, 500, and 600

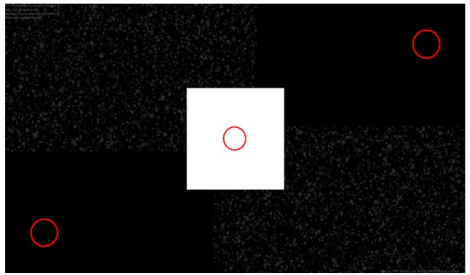


Figure 10-1: Static Contrast Ratio Test Pattern for DisplayHDR-400, 500, and 600 – Shown with Location Guidance Circles and Informational Text

2D pattern: For DisplayHDR 1000 and Higher

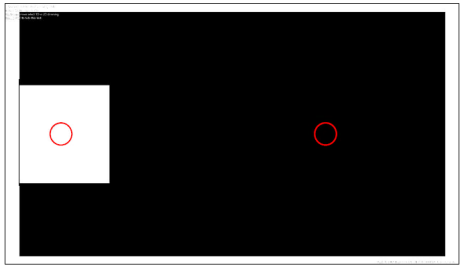


Figure 10-2: Static Contrast Ratio Test Pattern for DisplayHDR-1000 and 1400 – Shown with Measurement Location Circles and Informational Text

Ch12 Test Pattern

Full screen, five test images: 0, 0.05, 0.1, 0.3, 0.5 cd/m^2

DisplayHDR r1.2 – Key Updates

Test / Specification		Performance Tier				
Test item	**Test Pattern**	**400**	**500**	**600**	**1000**	**1400**
13 Subtitle Luminance Flicker Test	Gray 8% center square at 10 cd/m²	13%			10%	
14 XRite Color Square Test	50, 100 cd/m², 50% of Logo Level	8			6	

CH13 Test Pattern

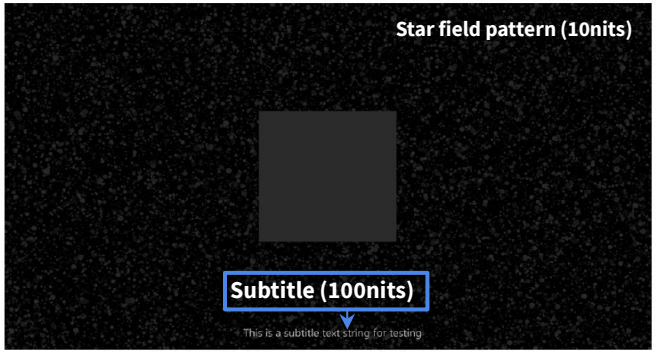


Figure 13-1: Subtitle Flicker Test – Gray Center Square Luminance
Should Not Change as Subtitles Appear and Disappear from the Screen

CH14 Test Pattern (Delta-TP)

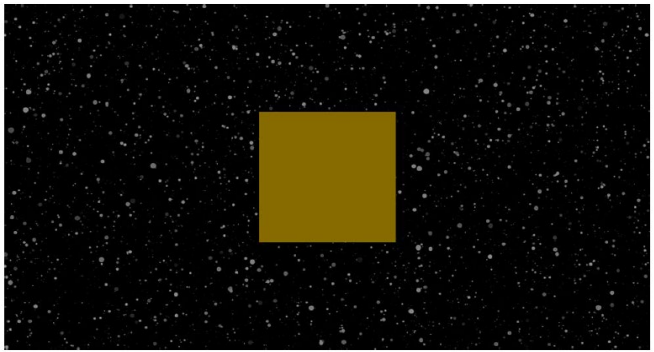


Figure 14-1: Xrite Color Square Test – One of 96 Test Colors,
Tested at Three Different Luminance Levels

VESA

VESA Certified — AdaptiveSync

Flawless Frames, Every Time

AdaptiveSync Certification

- Work by dynamically adjusting the display's refresh rate to match the GPU's frame rate output

Certified Logos

VESA CERTIFIED MediaSync DISPLAY

VESA CERTIFIED AdaptiveSync DISPLAY 144

VESA CERTIFIED AdaptiveSync DISPLAY 240 2160P | DISPLAY 480 1080P

MediaSync

Jitter-free media playback
Max RR ≧ 60Hz ;
Min RR ≦ 48Hz

AdaptiveSync (144Hz↑)

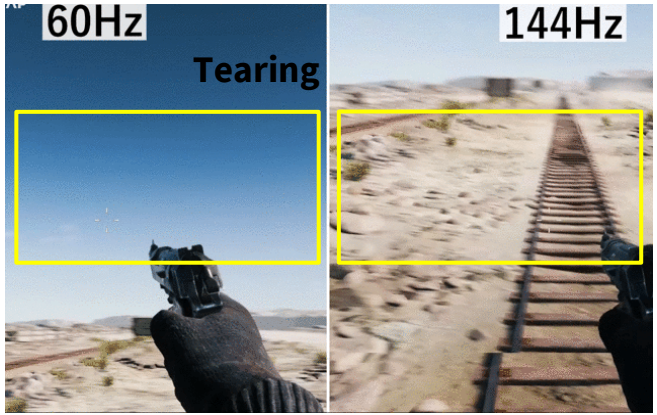
Optimized for gaming
Max RR ≧ 144Hz
Min RR ≦ 60Hz

Dual Mode Logo

Left: Native resolution & max RR
Right: Alternative resolution & max RR

Smooth & Tear-Free Motion

Low Latency & Fast Response



VESA

VESA Certified — ClearMR

Clarity in Motion

ClearMR Key Updates

- ☑ Standardized motion quality metric
- ☑ Smoother motion, less ghosting

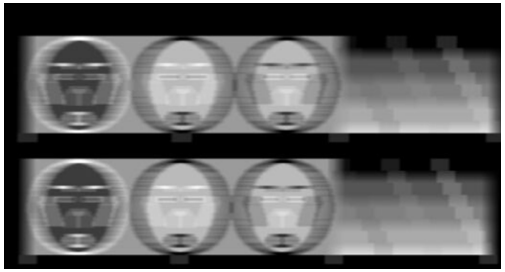
VESA CERTIFIED ClearMR 13000

Clear Pixels : blurry pixels = 130 : 1

ClearMR Tier	CMR Range
3000	2500 ≤ CMR < 3500
4000	3500 ≤ CMR < 4500
5000	4500 ≤ CMR < 5500
6000	5500 ≤ CMR < 6500
7000	6500 ≤ CMR < 7500
8000	7500 ≤ CMR < 8500
9000	8500 ≤ CMR < 9500
10000	9500 ≤ CMR < 10500
11000	10500 ≤ CMR < 11500
12000	11500 ≤ CMR < 12500
13000	12500 ≤ CMR < 14000
15000	**14000 ≤ CMR < 16500**
18000	**16500 ≤ CMR < 19500**
21000	**19500 ≤ CMR**

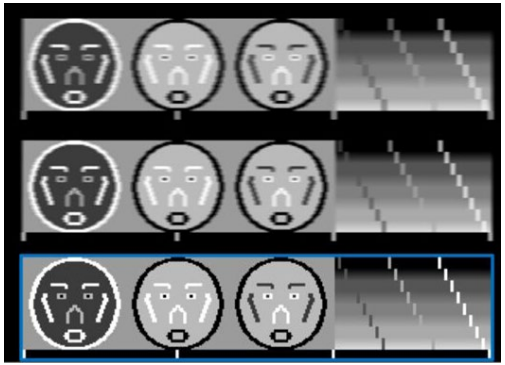
ClearMR tiers update in 2025/04

Highest tier increased from
ClearMR 13000 → ClearMR 21000



Higher ClearMR Tiers

motion looks clearer and closer to still image



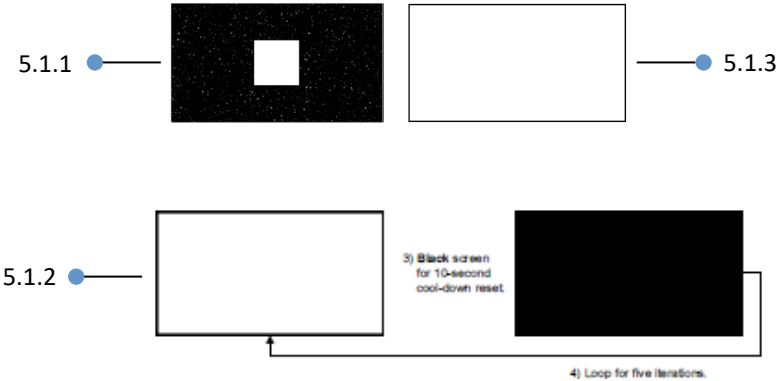
Still Image

Common Issues

DisplayHDR – Common Test Issues

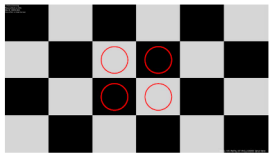
Overall brightness

- 5.1.1 - 10% Center Luminance
- 5.1.2 - Flash Luminance Test
- 5.1.3 - Full Screen Luminance Test

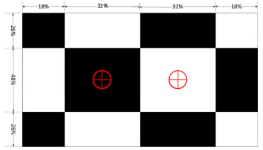


Local dimming capability

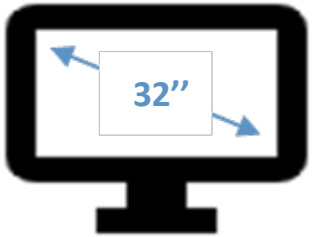
- 5.2.2 - CheckerBoard Test



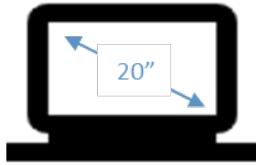
6x4 Pattern



4x3 Pattern



Monitor



Laptop

Adaptive Sync – Common Test Issues

G2G Response Time and Overdrive

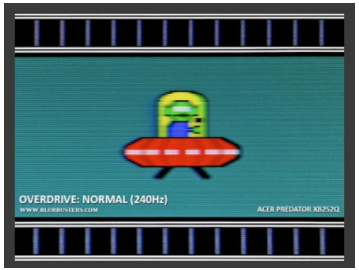
☑ Why is G2G important?

- No ghosting/trailing
- Sharper edges in motion
- Key for gaming & video

☑ Overdrive & Pixel Errors

- Stronger voltage → Faster response
- Overshoot = Bright halo / inverse ghosting
- Undershoot = Dark trailing

OD: Off / Lowest Setting (Ghosting)



OD: Normal / Medium-High Setting (Clear)

OD: Extreme Setting (Inverse Ghosting)

VESA

Policy & Next Steps

Family Definition

- Extra rules for **laptops**; other cases follow official Family Model Form/File.

Criteria	VESA CERTIFIED DisplayHDR™	VESA CERTIFIED AdaptiveSync DISPLAY 144	VESA CERTIFIED ClearMR	Examples
CPU - Cross Generation	✓	✗	✗	13th RPL & 14th MTL
CPU - Different Core family	✓	✗	✗	RPL-U & RPL-P
CPU - Different Series	✓	✓	✓	i5 & i7
GPU – Different brand / generation	✗	✗	✗	RTX 4080 & RTX 3070
GPU – Same brand generation, different Series	▲	▲	▲	RTX 5090 & RTX 5070

✓ = Can apply family model
✗ = Cannot apply family model
▲ = Case by case

DPM Path Forward

AdaptiveSync for HDMI TVs

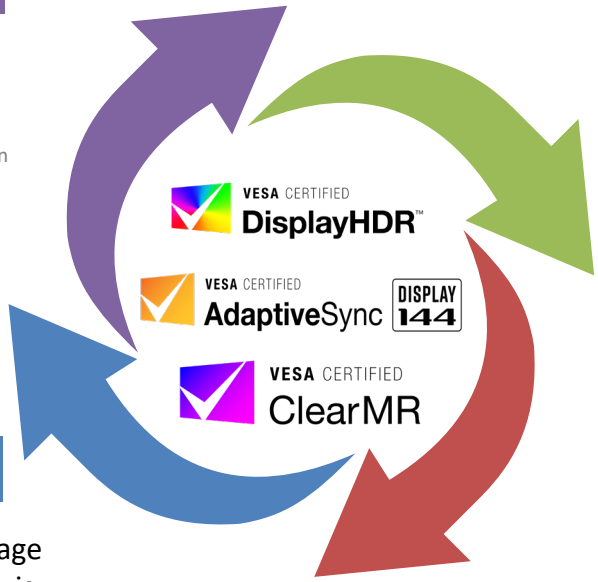
- Extend certification to HDMI-only TVs
- Validate HDMI VRR & tool readiness

Ref: DPM250408mn, DPM250429mn, DPM250603mn

Logo Expansion

- Extend to GPUs & test instruments
- Define CTS & qualification rules

Ref: DPM250114mn, DPM250603mn



DisplayHDR 2.0

- Advanced Color – add Rec.2020 coverage
- New Test Elements – reflectivity, off-axis performance, halo/starfield

Ref: DPM250114mn, DPM250311mn, DPM250603mn
2024.05.07 VESA DPM - DisplayHDR² Proposal

AR/VR & Multi-Platform Tools

- AR/VR-specific methods
- Tools beyond Windows → Linux

Ref: DPM250311mn, DPM250408mn, DPM250603mn

GRL Worldwide Locations

- Silicon Valley HQ, 9 labs around the world, > 350 employees
- Recognized World Leader in Test Services and Automation Solutions for Connectivity and Charging

WW HQ & Lab
Santa Clara, CA

US R&D
Austin, TX

Taiwan Lab
Taipei

India R&D & Lab
Bangalore

Japan Lab
Yokohama

Korea Lab
Incheon

Asia Pacific HQ
Singapore

Malaysia R&D
Penang

China Lab
Shanghai

China Lab
Dongguan

Germany Lab
Karlsruhe

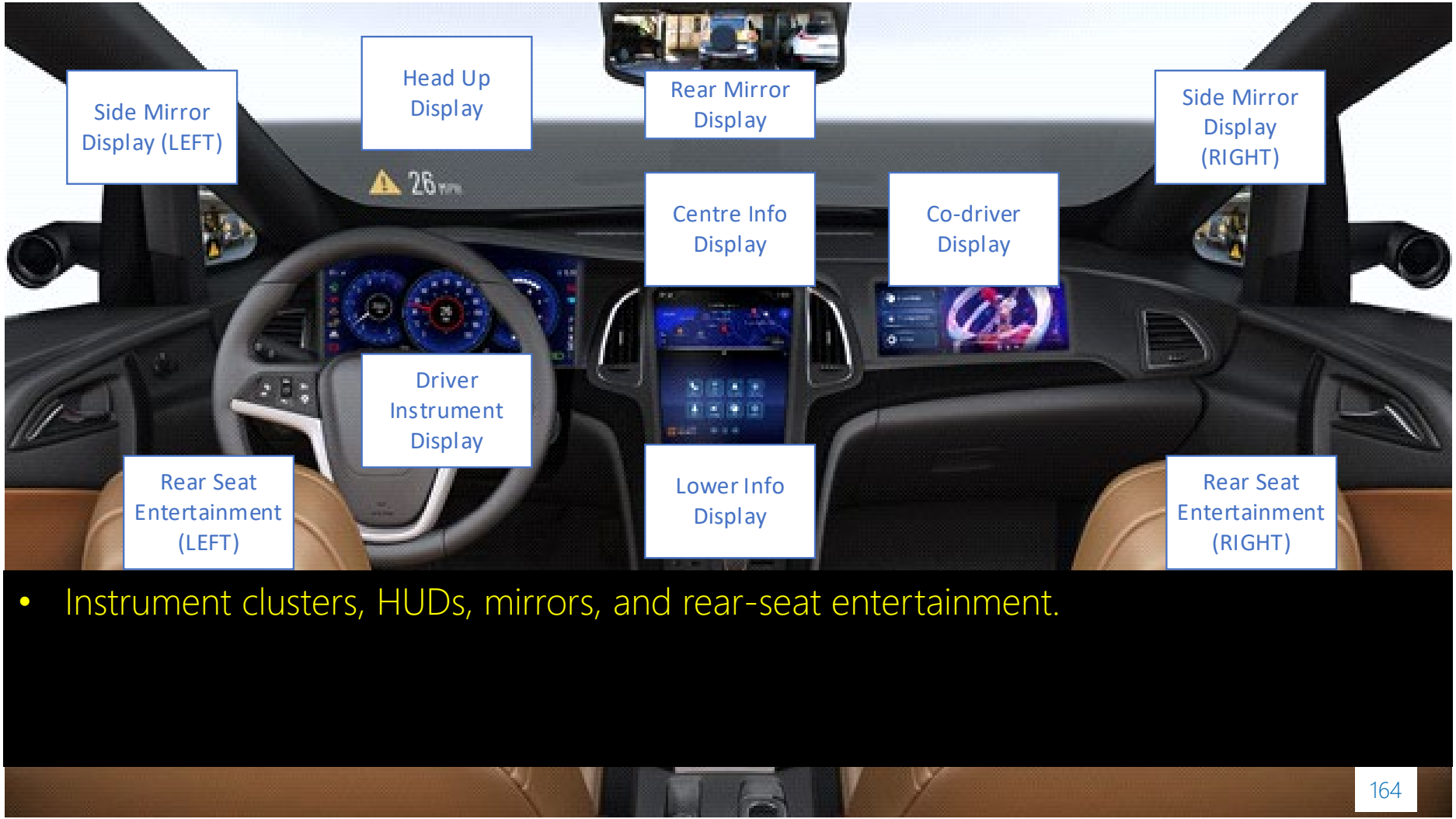
Belgium Lab
Hasselt

Introduction to VESA
DisplayPort Automotive Extensions

James Goel
DisplayPort Auto Extensions Sub-Group Chair
VESA Board Member

Tung-Sheng Lin
Senior Technical Manager
MediaTek USA Inc.

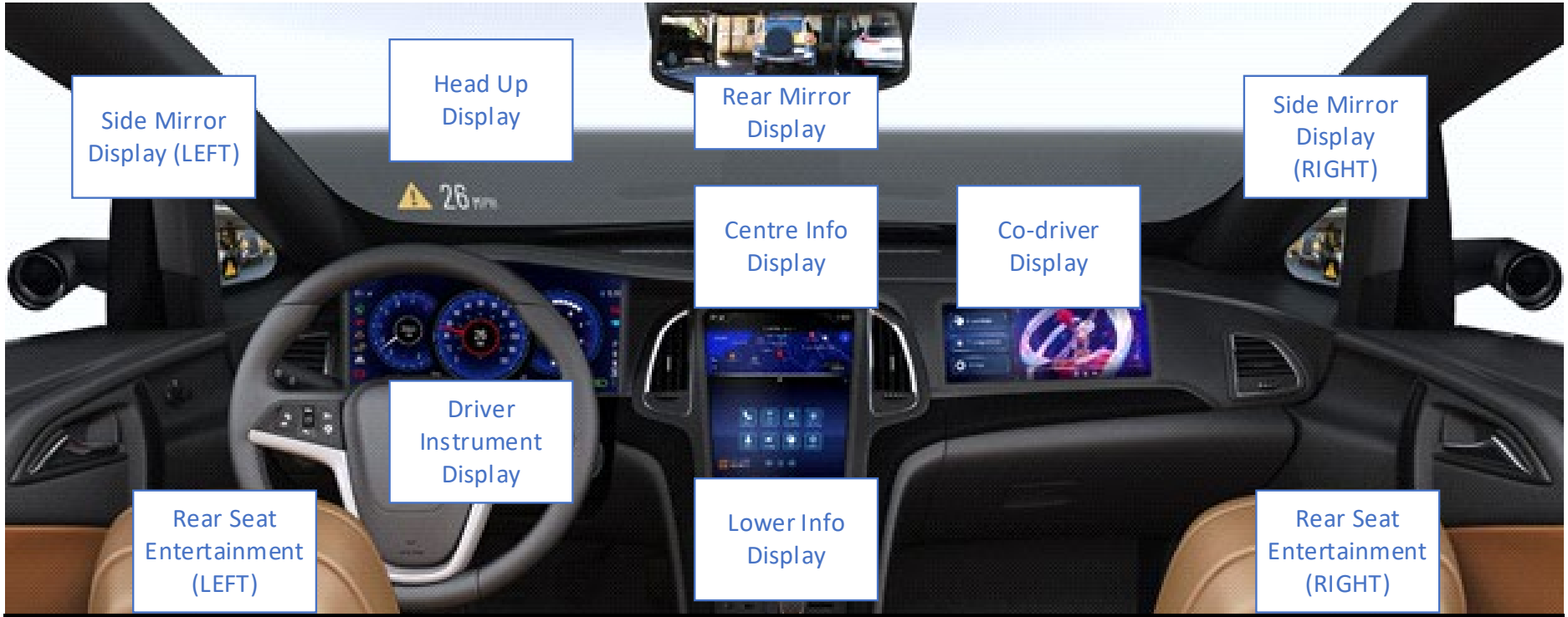

Side Mirror Display (LEFT)
Head Up Display
Rear Mirror Display
Side Mirror Display (RIGHT)
Centre Info Display
Co-driver Display
Driver Instrument Display
Rear Seat Entertainment (LEFT)
Lower Info Display
Rear Seat Entertainment (RIGHT)
GAME OVER



- Instrument clusters, HUDs, mirrors, and rear-seat entertainment.

- Instrument clusters, HUDs, mirrors, and rear-seat entertainment
- ASIL-D safety, UN155 and ISO 21434 security may be required

- Instrument clusters, HUDs, mirrors, and rear-seat entertainment
- ASIL-D safety, UN155 and ISO 21434 security may be required
- Existing DP/eDP protocols were not built with these challenges in mind.



- Instrument clusters, HUDs, mirrors, and rear-seat entertainment
- ASIL-D safety, UN155 and ISO 21434 security may be required
- Existing DP/eDP protocols were not built with these challenges in mind.
- Forcing OEMs into fragmented, non-standard solutions.

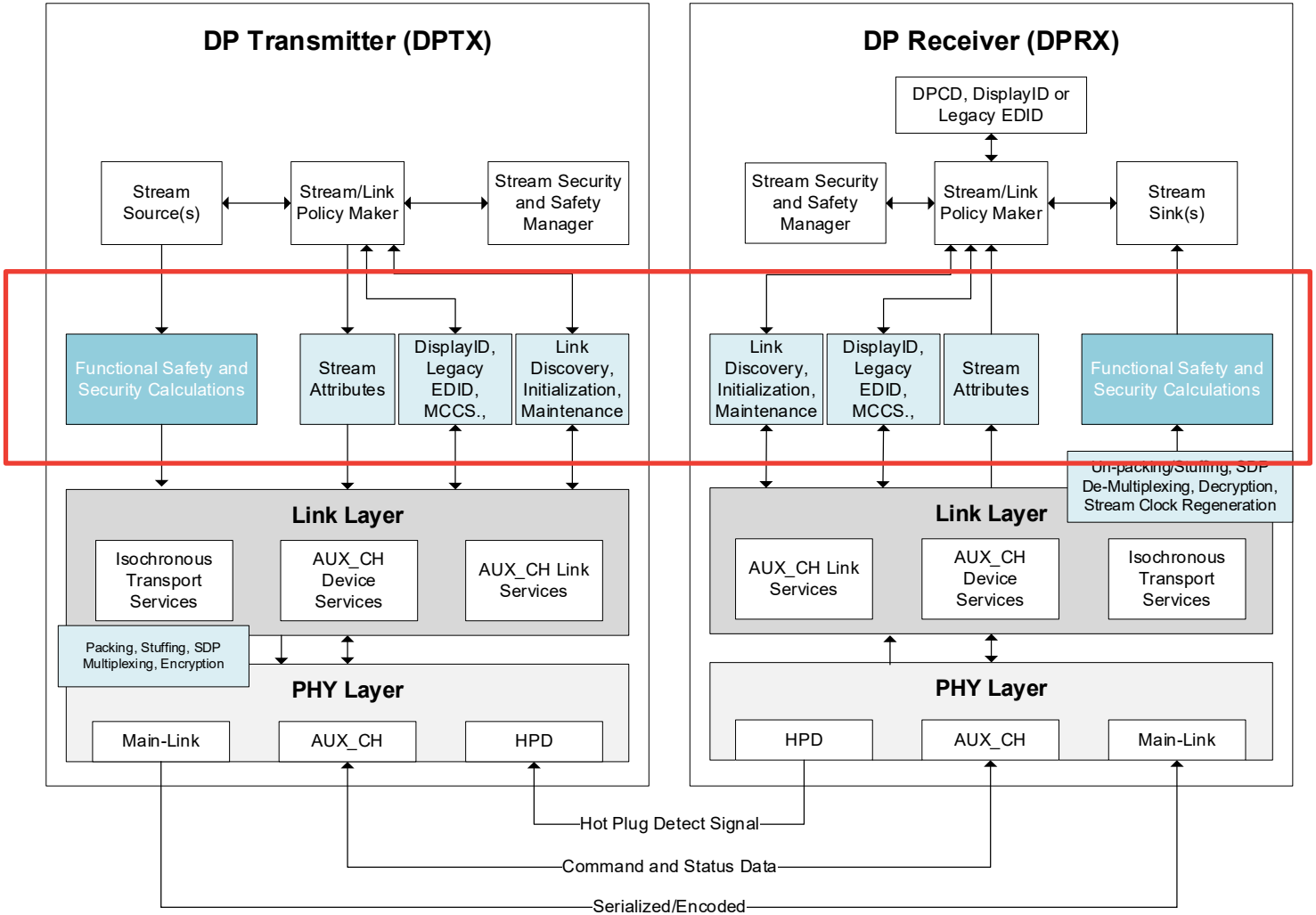

62 °F
12:30
AUTO
SRS AIRBAG
2550
RPM
26
MPH
KM/H
FUEL RANGE
278
MILES
E
F
H
C
MAINT REQD
P
R
N
D
L
TRIP A
1508 mi
22360 mi

- Entire video frame protected by Cyclic-Redundancy-Check Codes
- Additional Automotive grade Security (DMTF SPDM, MAC, DP AUX Encryption) available
- Important Regions-of-Interest protected with Cyclic-Redundancy-Check Codes

- Entire video frame protected by Cyclic-Redundancy-Check Codes
- Additional Automotive-grade Security (DMTF SPDM, MAC, DP AUX Encryption) available
- Important Regions-of-Interest protected with Cyclic-Redundancy-Check Codes
- Display Safety Icons gain extra protection

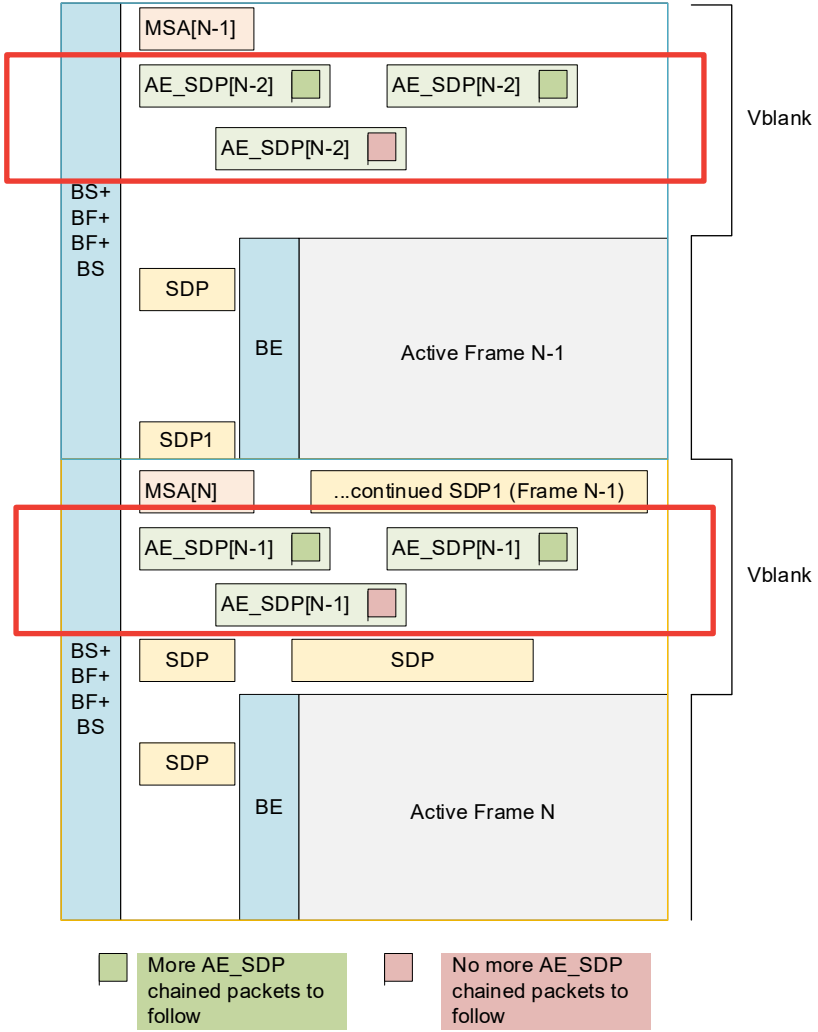
Solution Summary – Introducing DisplayPort Automotive Extension (DP-AE)

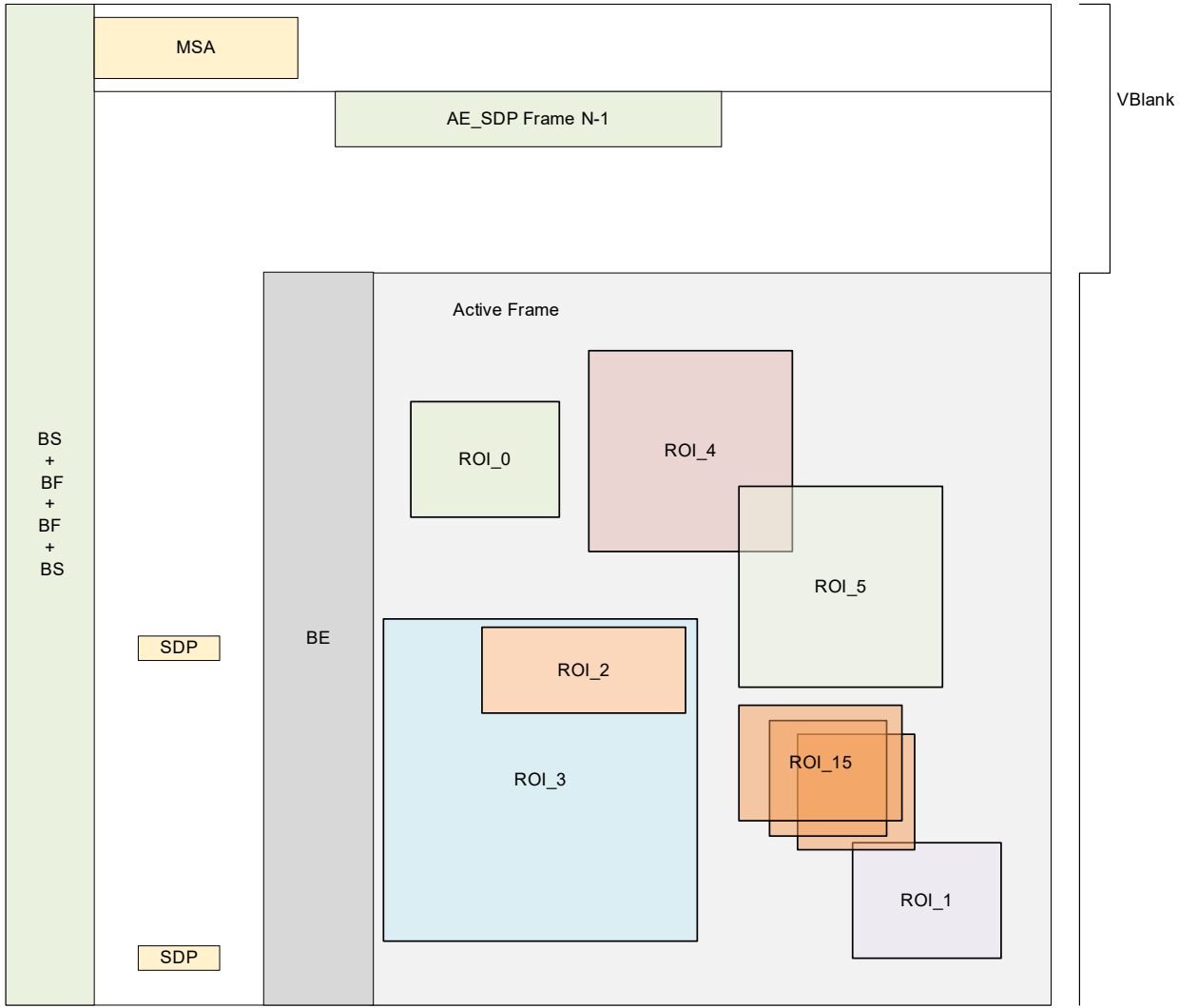
- Builds on DP 2.1a/eDP 2.0 with safety & security enhancements
- Functional Safety via ROI CRCs, Frame Counters, Timeout Monitoring
  - Per region CRCs (up to 16 ROIs)
  - Automatic SafeState transitions
- Data Integrity with SPDM (Security Protocol and Data Model) authentication & MAC (Message Authentication Code) tagging
- Secure AUX messaging & protocol stack isolation
- End-to-end Safety/Security supporting CRCs, MACs, SPDM-based authentication
- Support for Superframes and Subframes
- C-Model Emulator enables compliance testing
- Low complexity, high ecosystem readiness


DP Transmitter (DPTX)
DP Receiver (DPRX)
DPCD, DisplayID or Legacy EDID
Stream Source(s)
Stream/Link Policy Maker
Stream Security and Safety Manager
Stream Security and Safety Manager
Stream/Link Policy Maker
Stream Sink(s)
Functional Safety and Security Calculations
Stream Attributes
DisplayID, Legacy EDID, MCCS.,
Link Discovery, Initialization, Maintenance
Link Discovery, Initialization, Maintenance
DisplayID, Legacy EDID, MCCS.,
Stream Attributes
Functional Safety and Security Calculations
Un-packing/Stuffing, SDP De-Multiplexing, Decryption, Stream Clock Regeneration
Link Layer
Isochronous Transport Services
AUX_CH Device Services
AUX_CH Link Services
Link Layer
AUX_CH Link Services
AUX_CH Device Services
Isochronous Transport Services
Packing, Stuffing, SDP Multiplexing, Encryption
PHY Layer
Main-Link
AUX_CH
HPD
PHY Layer
HPD
AUX_CH
Main-Link
Hot Plug Detect Signal
Command and Status Data
Serialized/Encoded

DP-AE Protocol Stack Overview

- Layers added:
  - CRCs for Datapath, MSA and Secondary Data Packets
  - DP AUX Side-Channel VESA Auto Extension Layer (VAL) messaging
  - AUX-Channel Secure Transport Layer (VSTL)
  - MACs for Datapath, MSA and Active Frame data
  - Application Layer (extensive DPCD Registers)
- Uses existing AUX/SDP channels
  - Designed for static automotive topologies


MSA[N-1]
AE_SDP[N-2]
AE_SDP[N-2]
AE_SDP[N-2]
Vblank
BS+
BF+
BF+
BS
SDP
BE
Active Frame N-1
SDP1
MSA[N]
...continued SDP1 (Frame N-1)
AE_SDP[N-1]
AE_SDP[N-1]
AE_SDP[N-1]
Vblank
BS+
BF+
BF+
BS
SDP
SDP
SDP
BE
Active Frame N
More AE_SDP chained packets to follow
No more AE_SDP chained packets to follow

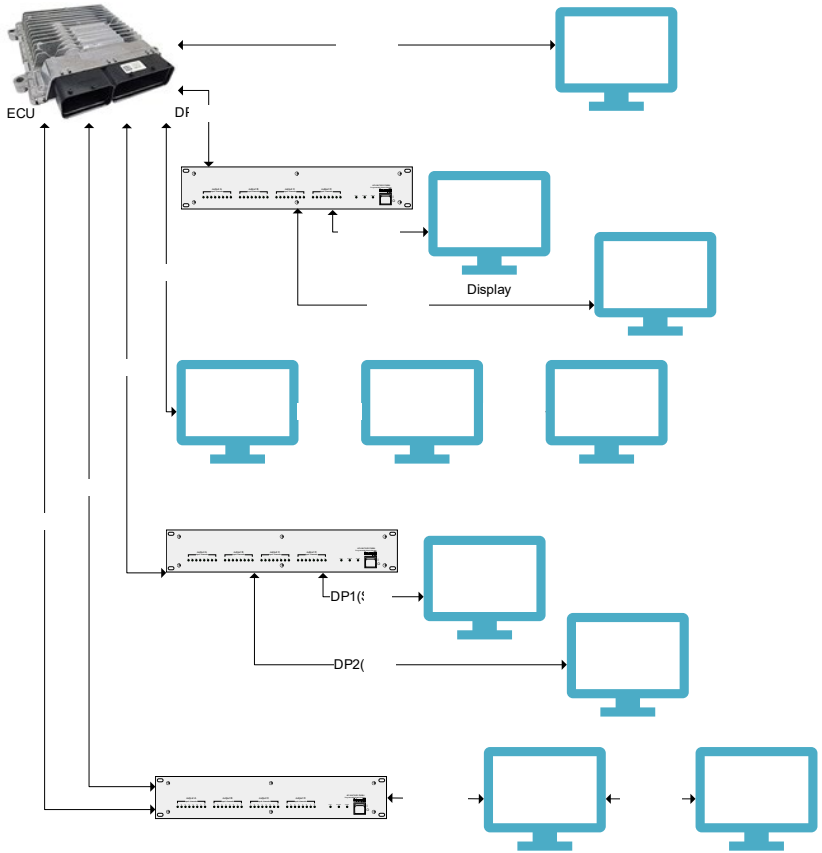

MSA
AE_SDP Frame N-1
VBlank
BS
+
BF
+
BF
+
BS
Active Frame
ROI_0
ROI_4
ROI_5
SDP
BE
ROI_2
ROI_3
ROI_15
ROI_1
SDP

Addressing Functional Safety and Security Gaps

- New functional safety protocol enhancements
  - New protocols to aid ISO 26262 ASIL-D certification
  - CRC, Frame and Time-Out Monitoring
  - Definitions and state transitions for soft failure recovery and escalation to hard failure
- New Automotive Compliant Security
  - UN155 Regulation Compliant and ISO 21434 certifiable
  - Security Protocol using Standard DMTF™ SPDM and use of NIST Compliant Algorithms
  - Source, Sink and DP AUX Channel Protection (Integrity, Encryption)
- All these FuSa and security enhancements are included in the C-Model Emulator for CTS

System Topologies and Profiles

- Static topologies assumed for automotive (ROM config ready)
- Supports SST/MST, SerDes bridge, Branch/Composite Devices
- Profiles 1–4:
  - Profile 1: End-to-End functional safety support for data plane and basic Hop-to-Hop functional safety support through direct DPCD register access
  - Profile 2: Profile 1 plus support for DP_AUX message client 16-bit CRC validation
  - Profile 3: Profile 2 plus advanced security for DP_AUX messages
  - Profile 4: Profile 3 plus authentication and integrity for VESA data plane
- VESA AE certification will be issued based on the profiles supported by the automotive platform


ECU
Display
DP1(S
DP2(

AE Spec Feature	Normative Section All part shall be implemented	AE Spec Category	Basic FuSa		Advanced FuSa (Basic Ctrl Plane Security)	FuSa with Enhanced Security
			Profile 1	Profile 2	Profile 3	Profile 4
Uncompressed Pixel Frame CRC or Reconstructed Pixel CRC per Slice Column	Chapter 10 - DP Auto Extensions Functional Safety using CRC	FuSa	Normative	Normative	Normative	Normative
Compressed Pixel Frame CRC	Optional	FuSa	Optional	Optional	Optional	Optional
CRC on defined SDPs	Chapter 10 - DP Auto Extensions Functional Safety using CRC	FuSa	Normative	Normative	Normative	Normative
CRC on MSA	Chapter 10 - DP Auto Extensions Functional Safety using CRC	FuSa	Normative	Normative	Normative	Normative
CRC on Regions-of-Interest Support (Max 16)	Chapter 10 - DP Auto Extensions Functional Safety using CRC	FuSa	"Min ROI Req of 0"	"Min ROI Req of 4"	"Min ROI Req of 4"	"Min ROI Req of 4"
Frame drop/repeat and timeout monitoring check	Chapter 12 - Auto FuSa Frame Count and Timeout Monitor	FuSa	Normative	Normative	Normative	Normative
Basic Safety App (Direct DPCD Register access)	Chapter 6 - DPCD Regs	FuSa	Normative	Normative	Normative	Normative
Support for DP_AUX messaging client plus DPCD Reg Access	Chapter 8 - Control Plane Protocol Stack	Security	Not supported	Normative	Normative	Normative
Basic Safety App with Get_Measure using VAL	Chapter 8 - Control Plane Protocol Stack	FuSa	Not supported	Normative	Normative	Normative
VESA Secure Transport Layer (VSTL)	Ch 8 and 9 - Security	FuSa	Not supported	Not supported	Normative	Normative
"Data Plane Security (Only Auth and Integrity)"	Ch 8 and 9 - Security	Security	Not supported	Not supported	Not supported	Normative
MAC on Uncompressed Pixel/Compressed Bytes +MSA	Ch 8 and 9 - Security	Security	Not supported	Not supported	Not supported	Normative
Full Integrity Security on AE_SDP data	Ch 8 and 9 – Security	Security	Not supported	Not supported	Not supported	Normative
MAC on AE_SDP data	Ch 8 and 9 - Security	Security	Not supported	Not supported	Not supported	Normative
Data Plane Confidentiality	Ch 8 and 9 - Security	Security	Not supported	Not supported	Not supported	Not supported
Super Frames	Chapter 11 - Superframes	FuSa	Optional	Optional	Optional	Optional

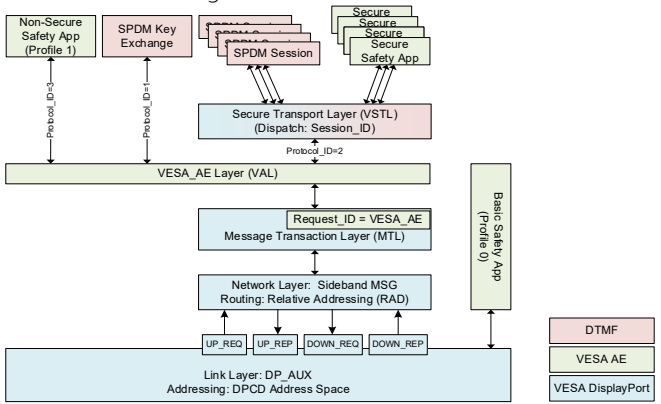
Addressing Security Gaps (Profile 3/4)

- Profile 3 Security
  - Same as Profile 2 (primary use of Message AUX client)
  - Security enforcement on the **control plane**
    - End-to-End device authentication using SPDM
    - VESA_AE Layer (VAL)
    - VESA_AE Secure Transport Layer (VSTL)
- Profile 4 Security
  - Same as Profile 3 (security on control plane)
  - Security enforcement on the **data plane**
    - DP frame integrity protection of AE_SDP, MSA and Active Pixel Data
    - AES-128-GMAC, AES-256-GMAC
    - Frame Keys generated from SPDM authentication (profile 3)
- Security and Safety can co-exist together or supported separately
  - Expectation is automotive systems will support Safety or Safety + Security

Security Profile 3

- VESA_AE Layer (VAL)
  - Used by Safety Applications in Profile 2
  - Operates on top of Message AUX Client Transport Layer
    - Message Transaction Layer (MTL)
    - Sideband messaging
    - Relative Addressing (RAD) routing
    - DPCD
  - Protocol in packet formation for secure and non-secure applications
  - Supported on DP SOURCE, DP SINK and DP Bridges

Figure 8-1



- VAL Protocol Data Unit
  - Carries the payload data from the secure and non-secure applications operating on top of the VAL
  - Protocol ID (4-bit identifier), CRC16

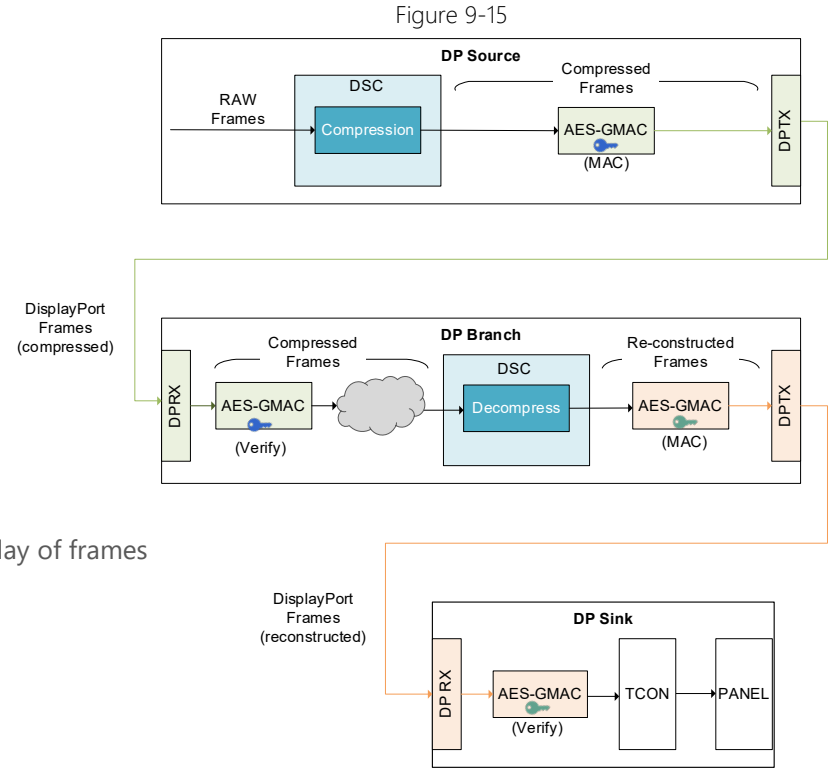
- VSTL Protocol Data Unit
  - Protected payload data from the secure applications (i.e. SPDM)
  - Session ID (4 bytes)
  - Protected by either AES-GCM (encryption, integrity) or AES-GMAC (integrity)
  - Embedded in the VAL PDU
  - VSTL API definitions (recommendation)

- Defined Safety and Security Message Types
  - Intended for read/write access to the DP VESA AE tables (i.e. DP SOURCE -> DP SINK)

Security Profile 4

- Supports Profile 3
  - Control Plane Security
- Data Plane Security
  - NIST compliant AES-GMAC (SP800-38D)
  - 128-bit security mandatory
  - 256-bit security is optional
  - Integrity only
- Security supported for AE_SDP, MSA and Active Pixels
  - Each are integrity protected
  - MAC for AE_SDP, MSA and Active pixels
  - Security enablement flag (SECURITY_PROT)
  - Separate SECURITY_CTR field from safety and ensures no replay of frames
- Key Management
  - Key update support (KEY_SEL)
- DP Modes
  - SST, MST, Superframe
- DP Devices
  - Source, DP Sink, DP Composite/Branch

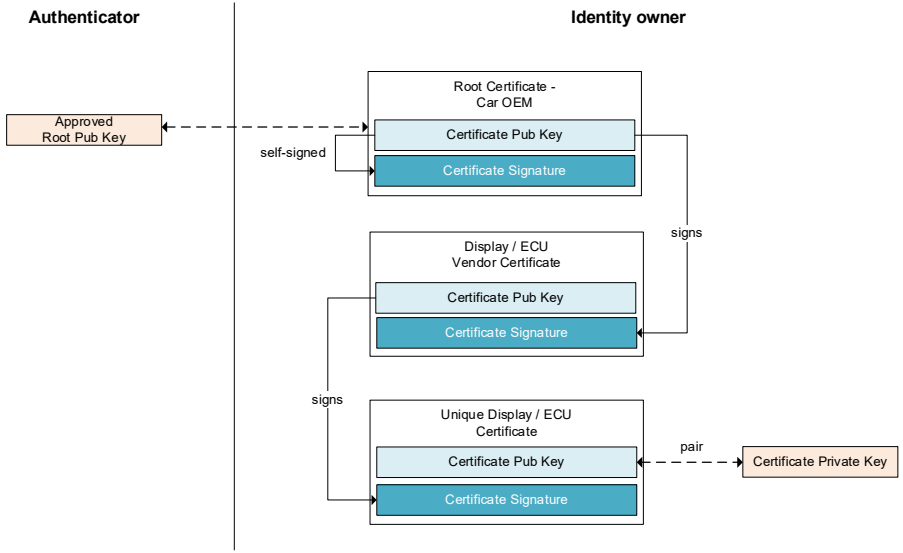
Figure 9-15



DP Device Authentication (Profile 3/4)

- Ensures use authorize parts
  - Cryptographic security to prevent installing counterfeit parts
  - DP Source, DP Sink, DP Bridges
- Certificate Base Authentication using Asymmetric Key Pair (CAKP)
  - X509 Certificate
  - Asymmetric base (RSA, ECDSA)
  - Mutual Authentication, One-way Authentication
  - PKI provisioning (more secure)
- Pre-shared Secret Key (PSK)
  - Shared secret
  - symmetric base
  - Shared secret provisioning (less secure)
- Pairing
  - Initially start with CAKP at the factory
  - Generate pairing key that is used for PSK (normal operating mode)
- SPDM Profiles
  - Selection of Cryptographic support used in different regions
  - Profile A: North/South Americas, Profile B: Western Europe, Profile C: China

Figure 9-2



Industry Security Regulations & Compliance

- **UNECE WP.29 R155**
  - Regulations dealing with vehicle cybersecurity
  - Provides a framework
  - Sets requirements to withstand cyberattacks
  - Mandatory in many countries by 2024 (EU, UK, Japan, etc.)
- **ISO/SAE 21434**
  - *Road vehicles – Cybersecurity Engineering*
  - Automotive industry standard
  - Identifies the engineering requirements for cybersecurity risk management for the lifecycle of the vehicle
  - Process-oriented approach to identify and mitigate cybersecurity risks
  - Intended for designing security into vehicles from the beginning
  - Widely adopted
- **NIST Compliance**
  - SP800-38D
  - Control plane AES-GCM (Profile 3/4)
  - Data plane AES-GMAC (Profile 4)

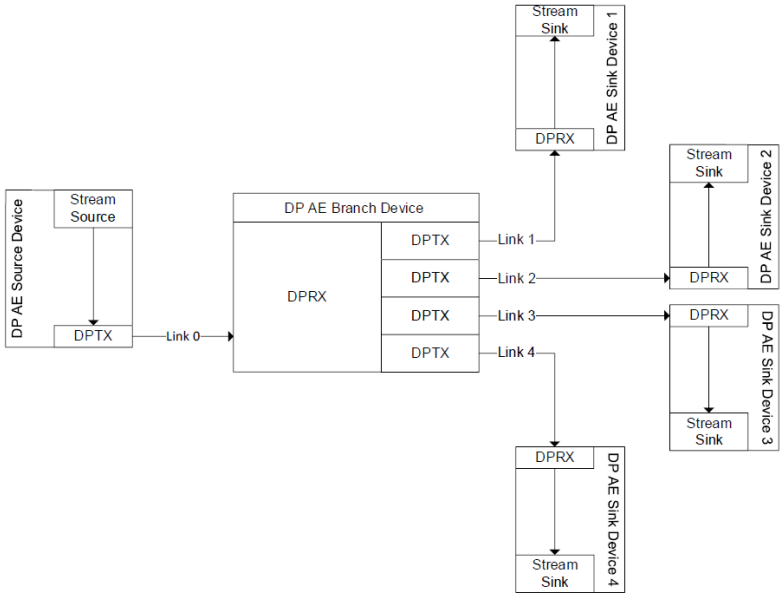
Security with Control and Data Plane Protection

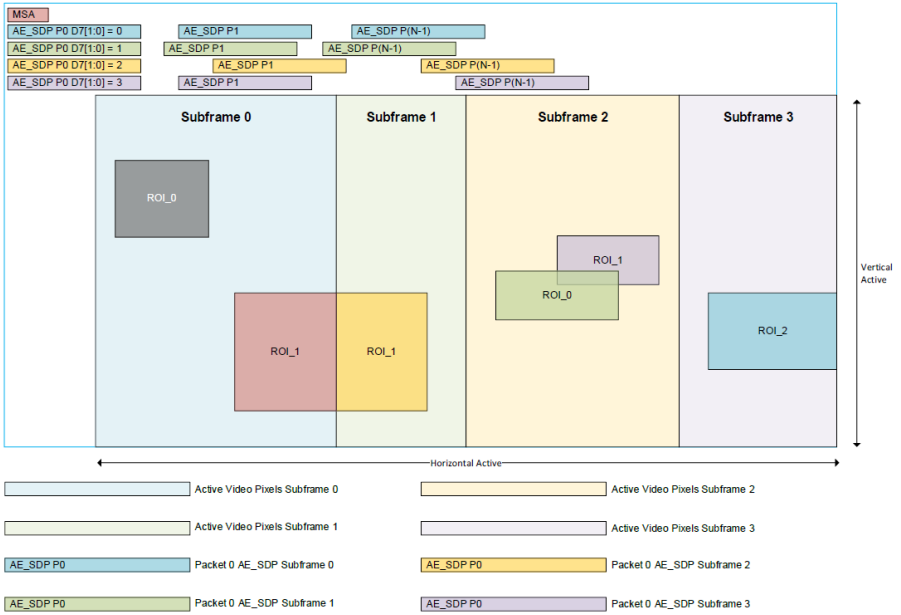
- SPDM handshake for Source-Sink authentication
  - Defined set of SPDM Profiles
- Control Plane protection using AES-GCM/GMAC on DP AUX message clients
  - Configurable encryption handling
- Data Plane integrity protection using AES-GMAC on MSA, active frame data and AE_SDP
  - 128-bit or 256-bit security
- Secure session management via VSTL

Superframe

- Allow a Source device to transmit multiple subframes (up to 4) within one SST or MST link, one AUX_CH and one HPD connected to a DP Composite device
- All subframes shall have:
  - An equal refresh rate
  - The same colorimetry
  - The same pixel format of YCbCr 4:4:4/RGB 4:4:4, although other pixel format may be supported
  - The same color depth
- Simplify connectivity while maintaining the versatility of DP AE functions

Superframe (cont'd)

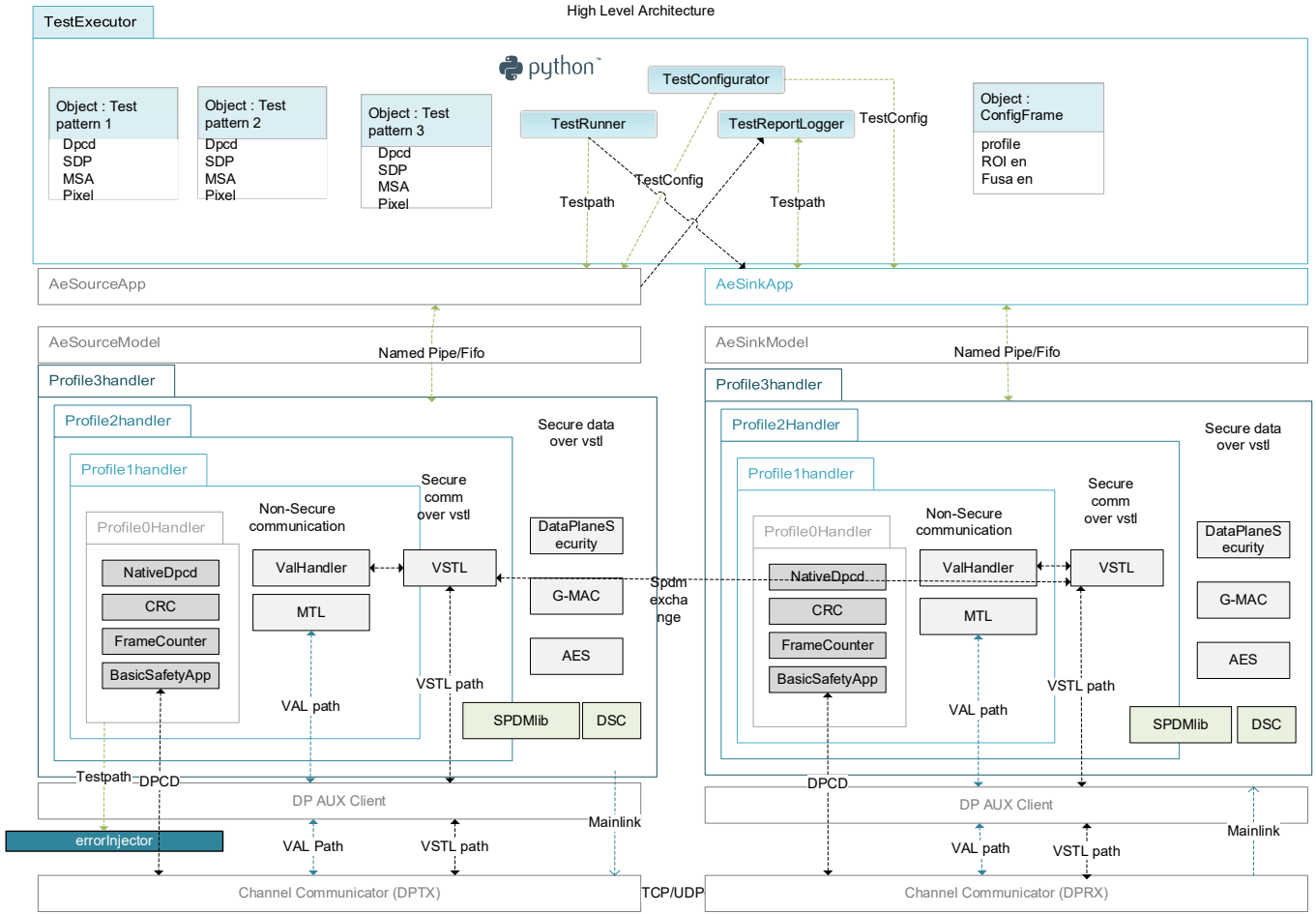




The VESA C-Model Emulator for Rapid Testing

- Virtual model implements the DP-AE protocol
- TCP/UDP-based simulation of AUX and frame channels
- Supports:
  - Fault injection
  - ROI on-the-fly changes
  - Self-testing and automation (Python API)
- Deployable across internal QA & OEM validation

C-Model Emulator Architecture



Executive Summary

VESA's new DisplayPort Automotive Extension (DP-AE) protocol brings critical functional safety and security features to the DisplayPort standard, enabling OEM's to meet the various regulations, compliance and certification standards (i.e. ISO26262 and ISO21434). Such features includes support for end-to-end CRC and MAC validation, secure AUX messaging, and SPDM-based device authentication.

In addition, the C-Model emulator allows engineers to simulate, test, and verify DP-AE behaviour virtually, accelerating compliance cycles and reducing risk. With backward compatibility and a flexible profile system, DP-AE enables scalable adoption across the automotive display ecosystem.

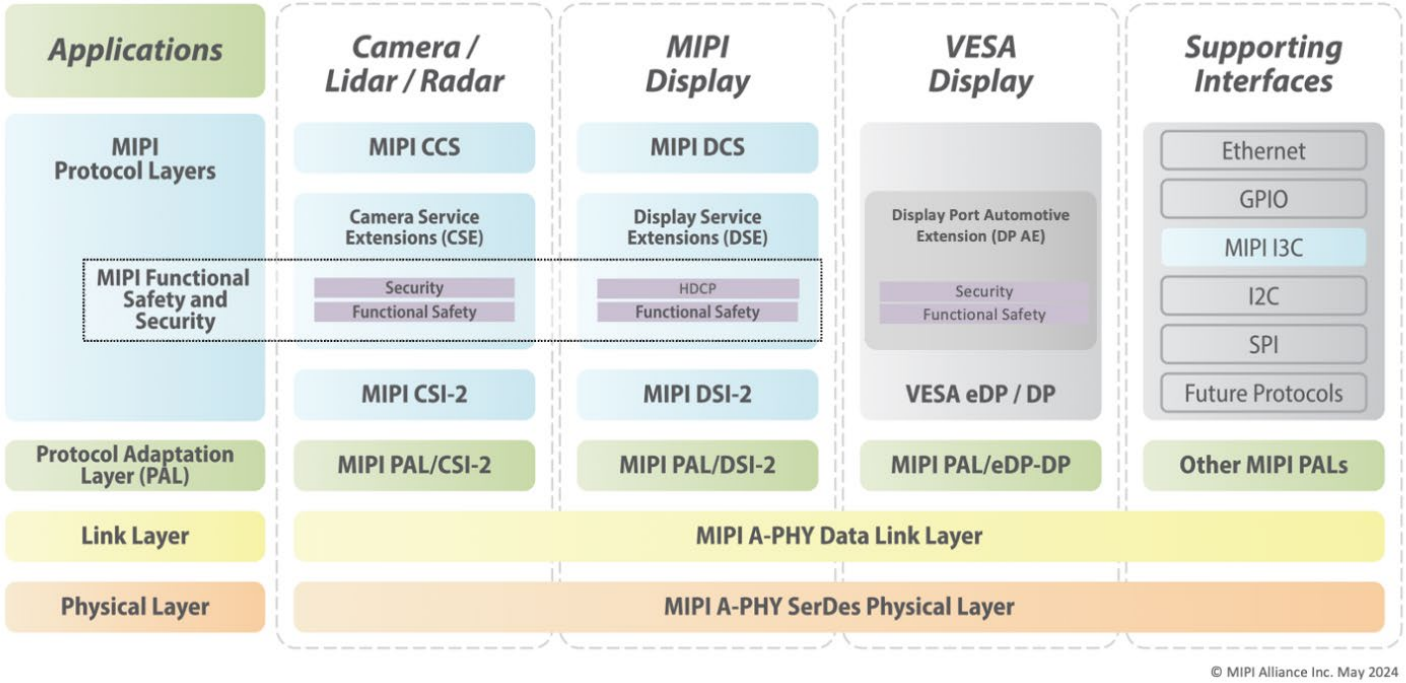
Key Takeaways

- Protocol level extension of DP 2.1 for the use of automotive display interface
  - Enablement with AES_SDP and extensive DPCD registers
- Features that facilitate the support of FuSa and security
  - ROI: region of interest
  - CRCs for Datapath, MSA, and SDP
  - Soft Fail/Hard Fail fault detection for robustness
  - SPDM-based device authentication
  - MACs for Datapath, MSA and Active Frame data
  - Automotive-grade encryption on control plane (DP AUX) and/or data plane (MSA, AES_SDP, active frame)
- Profiles 1-4 to accommodate various levels of FuSa and security requirements
- Use Superframe to simplify connectivity while maintaining the versatility of DP AE functions

Current Status and Timeline

- Spec:
  - 1.0 released in December 2023
  - 1.1 adoption vote: end of October 2025
- CTS:
  - First draft release: December 2025
  - TE implementation completion: end of March 2026
  - PlugFest to be held in Q1 or Q2 2026

As a Part of MIPI Automotive SerDes Solution (MASS) Ecosystem



MediaTek

Smarts and entertainment in auto innovation

Safe,
Secure,
Flexible ecosystem for automakers
to deliver powerful and connected automotive solutions

DP AE Capabilities:

- 8b/10b and 128b/132b coding
- SST/MST function
- Profiles 1~4
- Superframe
- Compatible with DP AE ver 1.1

MediaTek Development on VESA Automotive Extension

Spec collaboration

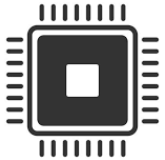
MediaTek aims to enhance the automotive application ecosystem by actively participating in spec development.

IP Simulation & Emulation

Pre-silicon development with SW simulation platform (VDK) and FPGA emulator.

CTS Verification

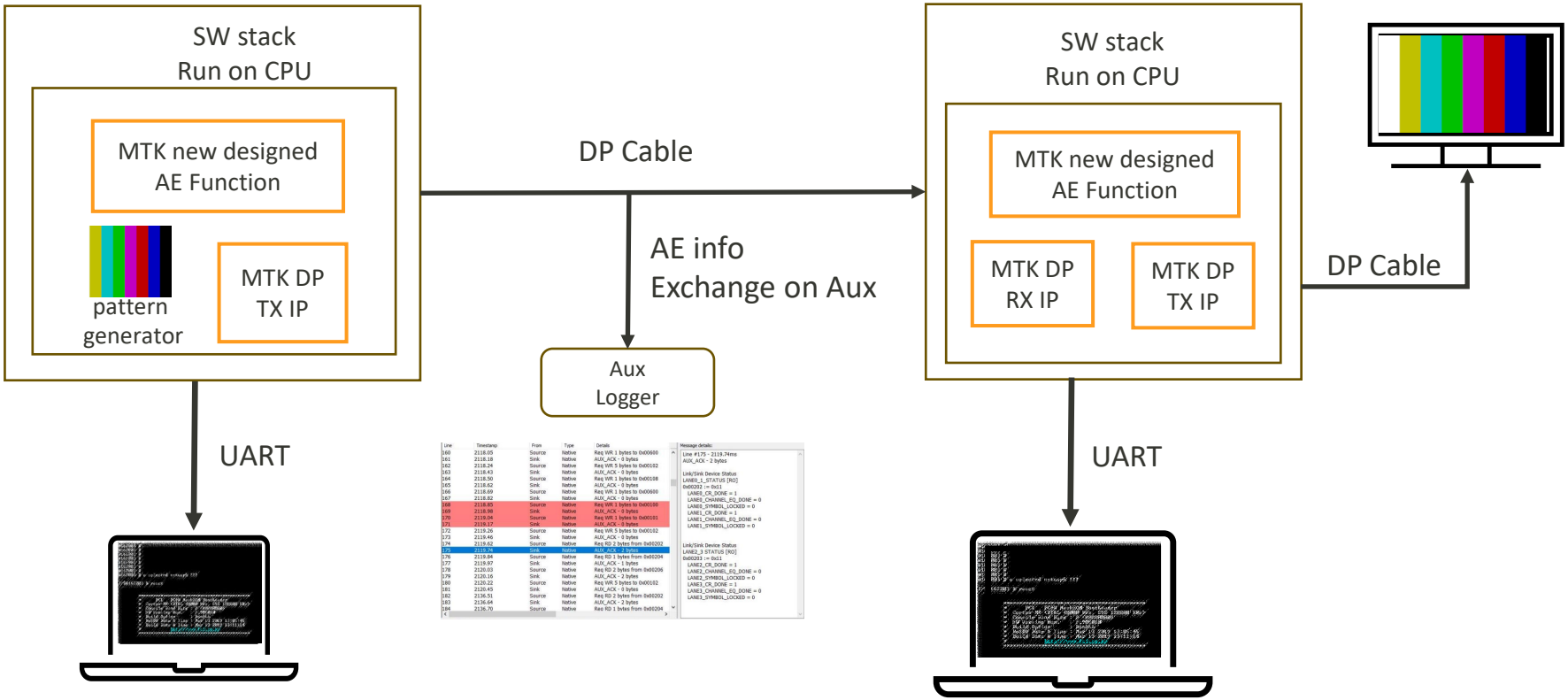
Utilize VESA's comprehensive CTS software model to pre-validate that the behavior of VESA AE IP complies with all specifications.



Design in Real Chip

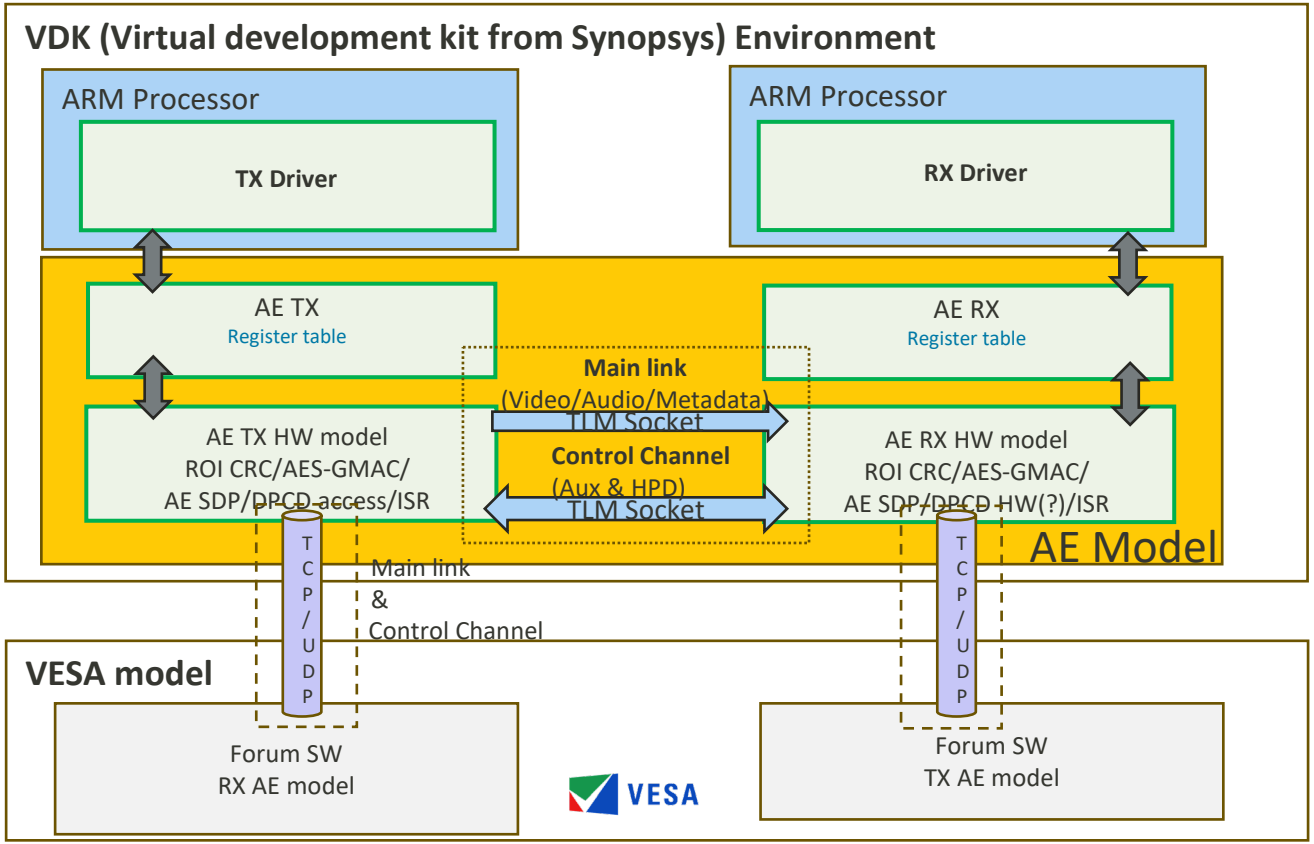
Integrate this comprehensive IP into the IC for future products to offer a complete solution.

MediaTek's VESA DP AE Development on FPGA



MediaTek Comprehensive Verification for VESA AE

VESA AE IP in VDK for SW flow and abstract HW behavior verification



DP LRD Active Cable Testing

Lexus Lee
Allion Labs,Inc
2025/10/17

Overview

- Why The LRD Active Cable development matters
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA DP8K(HBR3) Connector Certification Introduction

Overview

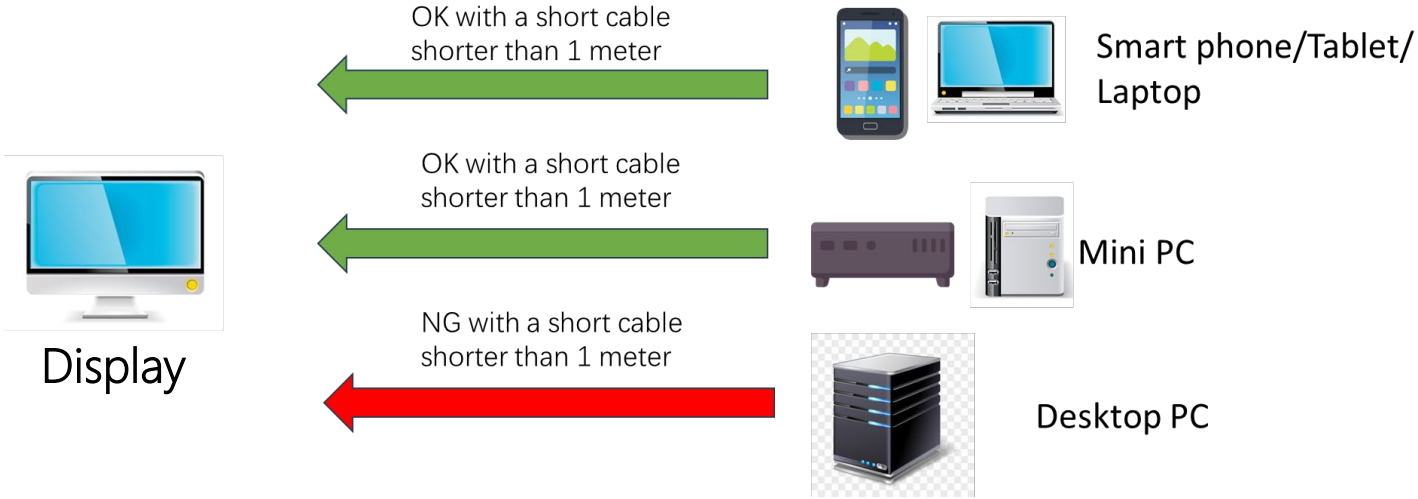
- Why The LRD Active Cable development matters
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA DP8K(HBR3) Connector Certification Introduction

The Current UHBR Passive Cable Status

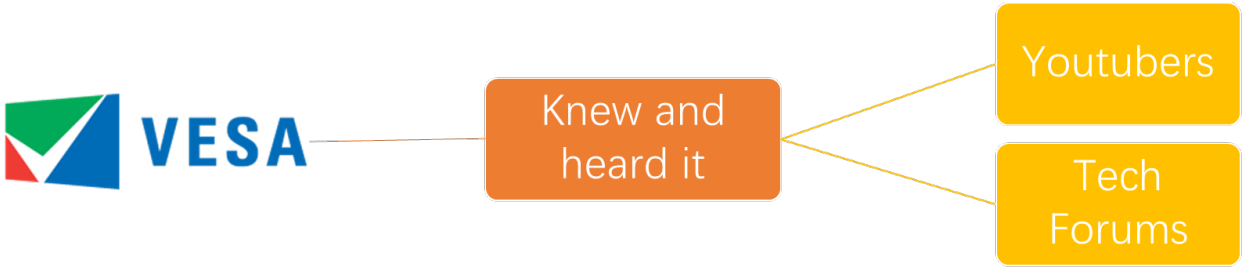
- DP to DP and USB-C to DP Passive cables for UHBR transmission
  - According to DP2.1a spec
    - UHBR 20-Capable Passive cable length: around 1 meter
    - UHBR 13.5-Capable Passive cable length: around 2 meters

- UHBR20 Passive cable in length: Not fitting all use-case

The Current UHBR Passive Cable Status Cont’



DisplayPort LRD Active Cable Solution



- VESA has brought us a solution to the criticism.
  - LRD Active Cable Solution
    - Get UHBR20 transmission to successfully work longer than 2 meter-long cable.
    - Creating a LRD Active Cable CTS

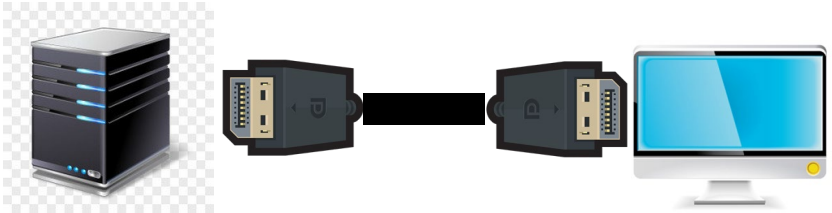
Overview

- Why The LRD Active Cable development matters
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA Legacy Connector Certification Update

CTS Testing Challenges

- Knowledge to get DP LRD cable to work up
  - AUX and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Aux P: Pull down to GND
2. Aux N: Pull high to 2.89~3.6V.
3. DP_PWR:2.89~3.6V
4. Aux transaction if needed

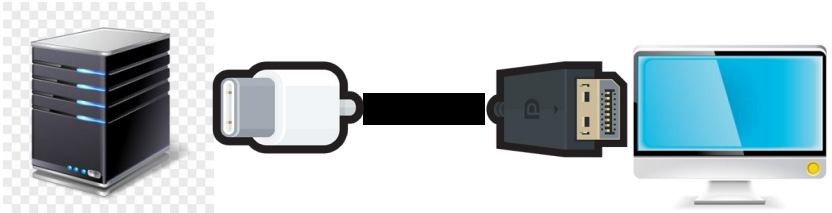


1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull high to 2.25~3.6V
5. Aux transaction if needed

CTS Testing Challenges Cont’

- Knowledge to get C to DP LRD cable to work up
  - Vconn, AUX, and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Vconn:3.0~5.5V
2. DP alt mode exerciser if needed.
3. Aux circuitry if needed.
4. Aux transaction if needed



1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull High to 2.25~3.6V
5. Aux transaction if needed

CTS Testing Challenges Cont’

- Power Consumption Check Before You Start Any Test
  - Do Link Training for
    - 1 Lane
    - 2 Lanes
    - 4 Lanes
  - Observe the current change of Vconn or DP PWR.
    - For example

	1 Lane	2 Lanes	4 Lanes
Current	80mA	170mA	380mA

CTS Testing Challenges Cont’

- Check How to Power up the LRD Cable Before You do Inrush Current Test
  - Supplying power to one end of a cable DUT ?
  - Supplying power to both ends of a cable DUT ?

	One End _Case	Both Ends_Case	Both Ends_but no power line used to connect the two LRD ICs.
Consuming Current	380 mA	190 mA	190mA

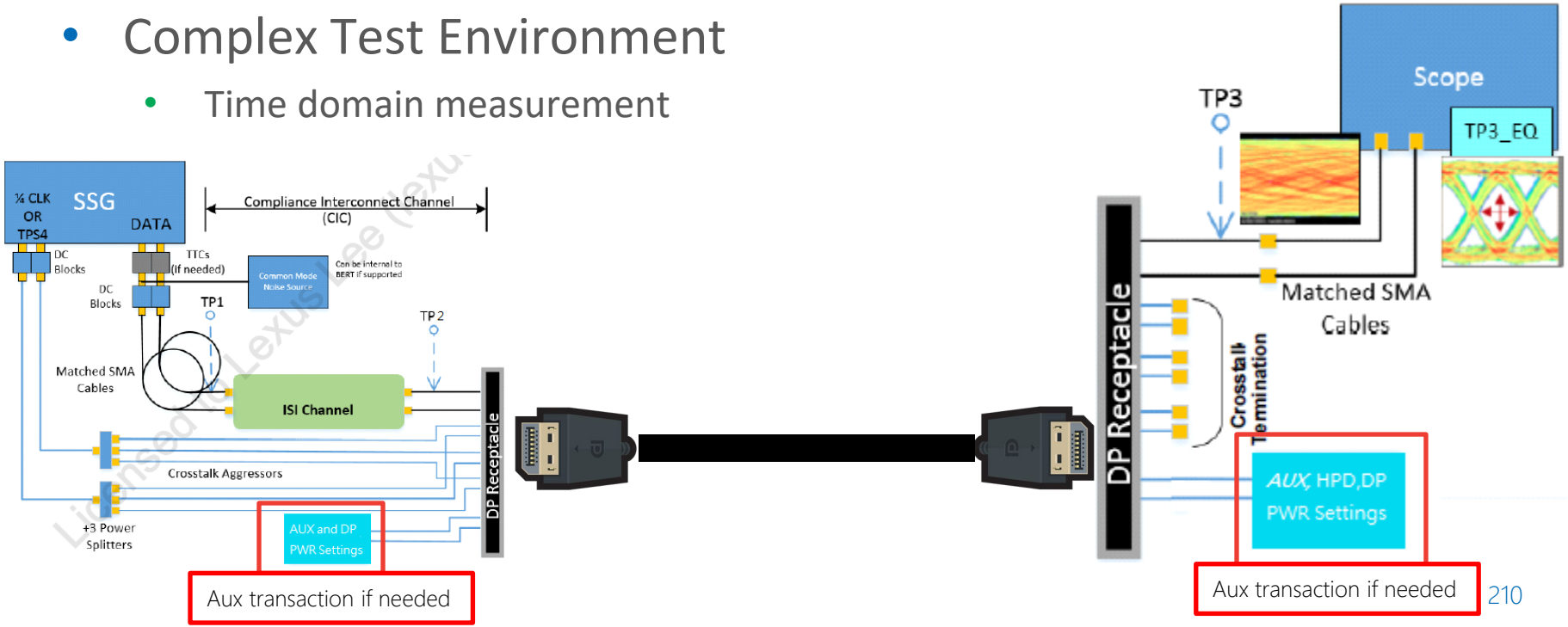
CTS Testing Challenges Cont’

- Why it matters
  - In order to get Maximum Inrush Current Energy

	One End _Case	Both Ends_Case	Both Ends_but no power line used to connect the two LRD ICs.
Measured Inrush Current Energy	4 mJ (wanted)	2 mJ (NOT wanted)	2 mJ (wanted)

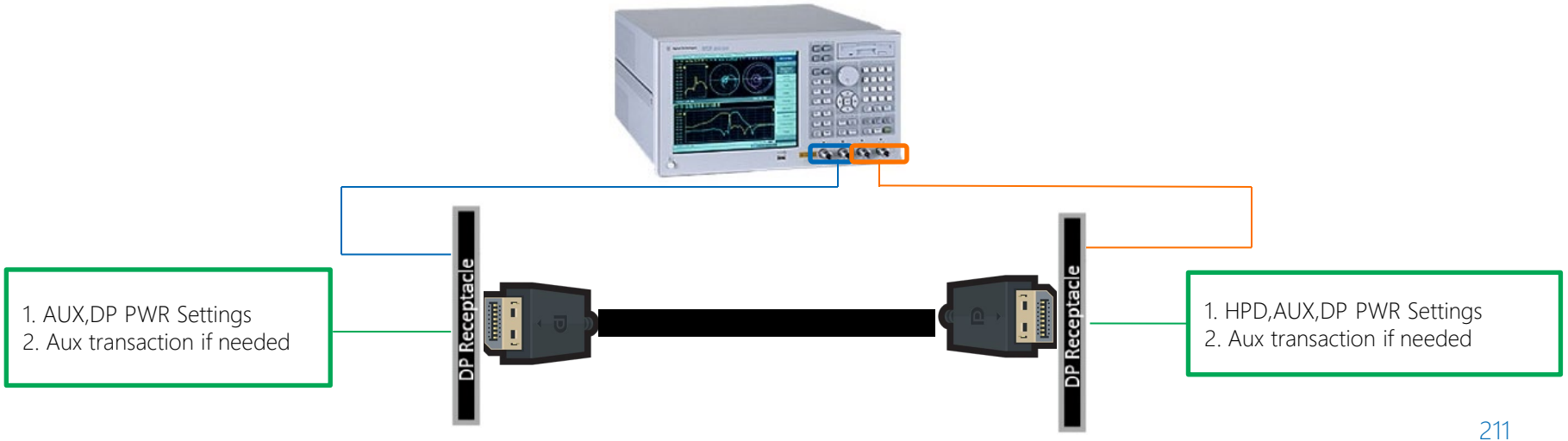
CTS Testing Challenges Cont’

- Complex Test Environment
  - Time domain measurement



CTS Testing Challenges Cont’

- Complex Test Environment
  - Frequency domain measurement

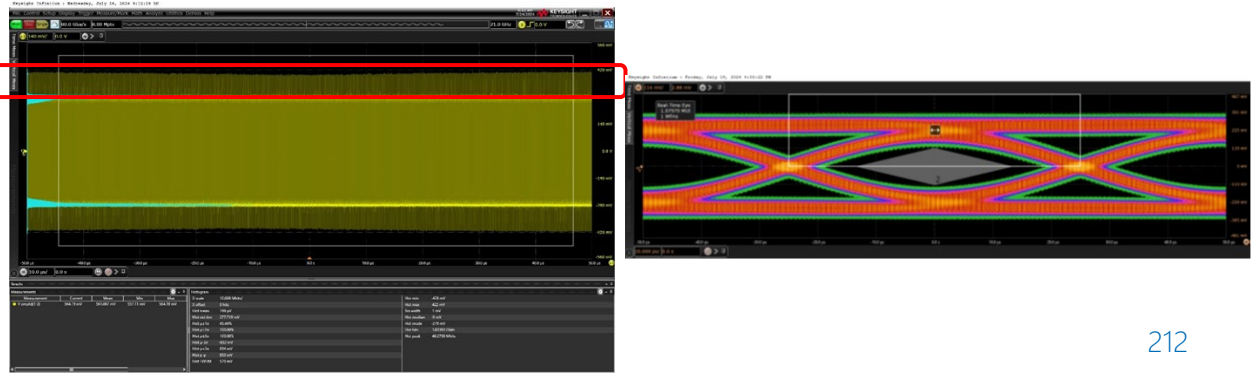


CTS Testing Challenges Cont’

- Stressed Signal Generator
  - Preset Calibration
    - Very important to stressed signal defined by DP spec.
    - Inaccurate preset number gets your stressed signal to highly not meet the expected ISI jitter, Eye Height, and Eye width.

Table 3-57: Preset FFE Coefficients[a] [b]

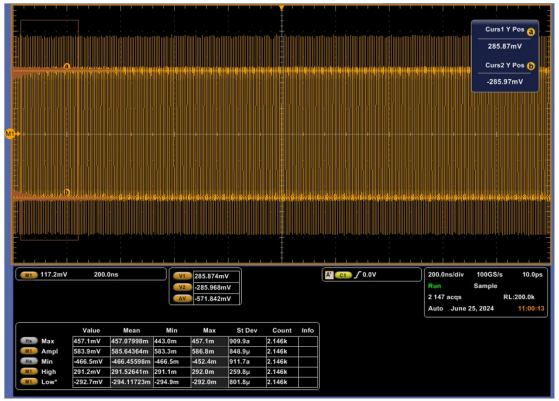
Preset Configuration #	Preshoot (dB)	De-emphasis (dB)	Informative Filter Coefficients		
			C_{-1}	C_0	C_{+1}
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0

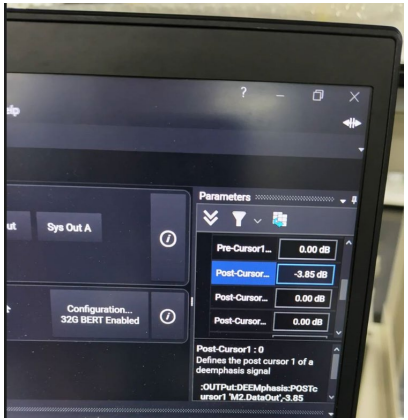


CTS Testing Challenges Cont’

- Stressed Signal Generator Cont’
  - Preset Calibration Cont’
    - Do not just enter the number that you want into your SSG FFE setting.

(SQ128) Rough De-emphasis: 20 log(585.6/923.4)=-3.95dB





Overview

- Why The LRD Active Cable development matters
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA Legacy Connector Certification Update

What Is Inside VESA LRD Cable CTS?

- Functional test
  - Successful Link Training
    - All data rate(from RBR to UHBR20)
    - All lane count (1-Lane, 2-Lane,4-Lane)
    - Bidirectional (Swap Sink/Source end)
    - Power management (Active Power ,Wake/Sleep, Aux-less ALPM)
    - USB-C Orientation (Flip/Normal)
  - SOP/SOP’ Response Check(SVDM2.0/SVDM2.1)

What Is Inside VESA LRD Cable CTS? Cont'

- Frequency Domain test
  - Insertion Loss Fit

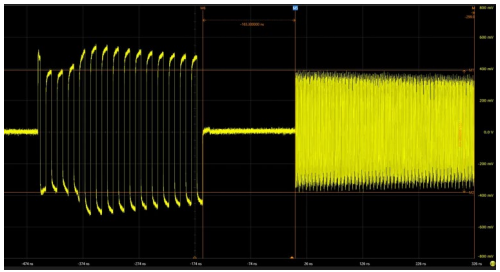
Table 4. Insertion Loss Fit Requirements

Frequency[1]	Insertion Loss Fit[2]	Description	Min	Max	Units
100MHz	*ILatDC*	Defining the ILfit mask for the cable response. Note: The main intention is to keep the cable with LPF characteristic similar to the passive cable.	DP80: -6 DP80LL and DP54: -5	0	dB
Nyquist	*ILFitatNq*		DP80: at 10GHz: -7.5 at 6.75GHz: -6.2 DP80LL: at 10GHz: -6.5 at 6.75GHz: -5.2 DP54: At 6.75GHz: -10.5 At 5GHz: -9	*ILatDC – 1.5*	dB
Nyquist x 1.25	*ILFitatf2*		*ILFitatNq - 3*	*ILFitatNq*	dB
Nyquist x 1.5	*ILFitatf3*		*ILFitatNq - 4*	*ILFitatf2*	dB
100MHz to Nyquist	*ILFitatWB*	Max gain of the cable in the range of DC to Nyquist Frequency		0	dB

What Is Inside VESA LRD Cable CTS? Cont'

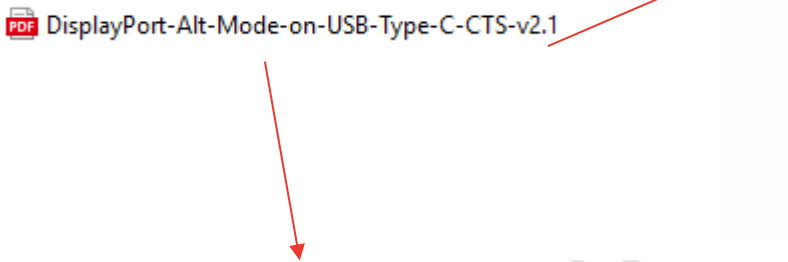
- Time Domain test
  - Eye Diagram
  - Instantaneous Common Mode Voltage
  - CONFIG2 Voltage and No DP_PWR thru Cable
  - AUX-Less ALPM
  - LOS Test
  - Inrush Current Test
  - AUX Voltage Clamping
  - Preset Distortion Thru the cable

CTS D5 version→ Final version



What Is Inside VESA LRD Cable CTS? Cont'

- Additional Tests Added for USB-C to DP LRD Active Cable
  - From DP Alt Mode 2.1 CTS



10.6

DisplayPort Alternate USB-C to DP Adapter Tests 141
10.6.1 DP Connector Attached to DP Sink 141
10.6.2 DP Connector Attached to DP Source 142

9.5

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9.5.1.2 Test Setup 56
9.5.1.3 Initial Conditions 56
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10.4

DisplayPort Alternate Mode on USB Type-C Tests for Cables 131
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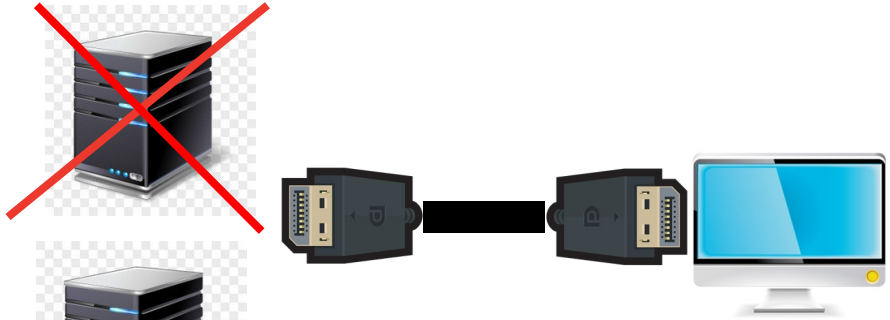
10.4.2 SOP' (SOP") DisplayPort Configurations and Exit Mode 133
10.4.3 DPAM Version 2.1 Cable Connected to DPAM Version 2.0 or 2.1 DFP_U 134

Most Failed Items Sharing

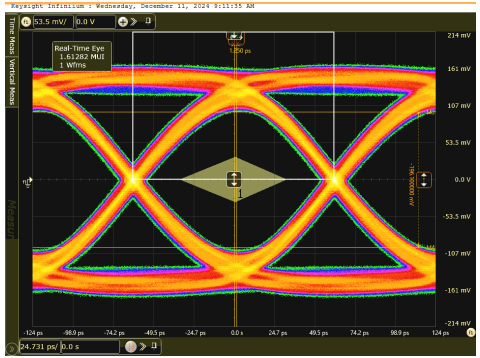
- Inrush Current
  - Criteria
    - ResultantENERGY_POWER_CONSUMER < 0.07mJ
    - ResultantPEAK_CURRENT_POWER_CONSUMER <= 13.5A
  - Inactive mode
    - No data running over Main Link
      - Nobody fails (All Pass)
  - Active mode
    - Data running over Main Link is on
      - Some cables failed



Most Failed Items Sharing

- Eye Diagram
  - UHBR20 Criteria
    - TP3_EQ-Inner Eye Height: 100mV
    - TP3_EQ-Eye Width: 560mUI
    - Cannot hit the eye mask
  - Requirement: Need to pass with 3 TxFFE Presets and average of 5 times.

Preset Configuration #	Preshoot (dB)	De-emphasis (dB)
0	0	0
1	0	-1.9
2	0	-3.6
3	0	-5.0
4	0	-8.4
5	0.9	0
6	1.1	-1.9
7	1.4	-3.8
8	1.7	-5.8
9	2.1	-8.0
10	1.7	0
11	2.2	-2.2
12	2.5	-3.6
13	3.4	-6.7
14	3.6	0
15	1.7	-1.7



  - Caused by Raw cable material quality and cable vendor manufacturing capability

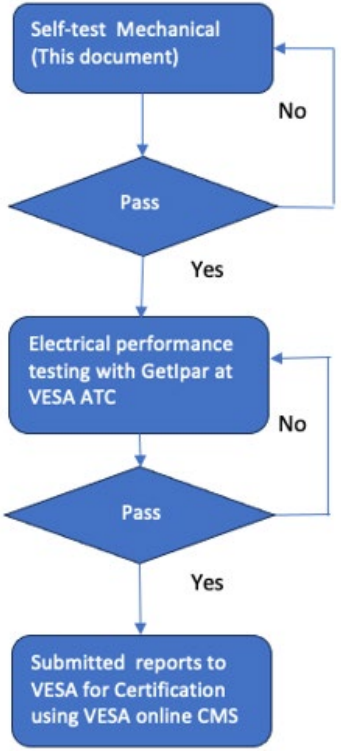
Overview

- Why The LRD Active Cable development matters
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA DP8K(HBR3) Connector Certification Introduction

DP Connector Certification Status

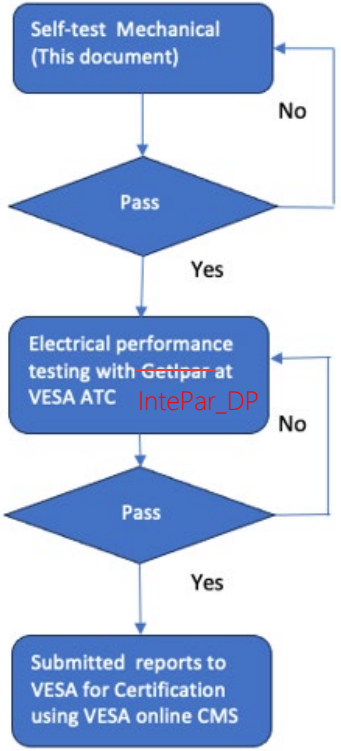
- Connector certification
  - Legacy connector(HBR2 and below)
    - Self-test Mechanical only
  - Enhanced Connector(UHBR13.5 and UHBR20)
    - Self-test Mechanical
    - ATC test Electrical Performance

VESA® DisplayPort™ Self-Test Report for Connectors v2.1



DP Connector Certification Status Cont'

- New, This Year
  - DP8K(HBR3) Connector Certification
    - Self-test Mechanical
    - ATC test Electrical Performance



VESA® DisplayPort™ Self-Test Report for DP Connectors Supporting HBR3 Link Rate and DP8K Cables

Thank you

VESA Compliance Program

Compliance Test Specification Updates

VESA has updated base specification and all CTS documents in past two years

- DP 2.1a Spec update – released 12/2023
- DP 2.1 PHY CTS v1.0 – released 6/23
- DP 2.1 Link CTS v1.1 – under final review, release by EOY
- Enhanced DP Connector Self-Test v2.1 – 8/2024
- DP Alt Mode CTS v2.1 – under final review, release by EOY
- Embedded DP (eDP) – 9/2024

Product certifications* 2023/2024/2025

Products	2023	2024	2025
DP Sources	99	93	133
DP Sinks	277	491	411
DP Cables	59	70	49
DisplayHDR	397	556	560
ClearMR	45	53	69
AdaptiveSync	80	75	105

*Note: Numbers are base model certs not including family models. Updates to CMS system will include feature to count family models in the future.

VESA PlugTest Events

- Provide significant value to VESA compliance program and member companies, particularly as new capabilities and products are deployed.
- Demonstrate and improve traditional interoperability
- Test Native DP and DP Alt Mode over USB Type-C™ products
  - UHBR rates, DSC, New MST Link Layer Tests, FEC, DisplayHDR and other new capabilities
  - Verify Test Equipment Correlation
- VESA hosted two successful PlugTests in 2024 (Taiwan and US)
- VESA hosts two PlugTests in 2025
  - South San Francisco, CA USA: **Q1 2025 (completed)**
  - Taipei, Taiwan: **Q4 2025 (Oct 20-23rd Taiwan)**

Summary

Summary

- Product shipments and certifications on based on VESA technologies continue to grow
- DP 2.1 UHBR capable product development and certifications ramped up 2024 and continue to increase in 2025
- VESA Enhanced cable and connector certification programs have been very successful with significant numbers of Enhanced Connectors and DP54, DP80 and DP80LL cables certified
- DisplayPort over USB-C is a game changer for small form factor and portable products and is now the defacto standard for laptops, tablets and handheld devices
- Display Performance Standards adoption and certification have been extremely successful since introduction
- Development and adoption of new technologies continues to drive increases in VESA membership growth

Questions?

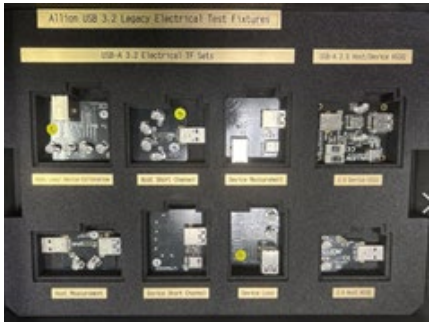
VESA

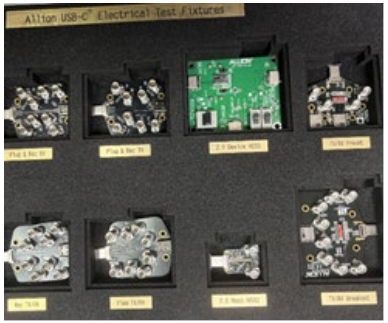
Demo Tables

Allion Demo Table

- Test Fixtures
  - Designed for USB-C to (m)DP Cable Compliance Testing
  - Designed for USB 3.2 & USB-C Compliance Testing

- Brochures
  - PCIe 6.0 Test Fixture
  - USB 3.2 Test Fixture
  - DP/HDMI Test Fixture
  - C to DP/mDP Cable Test Fixture





Teledyne LeCroy
Test Solutions for DisplayPort v2.1

M42de 80G Video Analyzer/ Generator

TELEDYNE LECROY
Everywhereyoulook™

Teledyne LeCroy
7F., No. 667, Bannan Rd
Zhonghe Dist, New Taipei City 235
Taiwan
Phone: +886-2-8228-6100

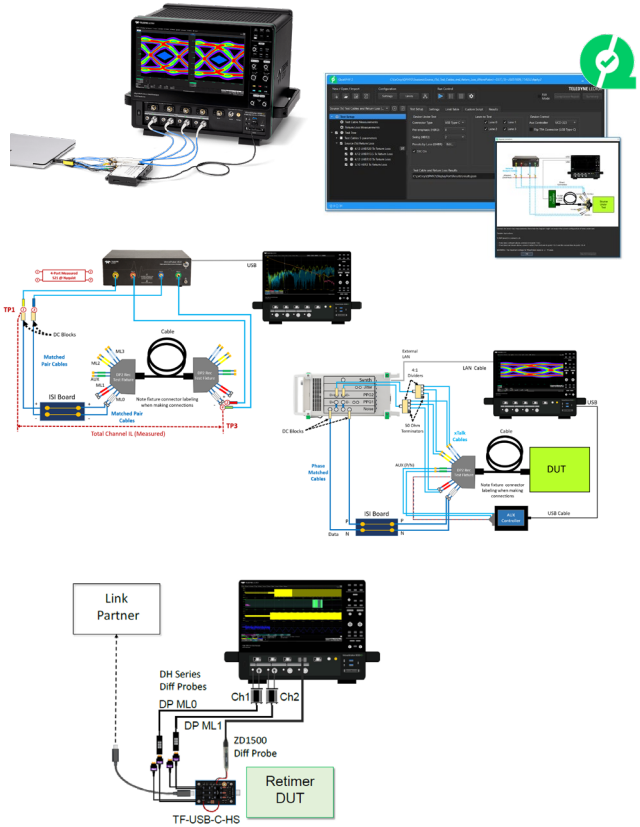
protocolsales@teledynelecroy.com

Teledyne LeCroy DisplayPort Test Platforms

- **Quantumdata M42de Analyzer / Generator**
  - DisplayPort 1.4 & 2.1 (UHBR) Lane Rates
  - DP80 and USB Type-C® connectors
  - Deep Capture / Analysis
  - T.A.P.4™ Passive Monitoring
  - Comprehensive DP 1.4 & 2.1 Compliance Coverage
    - Link, DSC, LTTPR, EDID & MST
  - qdPrime™ Automated Test Suite

- **Quantumdata M21 Analyzer**
  - Portable DP Analyzer & HDMI Analyzer / Generator
  - DisplayPort Source Testing only (up to UHBR 13.5Gb/s)
  - AUX Channel Monitoring

DisplayPort 2.1 PHY Compliance and PHY-Logic Debug

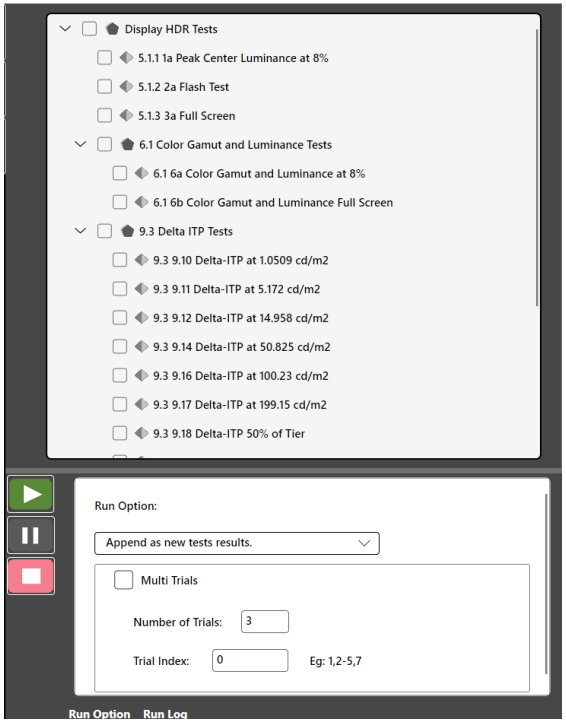


- DisplayPort 2.1 Source (Tx) Compliance
  - WaveMaster/SDA 8000HD with QualiPHY® 2 software
  - SDAX-DP expert analysis – Find Best CTLE/DFE
  - Reduced test times with QPHY2-PC
  - Automated Return Loss with WavePulser 40iX
- DisplayPort 2.1 Sink (Rx) Compliance
  - WaveMaster/SDA 8000HD with QualiPHY 2 software
  - SSG Cal and BER testing using Anritsu MP1900 SQA
  - Automated Channel Cal with WavePulser 40iX
- PHY-Logic (Interop) Debug
  - AUX Triggered + Main Link capture
  - TF-USB-C-HS – probing access
  - DP-AUX, USB-PD TDMP software
  - Clock switch testing on live link

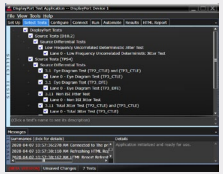
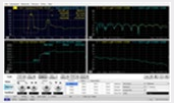
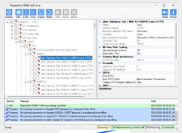
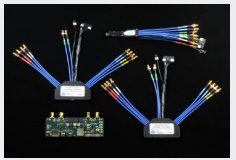
DisplayHDR Compliance Automation Test Application

- Support All DisplayHDR Tier
- A fully automated platform that executes VESA DisplayHDR Compliance test sequences
- Reducing human error and ensuring every product meets the strictest HDR performance standards.
- Automatically generate report, and then convert result into VESA excel sheet. (VESA HDR Measurement Result_1.2)

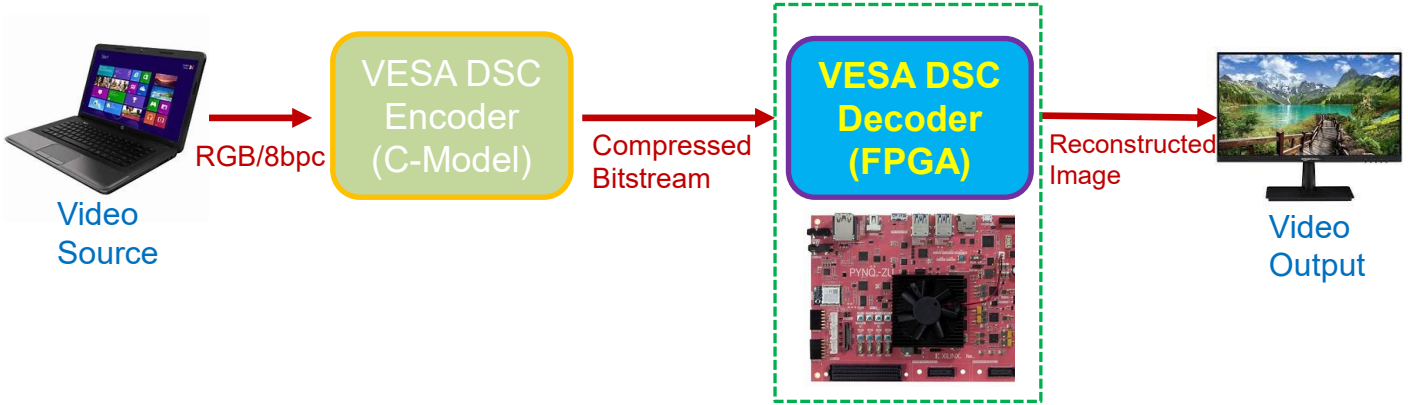
labs-insight.com



Keysight DisplayPort Solutions

	Source	Interconnects	Sink
Test Automation Software	 **D9040DPPC** **D9042DPPC** **D9040EDPV** Automated TX tests Compliance Debug & Characterization Automation via AUX channel	 S94DPPCB DisplayPort Cable Test SW	 BitifEye Digital Test Solutions **N5992DP2A** Accurate RX calibration Automated RX tests Compliance Debug & Characterization Automation via AUX channel
Instruments	 **UXR** Lowest noise Accurate measurements Channel (de-)embedding CDR, Equalization Eye/Jitter analysis	 **E5080B** Network Analyzer	 **M8050A** Best signal integrity Lowest noise Equalization, RJ, PJ, CMI Test patterns
Accessories	 **UCD-323 Gen2** **DPR-100** Reference Sink **N7015A/18A** Type-C test fixture 	 Luxshare ICT Cable test fixtures  Modular Switch Matrix	  **UCD-323 Gen2** **DPT-200** Reference Source

Cybertek VESA DSC Decoder IP Core Demo



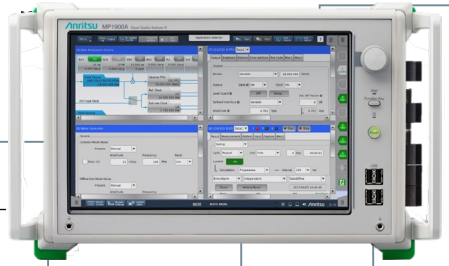
DSC Decoder IP Core Feature

- ✓ Compliant with VESA DSC 1.2a and 1.2b standards
- ✓ Support MMAP, BP, MPP and ICH encoding mechanisms
- ✓ YCbCr and RGB video input format
- ✓ 4:4:4, 4:2:2, and 4:2:0 native coding
- ✓ Support 8/10/12 bits per component
- ✓ Support 3 pixels per clock decoding
- ✓ Configurable features for gate count and speed

CYBERTEK SOLUTION

MP1900A Signal Quality Analyzer
High Speed Bus SINK Compliance Solution

MP1900A Standalone
Multi-channel BER Measurement
High-quality PPG
High-input-sensitivity ED
PAM3/4 BER Measurements



Jitter Tolerance Test
SJ/RJ/BUJ Injection
Low-rate estimated BER measurement

Thunderbolt
4/5&DP1.4/2.1 Rx Test
Stressed Signal Calibration and
Stressed Signal Input Test

USB Link Sequence Generation
Transition to Loopback mode

Stressed Signal Calibration
PCI Express Link Sequence Generation
Transition to Loopback Mode
Pass/Fail evaluation using BER measurement

Calibration of stressed signal* → **Transition DUT state to Loopback** → **Stressed Receiver Testing**

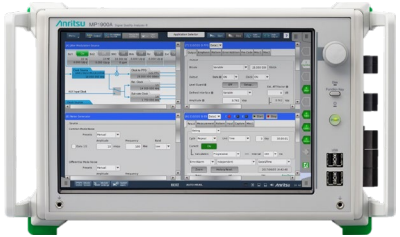
MX183000A Software

Stressed Signal Calibration*	USB Link Sequence Generation Function PCI Express Link Sequence Generation Function	Stressed Signal Input Test Function Jitter Tolerance Test Auto-receiver Test Function

MP1800A Hardware

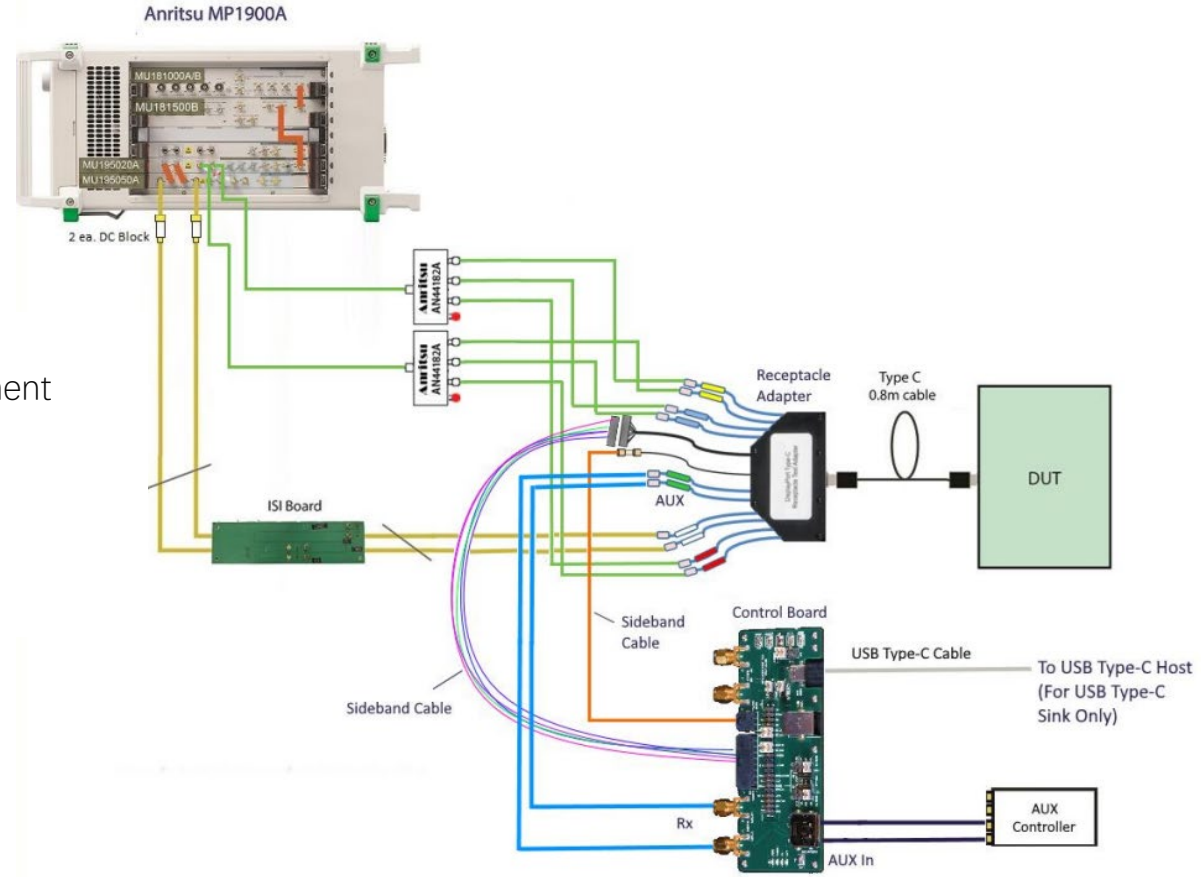
Up to 32 Gbit/s, 8ch	High Quality Signal	Jitter Emphasis

MP1900A Signal Quality Analyzer
DP1.4/2.1 SINK Compliance Test Structure



MP1900A Standalone

- Multi-channel BER Measurement
- High-quality PPG
- High-input-sensitivity ED
- PAM3/4 BER Measurements
- DP1.4/2.1 and USB4v1&v2 Compliance test Support



UNIGRAF

DisplayPort

USB Type-C

sales.asia@unigraf.fi

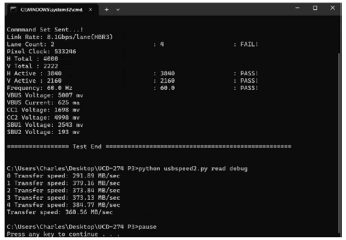
Unigraf DisplayPort and USB-C Test Solutions

UCD-500 Gen2

16K DP 2.1 Generator & Analyzer

- DP 2.1 Link Layer CTS Tool
- DP 2.1 Sinks and Sources up to 8K@60Hz (UHBR 20Gbps / Lane) and 16K@60Hz with DSC
- Featuring Link Analyzer, Panel Replay and eDP test functions

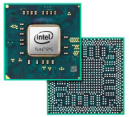
UTC-274



USB-C Test Automation Tool

- Test DP Alt Mode, Power Delivery and USB Speed
- Support EPR function up to 240W Source and Sink
- Test USB-C connector pins soldering and assembly quality with a single cable insertion

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DisplayPort Alt Mode Compliance Testing and Analysis solutions

SYMBIOSYS ALLIANCE

Ellisys USB/DPAM Test and Analysis Solutions

USB Explorer™ 350

Multi-function USB Type-C®, USB 3.2, and Power Delivery Protocol Test Platform

VESA-Approved Tester for DisplayPort ALT Mode

Type-C Tracker™

Protocol and Electrical Analysis Tool for USB Type-C® Standards

Includes DP AUX and DP ALT Support

ellisys
Better Analysis

GRL
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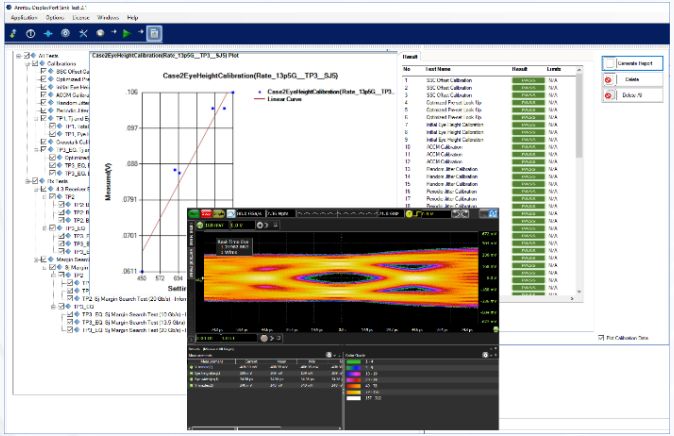
GRL DisplayPort

DP2.1 Tx PHY Test Solution
DP2.1 Rx PHY Test Solution
DPAM Test Solution

GRL Test Solution

DisplayPort 2.1 Tx/Rx Test Automation Solution



USB Type-C® Power Delivery Tester & Analyzer - EPR

The only instrument you need for validating compliance, inter-operability, and reliability of your designs

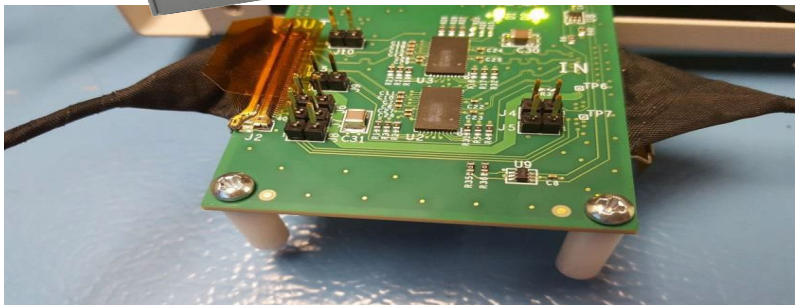
- USB Power Delivery Specification 3.2
- Type-C ® Functional Specification
- IEC Functional Safety (IEC 62368-1)
- **DisplayPort™ Alternate Mode Tests**
- Thunderbolt 3/4/5 Alternate Mode Tests
- Thunderbolt 3/4/5 Power Tests
- Qualcomm® Quick Charge 2™
- Qualcomm® Quick Charge 3™ and 3+™
- Qualcomm® Quick Charge 4™ and 4+™
- Qualcomm® Quick Charge 5™
- BC 1.2 for QC Sink products
- IEC 63680-1-2

eDP and DisplayPort Protocol Analysis and Validation Real Time *ANY* Source to *ANY* Sink

FuturePlus Systems
Advancing Technology Development

NEW NEW

USB-C Power Delivery Analysis Software for DisplayPort Ask for a Demo!



eDP 1.4b and 1.5a, DP2.1
USB-C and DisplayPort Probes
UHBR10, UHBR13.5
Up to 4 Lanes
Single Stream Transport and Multi-Stream Transport
and more....

Something Special? We Like Challenges!

Thank you for attending the VESA Workshop Taipei, Taiwan 2025