VESA 2026 Seoul Workshop

October 12, 2026

Agenda

Time	Topic	Speaker
9:00am	Registration Opens	N/A
9:30am – 10:00am	Snacks & Refreshments	N/A
10:00am – 10:30am	VESA Overview and Standards Updates, Including DisplayPort v 2.1b	Jim Choate, Compliance Manager, VESA
10:30am – 11:00am	DisplayPort Link Layer CTS v 2.1 MST Updates and Automotive Extension Services Updates	Neal Kendall, Senior Staff Product Marketing Manager, Teledyne LeCroy
11:00am – 11:30pm	DP v 2.1 PHY CTS Overview and Updates	Mike Engbretson, Product Manager, Teledyne LeCroy
11:30am – 12:00pm	VESA DisplayHDR & Adaptive-Sync Display CTS	SeungHyun Yoo, Wired Interface/Connectivity Standard Engineer, LG Electronics
12:00pm – 1:00pm	Lunch	N/A
1:00pm – 1:30pm	Changes to VESA Standards for High-Frame-Rate Display	Do Kyun Kim, Wired Interface/Connectivity Standard Project Leader, LG Electronics
1:30pm – 2:00pm	LRD/Active Cable Testing and DP 2.1 Enhanced Connector Certification Challenges	Jim Choate, Compliance Manager, VESA
2:00pm – 2:45pm	Design Considerations for USB-C Products	Abel Astley, Head of USB Technology, Unigraf Oy
2:45pm – 3:15pm	Break	N/A
3:15pm – 3:45pm	VESA Compliance Program	Jim Choate, Compliance Manager, VESA
3:45pm – 4:00pm	Summary, Questions & Answers	Jim Choate, Compliance Manager, VESA
4:00pm – 4:30pm	Demo Stations Overview	N/A

VESA Overview and Standards Updates

Jim Choate
VESA Compliance Program Manager
October 12, 2026

Agenda

- VESA Overview
- DisplayPort Overview
- VESA Technology Development Areas
- Summary

VESA OVERVIEW

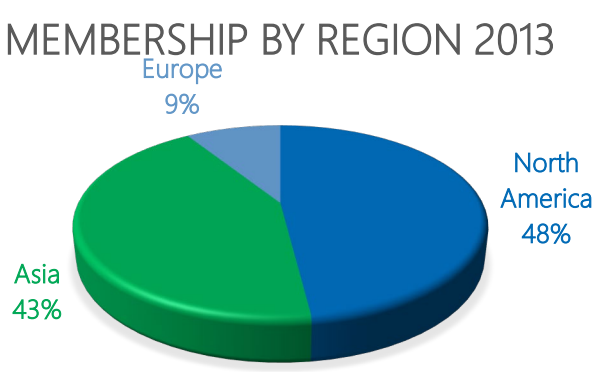
VESA Vision

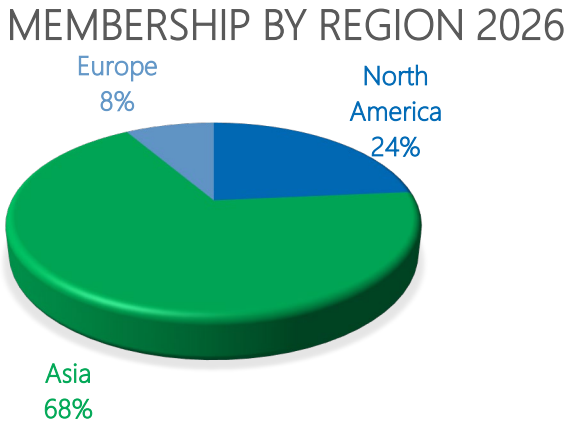
- VESA's vision is continual growth in technical standards development and evolution as an international trade association, with a worldwide membership driving standards initiatives, product implementations, and market implementation.

About VESA

- A growing global industry alliance with 369 members. Continuous growth in membership.
- Mission to develop, promote and support ecosystem of vendors and ***certified*** interoperable products for the electronics industry.
- *Develops OPEN standards, contribution is open to all companies at all stages of development*

VESA Membership Growth by %

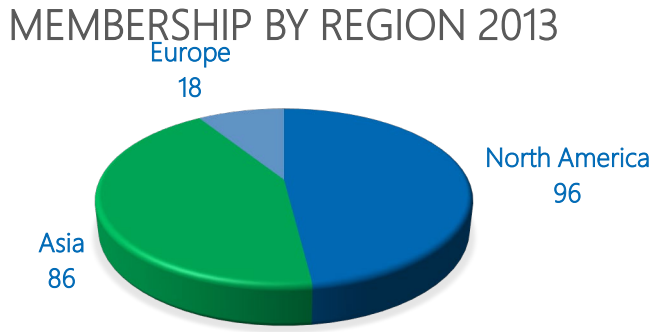


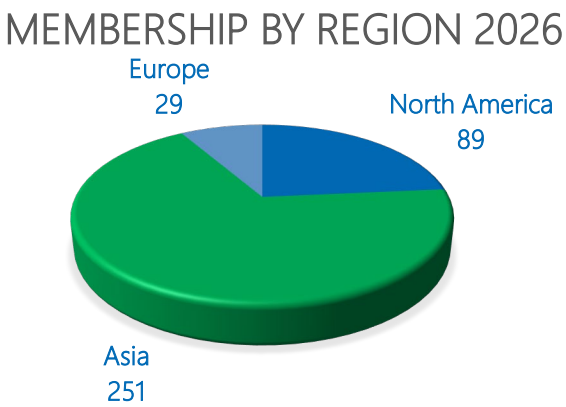


- **Total Ecosystem:** 200 total corporate members worldwide.
- **Western Core:** North American companies hold the largest single regional share.
- **Balanced Footprint:** Early-stage adoption driven primarily by foundational US chipmakers and device OEMs.

- **Total Ecosystem:** Expanded to 369 total corporate members.
- **Epicenter Shift:** Asian tech hubs now represent over two-thirds of the standards body.
- **Global Standard:** Widespread international integration driven by the ubiquity of DisplayPort, DPAM, eDP, Display Panel Metrics (DPM)) and automotive display profiles.

VESA Membership Growth by Total Companies





- **The Illusion of Decline:** A percentage-only view falsely suggests North American membership shrank by half (48% down to 24%).
- **The Reality of Stability:** In absolute numbers, North American membership stayed completely robust and stable (89 vs 96 companies). Europe membership has grown 61% in this interval.
- **The Growth Engine:** The structural shift is entirely additive—fueled by **165 new Asian companies** joining the ecosystem to support massive display infrastructure expansion.

VESA Standards Enable Many Market Segments…



Monitors, PCs and laptops



Gaming consoles and headsets



Smartphones and tablets



Automotive



Multi-Stream Transport (MST)

NEW: VESA DP AE specification and DP AE CTS

VESA Local Asian Support Capability

- VESA continues to provide local support to Asia to address growing regional membership needs
- **Kellen** is VESA's Representative in Asia
- This partnership provide members with a communication option in their native language. Kellen handles membership related activities including, new membership requests, renewals, event support and translation of VESA member messaging, etc.
- AsiaVESA@kellencompany.com or at +86 10 6580 0670

DisplayPort ™ Overview

DisplayPort Market Penetration

- DisplayPort adoption continues to grow in 2026
- DisplayPort and DisplayPort Alternate Mode over USB-C
  - The common monitor interface for personal computers
  - Supported on the USB-C interfaces
    - Mandated for USB4 and Thunderbolt
  - Automotive integration with DP AE specification
  - Mobile phones with USB-C
  - ***New:*** *AR/VR standard and CTS*
- Embedded DisplayPort (eDP)
  - >95% to near 100% penetration in notebook PCs, used in many high-end tablets and automotive

DisplayPort 2.1b Summary

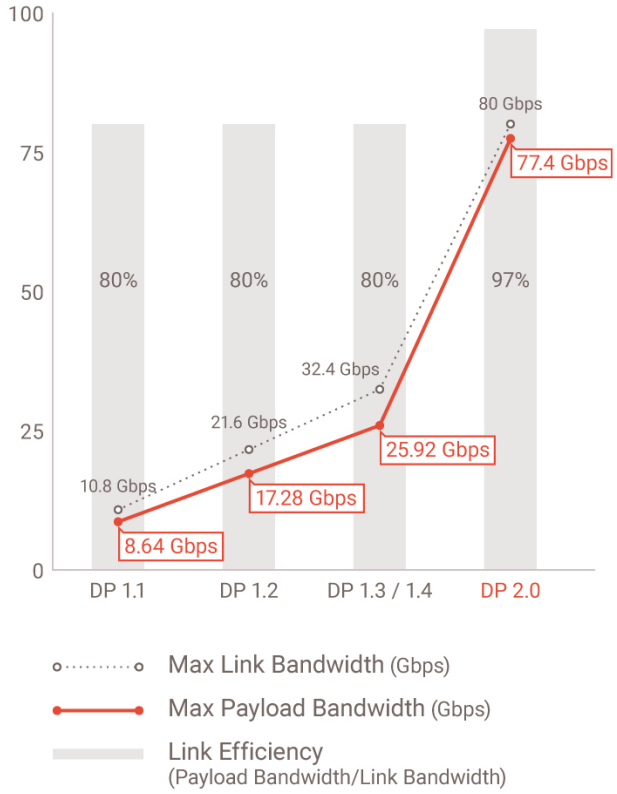
- DisplayPort v2.1b was released in December 2025
- Major features added in v2.0/v2.1/v2.1a/v2.1b:
  - Added 128b/132b DP channel coding (UHBR rates)
  - Increase in data bandwidth performance (almost 3X) with new link rates up to 20 Gbps/lane
  - Panel Replay, similar to PSR (Panel Self Refresh) used for eDP
  - DSC support mandated
  - Enhanced DP connectors and cables (DP40, DP54 and DP80)
  - DP PHY specification alignment with USB4 PHY specification
  - Updated DP to HDMI v2.1 or higher protocol converter (PCON)
  - Corrects errata
  - Replaces DP40 cables with DP54 to expand higher rate cable length
  - Expanded Tunneling capability
  - Updates for DP AE Services specification
  - DP80LL cable spec section (active cables for longer reach with lower loss)
  - LRD Active Cable Electrical Mandate section

VESA

- DisplayPort 2.1b enables up to 3X increase in video bandwidth performance vs DP 1.4
- UHBR10, UHBR13.5 and UHBR20 provides up to 80Gbps link bandwidth for 4 lanes at 20Gbps.
- First standard to support 8K resolution (7680 x 4320) at 60 Hz refresh rate with full-color 4:4:4 resolution, including with 30 bits per pixel (bpp) for HDR-10 support
- Beyond 8K resolutions achieved with maximum link rate to up to 20 Gbps/lane and more efficient 128b/132b channel coding

DisplayPort™

EVOLUTION OF DISPLAYPORT DATA BANDWIDTH



DisplayPort 2.1 Link Layer CTS Summary

- DP 2.1 LL CTS v1.1 released 12/2025
- Major updates:
  - Updates to align with other published VESA standards and terminology
  - Incorporated many approved and published SCRs
    - For example: FEC, Audio, DisplayID, min Hblank/Vblank, etc
  - Addition of new Source, Sink and Branch device MST tests (covered separately)
  - LTTPR emulation testing

VESA Technology Development Areas

VESA technology development

VESA members are collaborating on several key technology areas

- Embedded DisplayPort - v2.0 (published Sept 2024)
- DP Tunneling over USB4 – compliance testing has begun
- AR/VR Task Group
  - Focused on creating solutions roadmap to meet performance, power and implementation requirements for future AR/VR needs. Specification is released. Work on CTS underway
- DP Automotive Extension Task Group
  - Working with automotive industry to address needs for high-resolution performance in this market segment
  - Working on DP AE CTS and testing
- MST Compliance Test Updates
  - DP 2.1 LL CTS v1.1 released and new tests became normative 7/7/2029
- Display Performance Metrics Task Group
  - DisplayHDR, ClearMR, AdaptiveSync updates and proposals for future capabilities

VESA Logos and Marketing Guidelines

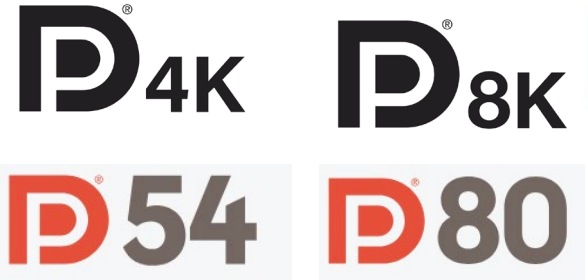
VESA Membership Allows Use of VESA Logos

- When your product passes certification company can use VESA logo to show customers proof of quality

Cable Logos include:

DP Product Logos include:

Display Logos include:



VESA DisplayPort MST CTS 改进

Alok Soni/Neal Kendall

Teledyne LeCroy

2026 년 10 월 12 일 – 서울, 대한민국

MST Source CTS Updates Since CTS Rev 1.1

- **Agenda**
  - Overview of CTS updates since Rev 1.1
  - MST Source CTS updates
  - MST Branch CTS updates
  - Composite Sink CTS updates
  - New Sink and Source tests
  - Summary
  - Q/A and feedback

MST 소스 CTS 버전 1.1 이후 CTS 업데이트

- **의제.**
  - 1.1 버전 이후 CTS 업데이트 개요
  - MST 출처 CTS 업데이트
  - MST 지부 CTS 업데이트
  - 복합 후이 CTS 업데이트
  - 새로운 피드인 및 소스 테스트
  - 초록
  - Q&A 및 피드백

MST Source CTS updates since CTS Rev 1.1

MST 소스 CTS 업데이트 CTS Rev 1.1 이후

MST CTS Coverage Summary

Area	Rev 1.1 Tests	New Tests	Updated Tests
Source	21	0	4
Branch	54	2	15
Composite Sink	48	1	14

MST CTS 보도 요약

면적	1.1 버전 테스트	새로운 시험	테스트 업데이트
출처	21	0	4
지선	54	2	15
복합 싱크대	48	1	14

CTS Updates - MST Source Device

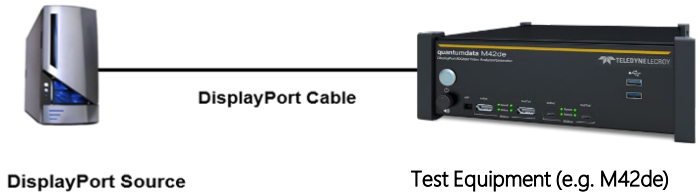
- MST Source Tests in Rev 1.1 CTS (21 Tests):
  - 4.10.1.1 to 4.10.1.21.
- MST Source Tests updates since Rev 1.1 CTS via approved SCRs.
  - 4.10.1.4
  - 4.10.1.8
  - 4.10.1.12
  - 4.10.1.21

MST 소스 CTS 업데이트 CTS Rev 1.1 이후

- MST 소스 테스트 버전은 1.1 CTS (총 21회 테스트) :
  - 4.10.1.1 to 4.10.1.21.
- 버전 1.1부터 MST 소스 테스트는 승인된 SCR을 통해 CTS를 업데이트했습니다.
  - 4.10.1.4
  - 4.10.1.8
  - 4.10.1.12
  - 4.10.1.21

CTS Updates - MST Source Device

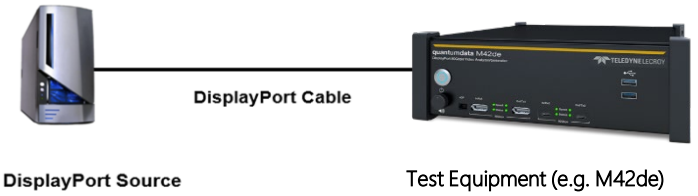
- How to run MST Source CTS:
  - Connect TE to Source DUT.



  - From Test Equipment software fill out CDF entry.
    - **Note**: Test Equipment automatically retrieves CDF entries from the VESA CDF JSON file.
  - Select MST Source Tests and then run them.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

CTS 업데이트 - MST 소스 장치

- 如何運行 MST 소스 CTS:
  - TE를 소스 DUT에 연결하세요.



  - 시험 장비 소프트웨어에서 CDF 항목을 작성하세요.
    - **참고: 테스트 장치는 VESA CDF JSON 파일에서 자동으로 CDF 항목을 검색합니다**.
  - MST 소스 테스트를 선택한 후 실행하세요.
  - 그래픽 사용자 인터페이스 안내를 따라 설정/검증을 하세요.
  - 테스트가 실행되면 HTML 보고서가 생성됩니다.

CTS 업데이트 - MST 소스 장치

MST 출처: CTS CDF 입력 정보

S.No	능력	CDF 등록	기본 값
1	MST 전송이 지원되나요? 선택지: 예, 아니오	MST_TRANS_SUPPORTED	네
2	최대 동시 스트림을 지원하나요? 선택지: 1, 2, 3, 4	MST_MAX_STREAM_COUNT	4
3	Source DUT가 업 요청을 처리하나요? 선택지: 예, 아니오	MST_UP_REQUEST_SUPPORTED	네
4	Source DUT가 RSN Up 요청을 처리하나요? 선택지: 예, 아니오	MST_RSN_REQUEST_SUPPORTED	아니
5	최대 데이지 체인 싱크대 수 지원하나요? 선택지: 1, 2, 3, 4	MST_MAX_DAISY_CHAIN_SINK_SUPPORTED	4
6	Source DUT가 파워 업-다운 물리 요청을 처리하나요? 선택지: 예, 아니오	MST_POWER_UP_DOWN_PHY_SUPPORTED	네

VESA

CTS Updates - MST Branch Device

- MST Branch Device Tests in Rev 1.1 CTS (54 tests)
  - Branch Setup 1: 6.10.1.1 to 6.10.1.12 (12 tests)
  - Branch Setup 2: 6.10.2.1 to 6.10.2.10 (10 tests)
  - Branch Setup 3: 6.10.3.1 to 6.10.3.14 (14 tests)
  - Branch Setup4: 6.10.4.1 to 6.10.4.14 (14 tests)
  - Branch Setup 5: 6.10.5.1 to 6.10.5.4 (4 tests)
- MST Branch Device Tests updates since Rev 1.1 CTS via approved SCRs.
  - Branch Setup 1: 6.10.1.[1,5,6,7,8,9,10,11,12] (9 tests)
  - Branch Setup 2: 6.10.2.[3,6,7] (3 tests)
  - Branch Setup 3: 6.10.3.[3] (1 test)
  - Branch Setup 4: 6.10.4.[2,3] (2 tests)
- MST Branch Device Tests addition since Rev 1.1 CTS via approved SCRs
  - Branch Setup 2: 6.10.2.11: Verify the DFP port allocate payload allocation and de-allocation sequence
  - Branch Setup 3: 6.10.3.15: Verify the DFP port allocate payload allocation and de-allocation sequence.

CTS 업데이트 - MST 지기 장치

- MST 분기 장치 버전 1.1 CTS에서 테스트된 것 (54회 테스트).
  - 브랜치 설정 1: 6.10.1.1부터 6.10.1.12까지 (12 테스트)
  - 브랜치 설정 2: 6.10.2.1부터 6.10.2.10까지(10번의 테스트)
  - 브랜치 설정 3: 6.10.3.1부터 6.10.3.14 (14 테스트)
  - 브랜치 설정 4: 6.10.4.1부터 6.10.4.14까지 (14개의 테스트)
  - 브랜치 설정 5: 6.10.5.1부터 6.10.5.4 (4번의 테스트).
- MST 분기 장치 테스트는 버전 1.1부터 CTS가 승인된 SCR을 통해 업데이트되었습니다.
  - 분기 설정 1: 6.10.1. [1,5,6,7,8,9,10,11,12] (9 테스트)
  - 분기 설정 2: 6.10.2. [3,6,7] (3 테스트)
  - 분기 설정 3: 6.10.3. [3] (1회 테스트)
  - 분기 설정 4: 6.10.4. [2,3] (2회 테스트).
- 버전 1.1부터는 승인된 SCR을 통해 MST 분기 장치 테스트가 추가됩니다.
  - 분기 생성 2: 6.10.2.11: DFP 포트 구성 페이로드 할당 및 분산 순서 검증
  - 분기 생성 3: 6.10.3.15: 페이로드 할당 및 분산 순서를 위한 DFP 포트 구성 검증.

CTS Updates - MST Branch Device

- How to run MST Branch CTS
  - Connect Test Equipment to Branch DUT in Setup 1.
  - From Test Equipment software fill out CDF entry.
  - Select MST Branch Setup 1 and then run.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.



CTS 업데이트 - MST 지기 장치

- 如何運行 MST 分支 CTS.
  - 테스트 장치를 설정 1의 브랜치 DUT에 연결하세요.
  - 시험 장비 소프트웨어에서 CDF 항목을 작성하세요.
  - MST 분기 설정 1을 선택한 후 실행하세요.
  - 그래픽 사용자 인터페이스 안내를 따라 설정/검증을 하세요.
  - 테스트가 실행되면 HTML 보고서가 생성됩니다.

CTS Updates - MST Branch Device

- How to run MST Branch CTS
  - Connect Test Equipment to Branch DUT in Setup 2.
  - From Test Equipment software fill out CDF entry.
  - Select MST Branch Setup 2 and then run.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.



CTS 업데이트 - MST 지부 장치

- 如何運行 MST 分支 CTS.
  - 테스트 장치를 구성 2의 브랜치 DUT에 연결하세요.
  - 시험 장비 소프트웨어에서 CDF 항목을 작성하세요.
  - MST 분기 설정 2를 선택한 후 실행하세요.
  - 그래픽 사용자 인터페이스 안내를 따라 설정/검증을 하세요.
  - 테스트가 실행되면 HTML 보고서가 생성됩니다.

CTS Updates - MST Branch Device

- How to run MST Branch CTS
  - Connect Test Equipment to Branch DUT in Setup 3.
  - From Test Equipment software fill out CDF entry.
  - Select MST Branch Setup 3 and then run.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

CTS 업데이트 - MST 지기 장치

- 如何運行 MST 分支 CTS.
  - 테스트 장치를 구성 3의 브랜치 DUT에 연결하세요.
  - 시험 장비 소프트웨어에서 CDF 항목을 작성하세요.
  - MST 분기 설정 3을 선택한 후 실행하세요.
  - 그래픽 사용자 인터페이스 안내를 따라 설정/검증을 하세요.
  - 테스트가 실행되면 HTML 보고서가 생성됩니다.



CTS Updates - MST Branch Device

- How to run MST Branch CTS
  - Connect Test Equipment to Branch DUT in Setup 4.
  - From Test Equipment software fill out CDF entry.
  - Select MST Branch Setup 2 and then run.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

CTS 업데이트 - MST 지기 장치

- 如何運行 MST 分支 CTS.
  - 테스트 장치를 설정 4의 브랜치 DUT에 연결하세요.
  - 시험 장비 소프트웨어에서 CDF 항목을 작성하세요.
  - MST 분기 설정 2를 선택한 후 실행하세요.
  - 그래픽 사용자 인터페이스 안내를 따라 설정/검증을 하세요.
  - 테스트가 실행되면 HTML 보고서가 생성됩니다.



CTS Updates - MST Branch Device

- How to run MST Branch CTS
  - Connect Test Equipment to Branch DUT in Setup 5.
  - From Test Equipment software fill out CDF entry.
  - Select MST Branch Setup 5 and then run.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

CTS 업데이트 - MST 지기 장치

- 如何運行 MST 分支 CTS.
  - 테스트 장치를 Setup 5의 브랜치 DUT에 연결하세요.
  - 시험 장비 소프트웨어에서 CDF 항목을 작성하세요.
  - MST 분기 설정 5를 선택한 후 실행하세요.
  - 그래픽 사용자 인터페이스 안내를 따라 설정/검증을 하세요.
  - 테스트가 실행되면 HTML 보고서가 생성됩니다.



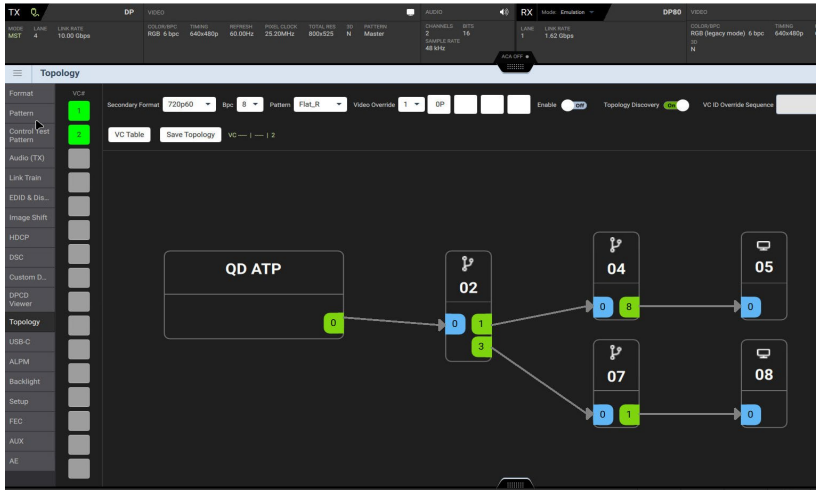
CTS 업데이트 - MST 지기 장치

MST 分支 CTS CDF 輸入細節

S.No	능력	CDF 등록	기본 값
1	DFP DP/USB-C 포트는 몇 개나 있나요? 선택지: 1부터 4까지	BRANCH_DUT_NO_OF_DFP_DPPORT	-
2	TE 송신기 포트에 연결된 MST 장치의 업링크 포트 번호 옵션: 0에서 16까지	BRANCH_DUT_UFP_PORT_NUM_CONNECTED_TO_TE	-
3	MST 장치의 다운링크 포트 번호는 TE Rx 포트로 반환됩니다 옵션: 0에서 16까지	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_TE	-
4	MST 장치 다운링크 포트 번호가 Sink1로 반환됩니다 옵션: 0에서 16까지	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK1	-
5	MST 장치의 다운스트림 포트 번호는 다시 Sink2에 연결됩니다 옵션: 0에서 16까지	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK2	-
6	MST 장치의 다운스트림 포트 번호를 다시 Sink3에 연결하세요 옵션: 0에서 16까지	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK3	-
7	MST 장치 다운링크 포트 번호는 Sink4에 다시 연결되어 있습니다 옵션: 0에서 16까지	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK4	-
8	Branch DUT 支援 CSN DFP 廣播嗎？ 選項：真、假	BRANCH_DUT_CSN_DFP_BROADCAST	틀렸다

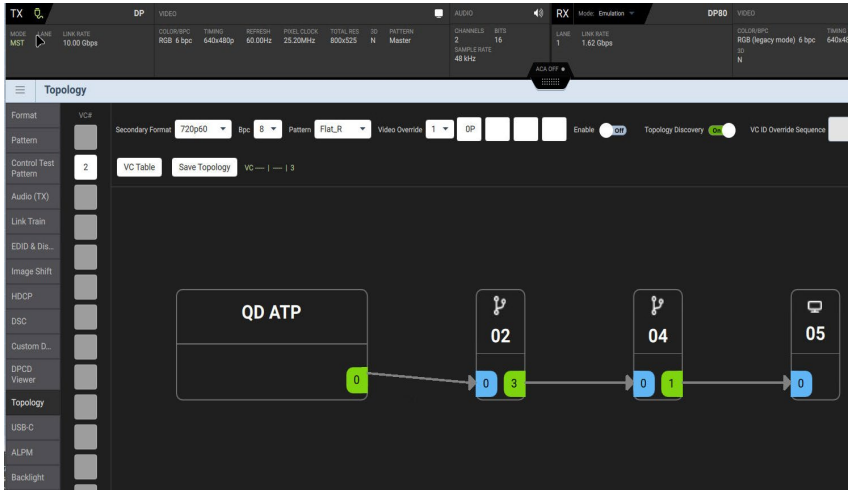
CTS Updates - MST Branch Device

- How to get port number value for CDF.
  - Connect Test Equipment to Branch DUT in Setup 2.
  - See Test Equipment Generator topology for ports (below left).
  - Disconnect one DFP port and see Test Equipment generator topology (below right).
  - The disconnected DFP port number is 1.



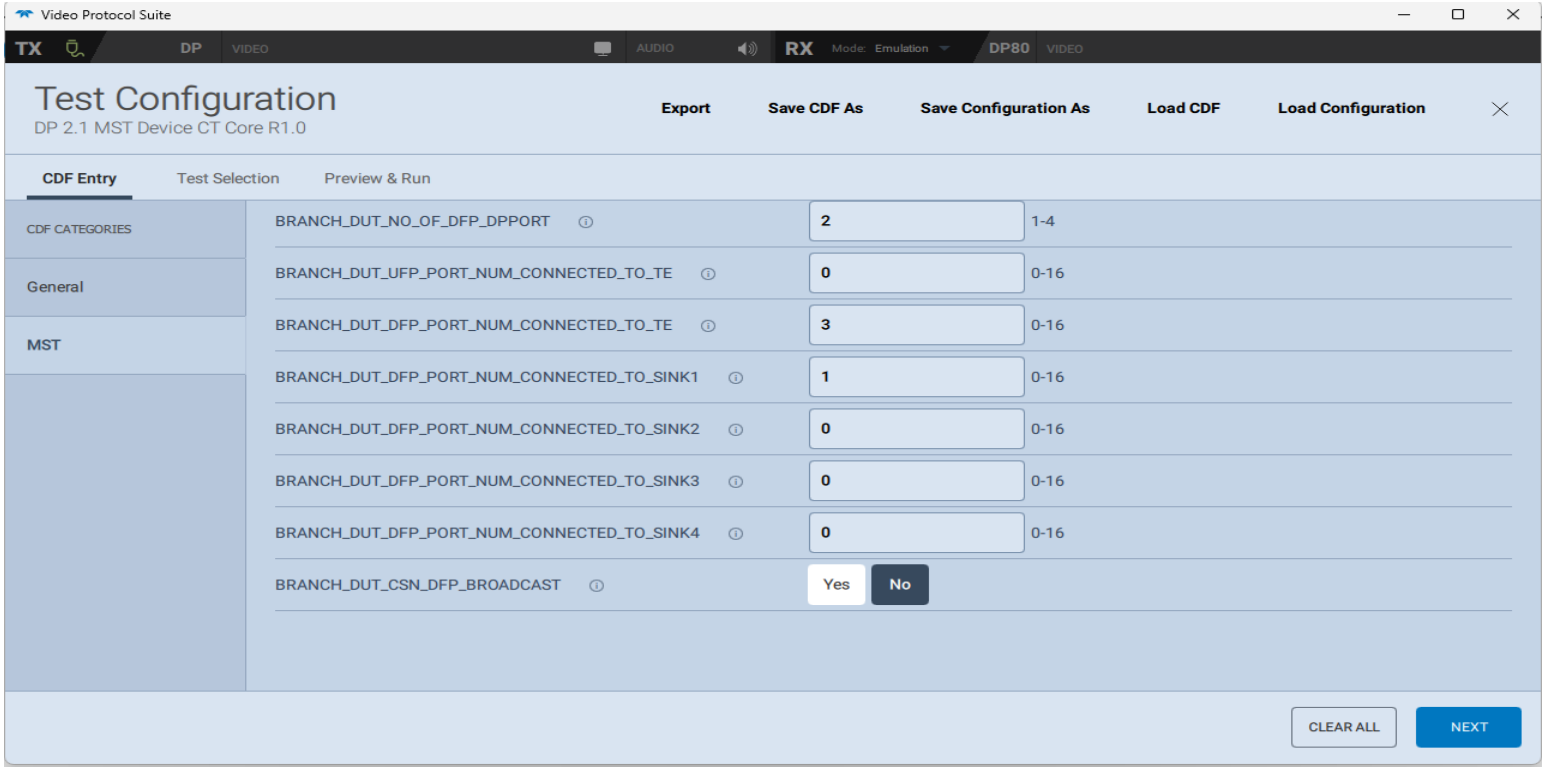
CTS 업데이트 - MST 지기 장치

- CDF의 포트 번호 값을 얻는 방법.
  - 테스트 장치를 구성 2의 브랜치 DUT에 연결하세요.
  - 포트 세부 사항은 테스트 장비 생성기 토폴로지를 참조해 주십시오.
  - DFP 포트를 분리하여 테스트 장비 생성기의 토폴로지를 확인하세요.
  - 분리된 DFP 포트 번호는 1입니다.



CTS Updates - MST Branch Device　CTS 업데이트 - MST 지기 장치

MST Branch CTS CDF Sample for Setup 2:　MST 分支 CTS CDF 설치 2 範例：



CTS Updates – Composite Sink Device

- MST Composite Sink Device Tests in Rev 1.1 CTS (48 tests)
  - CS Setup 1: 6.10.6.1 to 6.10.6.21 (21 tests)
  - CS Setup 2: 6.10.7.1 to 6.10.7.19 (19 tests)
  - CS Setup 3: 6.10.8.1 to 6.10.8.5 (5 tests)
  - CS Setup 4: 6.10.9.1 to 6.10.9.3 (3 tests)
- MST Composite Sink Device Test updates since Rev 1.1 CTS via approved SCRs.
  - CS Setup 1: 6.10.6.[2,4,6,7,8,11,12] (7 tests)
  - CS Setup 2: 6.10.7.[1,3,5,6,7,10] (6 tests)
  - CS Setup 3: 6.10.8.[1] (1 test)
- MST Composite Sink Device Test additions since Rev 1.1 CTS via approved SCRs
  - CS Setup 1: 6.10.6.22: Verify the DFP port allocate payload allocation and de-allocation sequence

CTS 업데이트 – 복합 싱크 설치

- 버전 1.1 CTS에서 테스트된 MST 복합 채널 장치 (48회 테스트).
  - CS Setup 1: 6.10.6.1 to 6.10.6.21 (21 tests)
  - CS Setup 2: 6.10.7.1 to 6.10.7.19 (19 tests)
  - CS Setup 3: 6.10.8.1 to 6.10.8.5 (5 tests)
  - CS Setup 4: 6.10.9.1 to 6.10.9.3 (3 tests)
- CTS 버전 1.1부터 MST 복합 융합 장비 테스트는 SCR 업데이트를 통해 승인되었습니다.
  - CS Setup 1: 6.10.6.[2,4,6,7,8,11,12] (7 tests)
  - CS Setup 2: 6.10.7.[1,3,5,6,7,10] (6 tests)
  - CS Setup 3: 6.10.8.[1] (1 test)
- 버전 1.1 CTS 이후로는 승인된 SCR을 통해 MST 복합 집계 장치 테스트가 추가되었습니다.
  - CS 설정 1: 6.10.6.22: 페이로드 할당 및 분산 순서를 위한 DFP 포트 구성 검증

CTS Updates - Composite Sink Device

- How to run MST Composite Sink Device CTS Setup 1
  - Connect Test Equipment to Composite Sink DUT in Setup 1.
  - From Test Equipment software fill out CDF entry.
  - Select MST Composite Sink Setup 1 Tests and then run them.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.



CTS 업데이트 - 복합 합성 버스 장치

- MST 컴포지트 케이블 장치 CTS 설정 1 실행 방법.
  - 설정 1에서는 테스트 장비가 복합 싱크대 DUT에 연결됩니다.
  - 시험 장비 소프트웨어에서 CDF 항목을 작성하세요.
  - MST 복합 싱크 설정 1 테스트를 선택한 후 실행하세요.
  - 그래픽 사용자 인터페이스 안내를 따라 설정/검증을 하세요.
  - 테스트가 실행되면 HTML 보고서가 생성됩니다.

CTS Updates - Composite Sink Device

- How to run MST Composite Sink Device CTS Setup 2
  - Connect Test Equipment to Composite Sink DUT in Setup 2.
  - From Test Equipment software fill out CDF entry.
  - Select MST Composite Sink Setup 2 Tests and then run them.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

CTS 업데이트 - 복합 합성 버스 장치

- MST 컴포지트 케이블 장치 CTS 설정 2 실행 방법.
  - 설정 2에서는 테스트 장비가 복합 싱크의 DUT에 연결됩니다。
  - 시험 장비 소프트웨어에서 CDF 항목을 작성하세요。
  - MST 컴포지트 싱크 세팅 2 테스트를 선택하고 실행하세요。
  - 설정/검증을 위한 그래픽 사용자 인터페이스 안내를 따라 하세요。
  - 테스트가 실행되면 HTML 보고서가 생성됩니다。



CTS Updates - Composite Sink Device

- How to run MST Composite Sink Device CTS Setup 3
  - Connect Test Equipment to Composite Sink DUT in Setup 3.
  - From Test Equipment software fill out CDF entry.
  - Select MST Composite Sink Setup 3 Tests and then run them.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

CTS 업데이트 - 복합 합성 버스 장치

- MST 컴포지트 케이블 장치 CTS 설정 3 실행 방법.
  - 셋업 3에서는 시험 장비가 복합 싱크대 시험 대상에 연결됩니다.
  - 시험 장비 소프트웨어에서 CDF 항목을 작성하세요.
  - MST 컴포지트 버스바 셋업 3 테스트를 선택한 후 실행하세요.
  - 그래픽 사용자 인터페이스 안내를 따라 설정/검증을 하세요.
  - 테스트가 실행되면 HTML 보고서가 생성됩니다.



CTS Updates - Composite Sink Device

- How to run MST Composite Sink Device CTS Setup 4
  - Connect Test Equipment to Composite Sink DUT in Setup 4.
  - From Test Equipment software fill out CDF entry.
  - Select MST Composite Sink Setup 4 Tests and then run them.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

CTS 업데이트 - 복합 합성 버스 장치

- MST 컴포지트 케이블 장치 CTS 설정 4 실행 방법.
  - 설정 4에서는 테스트 장비가 복합 싱크대 DUT에 연결되어 있습니다.
  - 시험 장비 소프트웨어에서 CDF 항목을 작성하세요.
  - 4 테스트용으로 MST 복합 싱크를 선택한 후 수행하세요.
  - 그래픽 사용자 인터페이스 안내를 따라 설정/검증을 하세요.
  - 테스트가 실행되면 HTML 보고서가 생성됩니다.



컴포지트 케이블 장치 CTS 업데이트

MST 복합匯 CTS CDF 輸入細節

S.No	능력	CDF 등록	기본 값
1	DFP DP/USB-C 포트는 몇 개나 있나요? 선택지: 1부터 4까지	BRANCH_DUT_NO_OF_DFP_DPPORT	-
2	TE 송신기 포트에 연결된 MST 장치의 업링크 포트 번호 옵션: 0에서 16까지	BRANCH_DUT_UFP_PORT_NUM_CONNECTED_TO_TE	-
3	MST 장치의 다운링크 포트 번호는 TE Rx 포트로 반환됩니다 옵션: 0에서 16까지	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_TE	-
4	MST 장치 다운링크 포트 번호가 Sink1로 반환됩니다 옵션: 0에서 16까지	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK1	-
5	MST 장치의 다운스트림 포트 번호는 다시 Sink2에 연결됩니다 옵션: 0에서 16까지	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK2	-
6	MST 장치의 다운스트림 포트 번호를 다시 Sink3에 연결하세요 옵션: 0에서 16까지	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK3	-
7	MST 장치 다운링크 포트 번호는 Sink4에 다시 연결되어 있습니다 옵션: 0에서 16까지	BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK4	-
8	Branch DUT가 CSN DFP 방송을 지원하나요? 선택지: 참, 거짓, 아니오	BRANCH_DUT_CSN_DFP_BROADCAST	錯誤

CTS Updates – Composite Sink Device

- How to get port number value for CDF.
  - Connect Test Equipment to Composite Sink DUT in Setup 2.
  - See Test Equipment Generator topology:
  - The Composite Sink has 2 DFP Ports, 1 internal and 1 external.
  - Test Equip Sink connected by DFP Port 1
  - Sink 1 connected on Test Equip DFP Port 0
  - Sink 2 connected on Sink1 DFP Port 1.



CTS 업데이트 – 복합 싱크 설치

- CDF의 포트 번호 값을 얻는 방법.
  - 설정 2에서는 테스트 장비가 복합 싱크의 DUT에 연결됩니다。
  - 테스트 장비 발전기 토폴로지를 참조하세요:
  - 복합 싱크대에는 내부와 외부에 각각 두 개의 DFP 포트가 있습니다.
  - 테스트 장비 버스바는 DFP 포트 1로 연결됩니다
  - 싱크 1은 테스트 장비 DFP 포트 0에 연결되어 있습니다
  - 싱크대 2는 싱크1의 DFP 포트 1에 연결되어 있습니다.

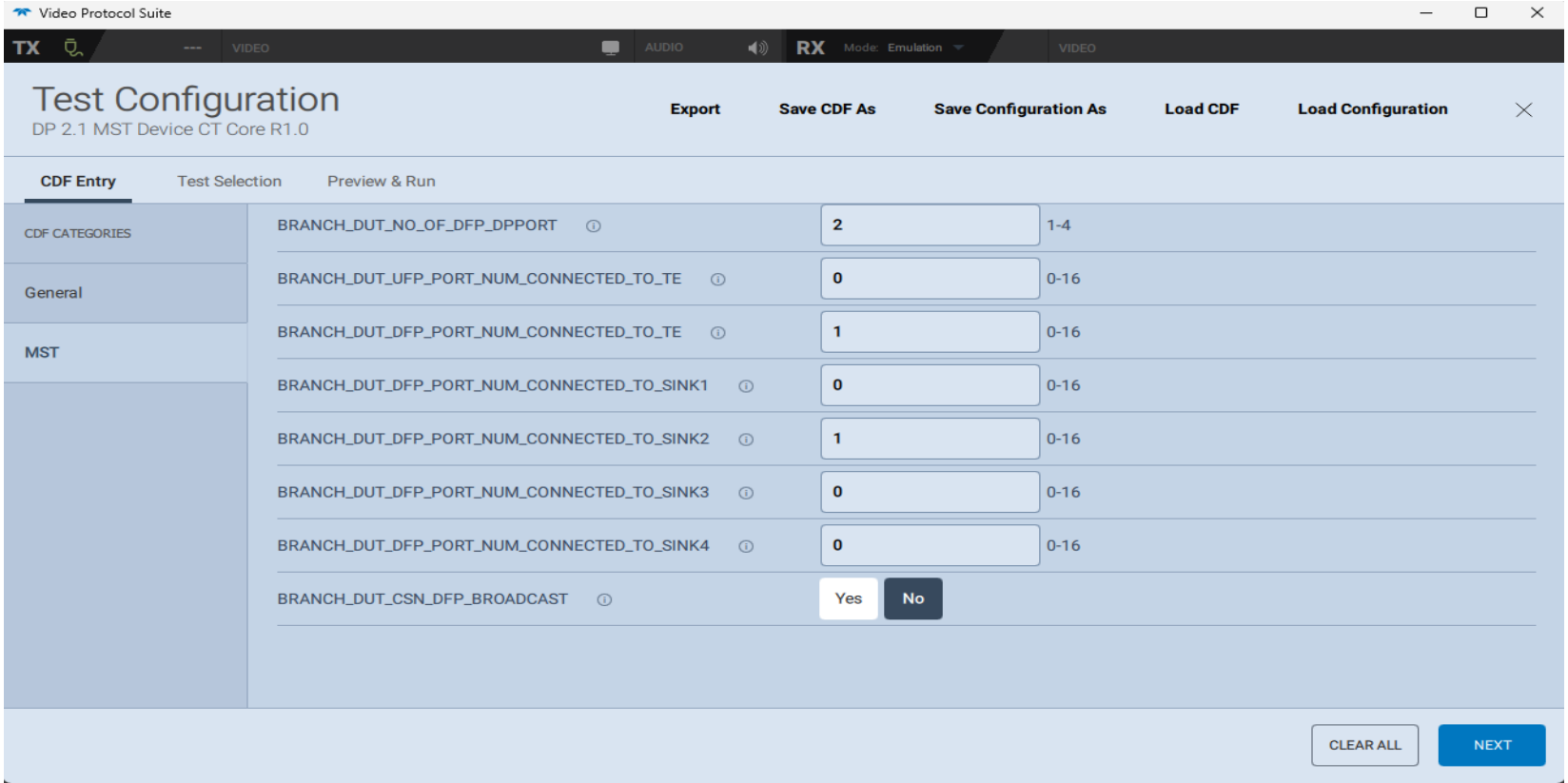


CTS Updates – Composite Sink Device

CTS 업데이트 – 복합 싱크 설치

MST Composite Sink CTS CDF Sample for Setup 2:

MST 컴포지트 가져오기 CTS CDF 설정 예제 2 :



Recent New Test Additions

- New Source Tests
  - 4.3.1.25 : Successful link training when Sink is in BIOS mode with random LTTPR .
  - 4.4.1.7 : Verify Source DUT video transmission timing is within MAX_UNCOMPRESSED_PIXEL_RATE capability
  - 4.4.1.8 : Validation for VSC-SDP when transmitting YCbCr4:20 and ITU-R BT.2020 formats

최근 추가된 테스트 항목들

- 새로운 소스 테스트.
  - 4.3.1.25: Sink가 BIOS 모드에 들어가 LTTPR을 무작위로 설정하면 링크 훈련이 성공합니다.
  - 4.4.1.7: 소스 테스트 장치의 비디오 전송 시간이 MAX_UNCOMPRESSED_PIXEL_RATE 능력 내에 있는지 확인
  - 4.4.1.8: YCbCr4:20 및 ITU-R BT.2020 포맷 전송 시 VSC-SDP 검증

Recent New Test Additions

- New Sink Tests
  - 5.7.1.7 EDID – Mandatory Blocks for HDR Displays
  - 5.7.19.7 Native DisplayID – Mandatory Blocks for HDR Displays
  - 5.7.20.4 Native DisplayID – Product Identification Data Block Product Name String ASCII Validation
  - 5.7.20.5 EDID – Product Identification Data Block Revision (Byte 1)
  - 5.7.20.6 EDID – Product Identification Data Block Number of Payload Bytes in Block (Byte 2)
  - 5.7.20.7 EDID – Product Identification Data Block Week of Manufacture/Model Tag and Year of Manufacture/Model Year (Bytes 12 and 13)
  - 5.7.20.8 EDID – Product Identification Data Block Product Name String ASCII Validation
  - 5.7.21.6 Native DisplayID – Display Parameters Data Block Horizontal and Vertical Image Size Verification
  - 5.7.21.7 EDID – Display Parameters Data Block Revision (Byte 1)
  - 5.7.21.8 EDID – Display Parameters Data Block Number of Payload Bytes in Block (Byte 2)
  - 5.7.21.9 EDID – Display Parameters Data Block Feature Support Flags Field (Byte 0Bh)
  - 5.7.21.10 EDID – Display Parameters Data Block Native Luminance-related Fields (Bytes 18h to 1Dh)
  - 5.7.21.11 EDID – Display Parameters Data Block Depth and Display Device Technology Fields (Byte 1Eh).

최근 추가된 테스트 항목들

- 신후이 시험.
  - 5.7.1.7 EDID – 강제 HDR 디스플레이 블록
  - 5.7.19.7 네이티브 DisplayID – HDR 표시를 위한 강제 차단
  - 5.7.20.4 네이티브 디스플레이ID – 제품 식별 데이터 블록 제품명 문자열 ASCII 인증
  - 5.7.20.5 EDID – 제품 식별 데이터 블록 개정판 (바이트 1)
  - 5.7.20.6 EDID – 제품 식별 데이터 블록 페이로드 바이트 (바이트 2)
  - 5.7.20.7 EDID – 제품 식별 데이터 블록 제조 주간/모델 라벨 및 제조 연도/모델 연도 (바이트 12 및 13)
  - 5.7.20.8 EDID – 제품 식별 데이터 블록 제품명 문자열 ASCII 검증
  - 5.7.21.6 네이티브 디스플레이ID – 디스플레이 매개변수 데이터 블록에서 수평 및 수직 이미지 크기 검증
  - 5.7.21.7 EDID – 디스플레이 매개변수 데이터 블록 수정 (바이트 1)
  - 5.7.21.8 EDID – 디스플레이 매개변수 데이터 블록 페이로드 바이트 (블록 2)
  - 5.7.21.9 EDID – 표시 매개변수 데이터 블록 기능 지원: 플래그 필드(바이트 0Bh)
  - 5.7.21.10 EDID – 디스플레이 매개변수 데이터 블록 네이티브 밝기 관련 필드 (바이트 18h에서 1Dh)
  - 5.7.21.11 EDID – 디스플레이 매개변수, 데이터 블록 깊이, 디스플레이 장치 기술 필드 (바이트 1Eh)。

Recent New Test Additions

- New Sink Tests Continued…
  - 5.7.21.12 – EDID – Display Parameters Data Block Horizontal and Vertical Image Size Verification
  - 5.7.22.8 – EDID – Display Interface Features Data Block Revision (Byte 1)
  - 5.7.22.9 – EDID – Display Interface Features Data Block Number of Payload Bytes in Block (Byte 2)
  - 5.7.22.10 – EDID – Display Interface Features Data Block Supported Interface Color Depth-related Fields
  - 5.7.22.11 – EDID – Display Interface Features Data Block Minimum Pixel Rate at Which YCbCr 4:2:0 Encoding Is Supported (Byte 7)
  - 5.7.22.12 – EDID – Display Interface Features Data Block Supported Interface Audio Capability and Feature Flags (Byte 8)
  - 5.7.22.13 – EDID – Display Interface Features Data Block Supported Interface Color Space and EOTF-related Fields
  - 5.7.22.14 – EDID – Display Interface Features Data Block Additional Supported Interface Color Space and EOTF-related Fields (Bytes 0Bh to 12h)
  - 5.4.1.9 : Verify Sink DUT displays the video timing based on MAX_UNCOMPRESSED_PIXEL_RATE capability
  - 5.6.3.8: Verify Sink DUT correctly reconstructs image when HActive % Slice_Count != 0.

최근 추가된 테스트 항목들

- 새로운 침몰 시험이 계속되었다…
  - 2012년 7월 7일 – EDID – 디스플레이 매개변수 데이터 블록 수평 및 수직 이미지 크기 검증
  - 5.7.22.8 – EDID – 디스플레이 인터페이스 기능 데이터 블록 개정판 (바이트 1)
  - 5.7.22.9 – EDID – 디스플레이 인터페이스 기능 데이터 블록, 페이로드 바이트 수(바이트 2)
  - 5.7.22.10 – EDID – 디스플레이 인터페이스 기능, 데이터 블록 지원 인터페이스, 색상 깊이 관련 필드
  - 5.7.22.11 – EDID – 디스플레이 인터페이스 기능이 YCbCr 4:2:0 최소 픽셀 속도 데이터 블록(바이트 7)으로 인코딩을 지원합니다
  - 5.7.22.12 – EDID – 디스플레이 인터페이스 기능, 데이터 블록, 지원 인터페이스, 오디오 기능 및 기능 플래그 (8바이트)
  - 5.7.22.13 – EDID – 디스플레이 인터페이스 기능, 데이터 블록 지원 인터페이스, 색상 공간, EOTF 관련 필드
  - 5.7.22.14 – EDID – 디스플레이 인터페이스 기능, 데이터 블록, 추가 지원 인터페이스, 색상 공간, EOTF 관련 필드(바이트 0Bh부터 12h까지)
  - 5.4.1.9: MAX_UNCOMPRESSED_PIXEL_RATE 기능을 기반으로 임포트된 테스트 장치의 비디오 표시 타이밍을 검증합니다
  - 5.6.3.8: HActive % Slice_Count ! = 0, 가져오기 DUT가 이미지를 올바르게 재구성하는지 검증합니다.

Summary

- **Key Takeaways**
  - CTS coverage significantly expanded since Rev 1.1
  - New Source, Branch, and Composite Sink validations added
  - Test Equipment software supports automated CDF population via VESA JSON file
  - Simplified CTS execution workflow
  - New tests improve EDID, NDID, HDR and MST interoperability coverage

초록

- **주요 요약.**
  - Rev 1.1 이후 CTS 보장이 크게 확대되었습니다
  - 소스 코드, 분기 및 복합 교환 검증 기능 추가
  - 테스트 장비 소프트웨어는 VESA JSON 파일을 통해 자동으로 CDF를 생성하는 것을 지원합니다
  - 간소화된 CTS 실행 워크플로우
  - 새로운 테스트는 EDID, NDID, HDR, MST 상호운용성에 대한 범위를 강화합니다

Q&A 및 피드백

Alok Soni/Neal Kendall – 감사합니다

Teledyne LeCroy

2026년10월12일 – 서울, 대한민국

VESA 디스플레이포트 자동차 확장 (DP AE) 기능 안전 구현 테스트

Neal Kendall and Alok Soni

Teledyne LeCroy

2026년 10월 12일 – 서울, 대한민국

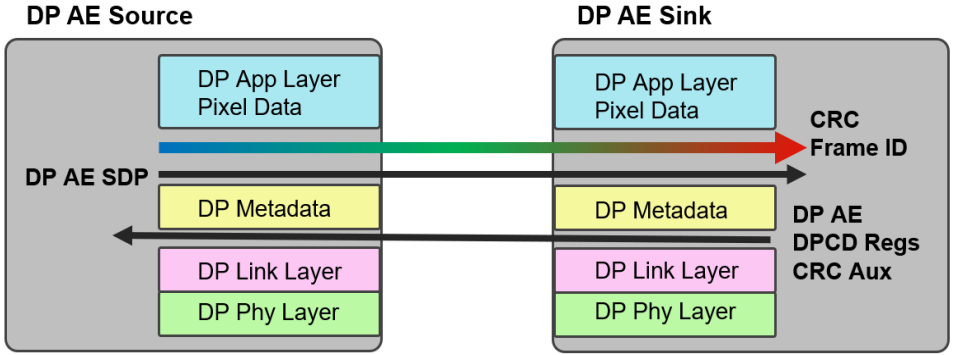
DisplayPort 오토모티브 익스텐션 – 소개

VESA DisplayPort 자동차 확장 서비스와 디스플레이포트 – 무엇이 다른가요?

- 전통적인 DisplayPort는 링크 신뢰성에 중점을 둡니다:
  - 링크 훈련, 링크 정렬, 시계 회복.
  - 전방 오류 수정(FEC).
  - 디스플레이 스트림 압축(DSC).
  - 영상과 오디오 전송 중.
  - 다중 스트림 전송(MST).
- DisplayPort는 이를 검증하지 않습니다:
  - 전체 이미지 파이프라인이 정확했습니다.
  - 올바른 이미지가 생성되었습니다.
  - 프레임이 손실되지 않았습니다.
  - 사진들은 제때 도착했다.

참고: DisplayPort Automotive Extension의 토폴로지는 정적이라고 가정합니다; 검색, 초기화 및 구성이 단순화되었습니다.

- DisplayPort에 대한 자동차 확장 애드온:
  - AE는 DisplayPort 2.1a 및/또는 eDP 2.0 사양을 사용합니다.
  - DP AE는 기능, 상태 및 구성을 위한 새로운 DP AE DPCD 레지스터를 도입했습니다.
  - DP AE는 영상과 데이터에 대해 CRC 검사를 사용합니다.
  - DP AE는 수신된 DisplayPort 스트림에서 프레임 시퀀스와 프레임 타이밍을 확인합니다.



DisplayPort 자동차 확장 – 프로필

기능 안전 및 보안 프로필

기능 안전 요소 – 프로파일 1 및 2

압축되지 않은 픽셀에서의 CRC	압축된 픽셀에 대한 CRC
재구성된 DSC 픽셀에 대한 CRC	보조 데이터 패킷(SDP)에서의 CRC
관심 지역 CRC	CRC의 메인 스트림 속성(MSA)
프레임 드롭, 반복 및 타임아웃 모니터링	상태 보고

- 자동차 확장 기능.
  - 기능 안전(프로파일 1 및 2) - 우발적 고장으로부터 보호.
  - 보안 (프로필 3 및 4) – 악의적인 침입과 수정으로부터 보호합니다.

보안 요소 – 프로파일 3 및 4

압축되지 않은 픽셀/압축 바이트 및 MSA에서의 MAC	DP AE 보조 데이터 패킷(SDP)에 MAC
데이터 평면 보안 (보조 채널 인증)	AE 보조 데이터 패킷(SDP)의 완전한 무결성 보안

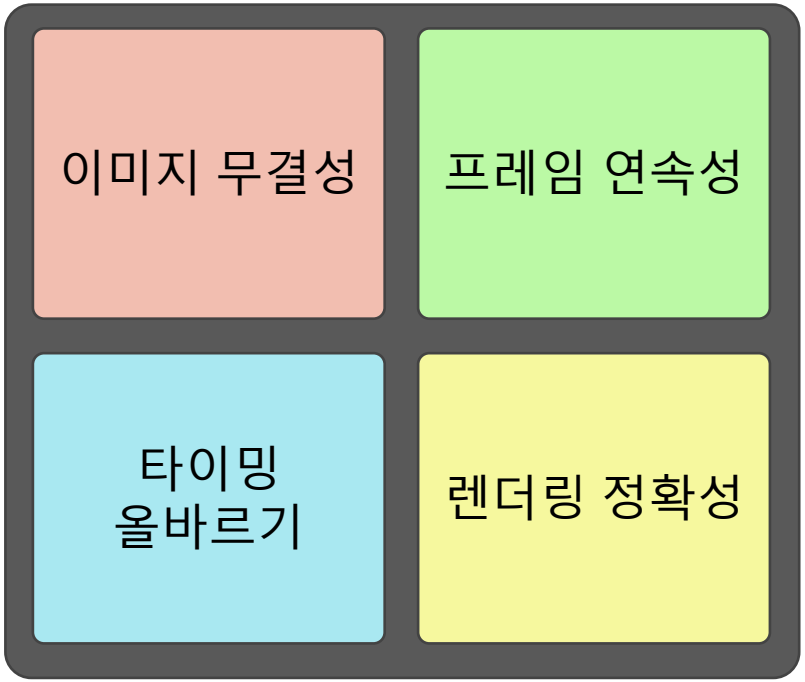
DisplayPort 자동차 확장 – 기능 안전

디스플레이포트를 비디오 전송 인터페이스에서 자동차 디스플레이용 종단 간 모니터링 시스템으로 확장함

왜 DP AE가 기능 안전인지?

- 자동차 디스플레이는 점점 더 안전에 중요한 정보를 제공합니다.
- 전통적인 DisplayPort는 링크 전송을 검증하지만, 종단 간 이미지 정확성은 확인하지 않습니다.
- DisplayPort AE는 모니터링 메커니즘을 추가합니다:
  - 이미지 무결성.
  - 프레임 연속성.
  - 타이밍 정확성.
  - 렌더링 정확성.
- DisplayPort AE는 빠른 장애 감지와 시스템 수준의 안전 대응을 가능하게 합니다.
- DisplayPort AE는 계기판에서 다중 디스플레이 조종석 아키텍처까지 확장 가능합니다.

디스플레이포트 자동차 확장 기능 안전



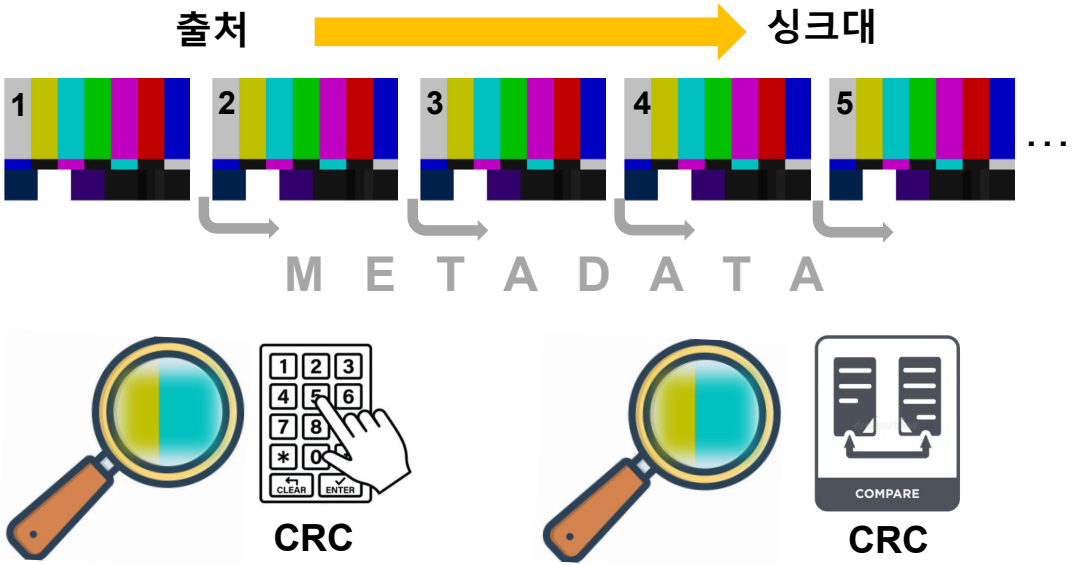
DisplayPort AE – 기능 안전 – 이미지 무결성

이미지 무결성 모니터링 – 이미지 데이터가 올바르게 도착했는가?

목표: 표시되는 이미지가 소스에서 생성된 이미지와 일치하는지 검증합니다.

- 기전:
  - CRC 픽셀 (압축되지 않은 또는 압축된 "재구성된 픽셀").

    참고: 압축은 SerDes의 비용을 낮추고, 케이블 복잡성과 무게를 줄이며, 전력 소비를 줄입니다.
  - CRC 압축 바이트.
  - CRC 메인 스트림 속성(MSA).
  - CRC 보조 데이터 패킷(SDP).
  - CRC 자동차 확장 SDP.
  - CRC 보조 채널 메시징.
  - CRC 관심 영역(ROI).
- 탐지함:
  - 픽셀 손상(압축/비구성).
  - 링크 전송 및 메타데이터 오류.



DisplayPort AE – 기능 안전 - 관심 영역

관심 영역(ROI)을 이용한 프레임 비디오 중요 모니터링

목표: 디스플레이에서 가장 중요한 영역을 지정함.

- 목적.
  - 디스플레이의 안전이 중요한 부분에 기능 안전 모니터링을 집중하세요.
  - 가장 중요한 시각 정보를 표적으로 보호할 수 있게 합니다.
- 관심 지역(ROI) 역량.
  - 각 ROI에 대해 별도로 계산된 CRC입니다.
  - 디스플레이당 최대 16 ROI를 제공합니다.
  - ROI는 동적으로 활성화, 비활성화 또는 재구성할 수 있습니다.
  - ROI는 디스플레이 내에서 겹칠 수 있습니다.
  - ROI 좌표는 초기화 시 보조 채널을 통해 싱크로 전송됩니다.



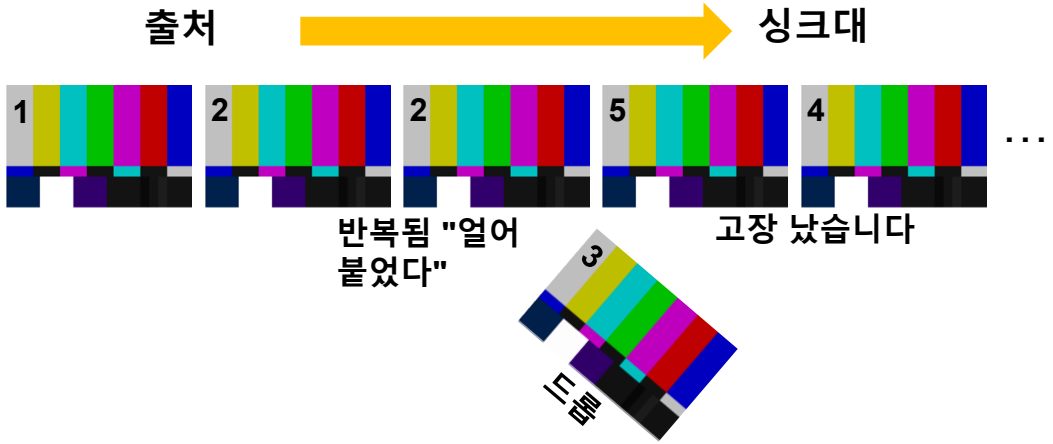


DisplayPort AE – 기능 안전 – 프레임 연속성

프레임 연속성 모니터링 검사, 모든 프레임을 받았나요?

목표: 모든 비디오 프레임이 올바른 순서로 도착하는지 확인.

- 기전:
  - 프레임마다 증가하는 FRAME ID 카운터입니다.
- 탐지함:
  - 프레임이 빠졌다.
  - 반복 프레임.
  - 순서가 맞지 않는 프레임.

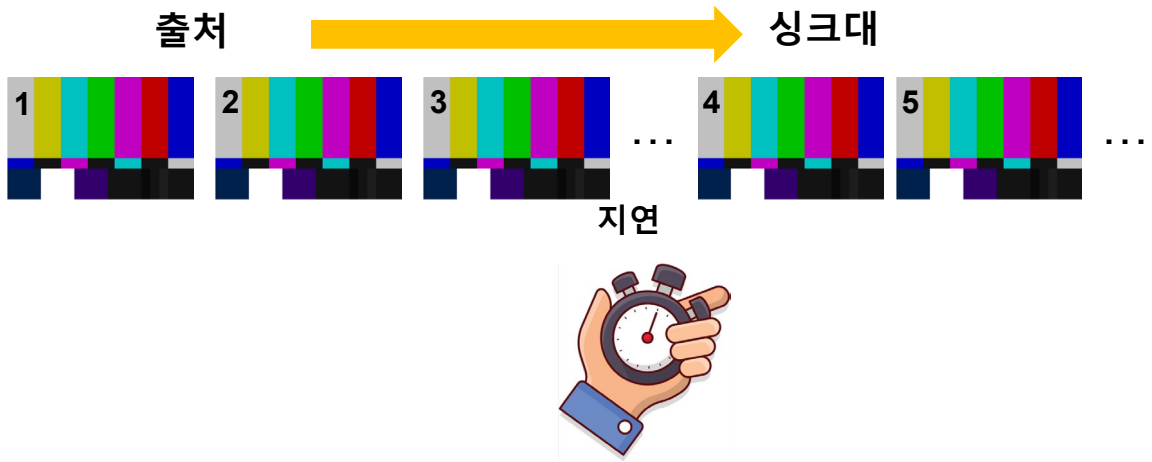


DisplayPort AE – 기능 안전 – 타이밍 정확성

타이밍 정확성 검사, 영상 프레임과 메타데이터가 제때 도착했나요?

목표: 정보가 예상 시에 도착하는지 확인.

- 기전:
  - 타임아웃 모니터링.
  - 프레임 ID 진행
  - AE SDP 메타데이터 모니터링.
- 탐지함:
  - 프레임 지연.
  - 파이프라인이 정체된 상태.
  - 과도한 지연.



DisplayPort AE – 기능 안전 – 결함 감지/격리

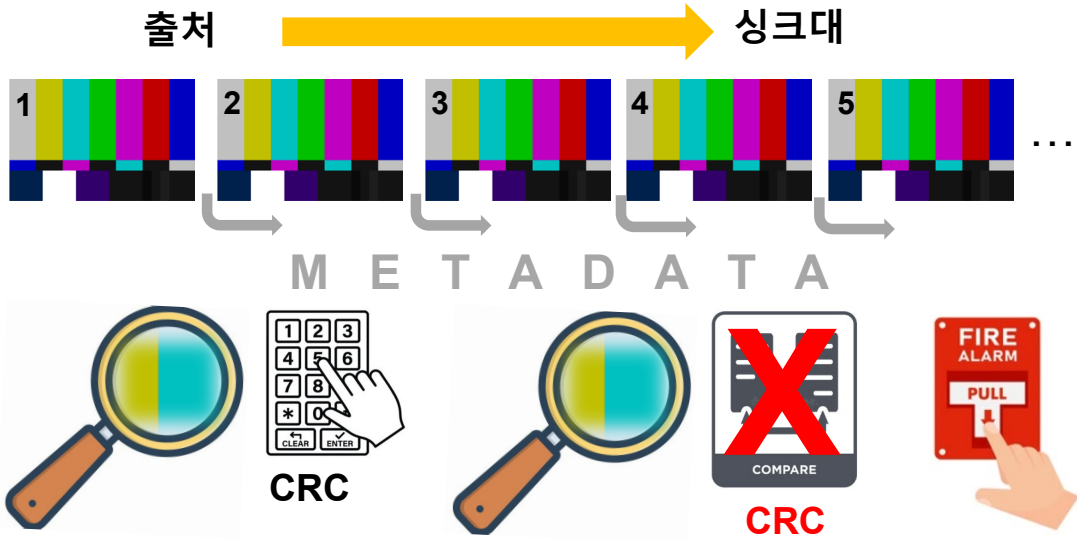
신속한 고장 탐지 및 에스컬레이션 - 차량이 적절히 대응할 수 있도록 합니다

목표: 오류가 감지되면 운전자와 시스템에 경고.

- 소프트 에러:
  - CRC 불일치.
  - 프레임 불일치.
  - 타임아웃 이벤트.
- 하드 에러스:
  - 지속적인 결함.
  - 오류 임계값 초과.

참고: ROI는 자체 CRC를 가지고 있습니다.

- 결함 감지 활성화:
  - 운전자 경고.
  - 실패 방지 작동.
  - 시스템 중복 활성화 및 진단 로깅.

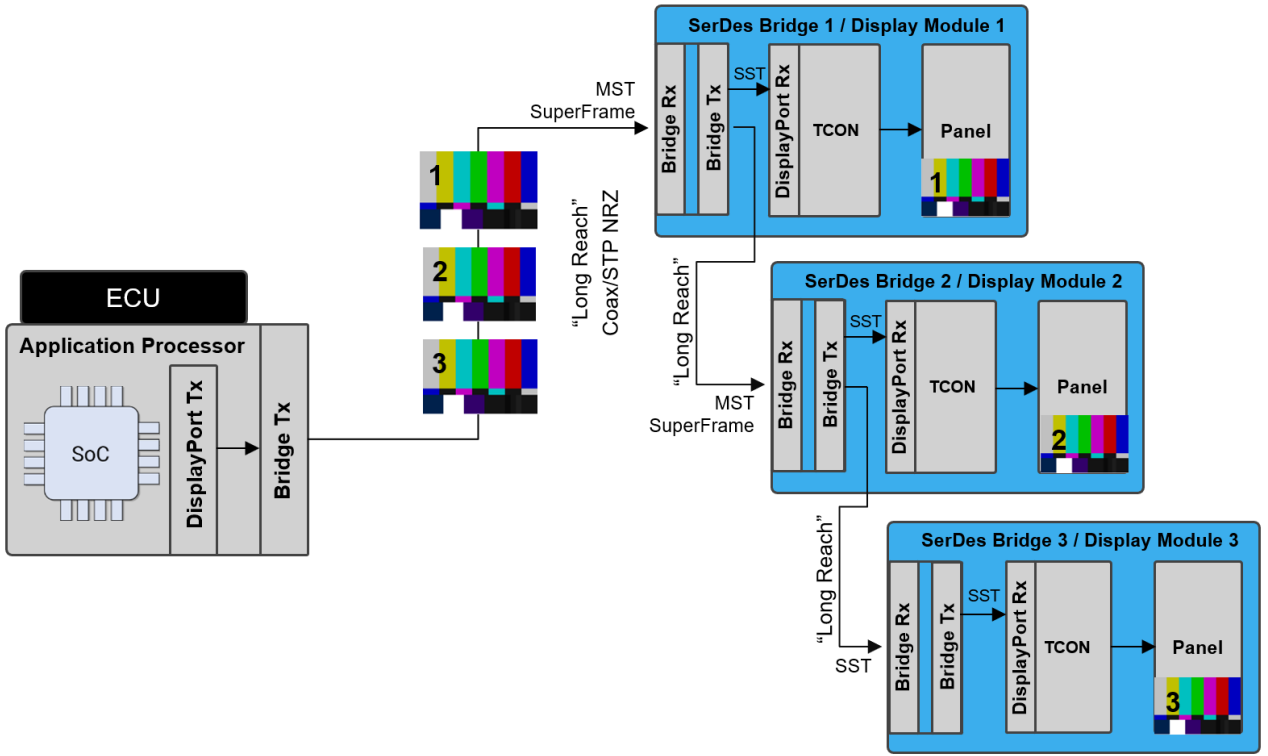


DisplayPort AE – 토폴로지 및 아키텍처

DisplayPort 자동차 확장 토폴로지

DP AE 테스트 초기화.

- 멀티스트림 전송(MST) – 단일 물리적 채널 위에 여러 가상 채널을 통해 여러 디스플레이를 지원합니다.
- MST는 OpenGMSL, FPD Link, A-Phy와 같은 '롱 리치' 전송 매체를 통해 실행됩니다.

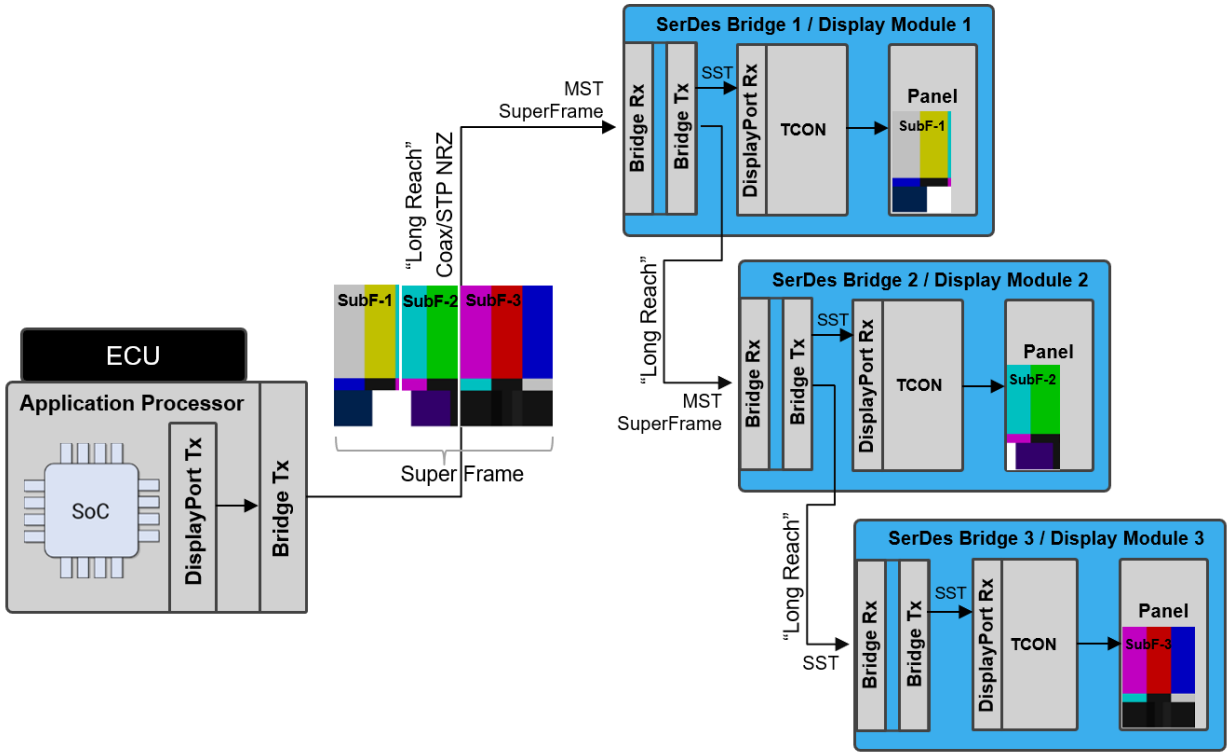


DisplayPort AE – 토폴로지 및 아키텍처

DisplayPort 자동차 확장 토폴로지

DP AE 테스트 초기화.

- 슈퍼프레임과 서브프레임 – 단일 비디오 프레임이 여러 디스플레이로 확장되었습니다.
- 슈퍼프레임은 OpenGMSL, FPD Link, A-Phy와 같은 '롱 리치' 전송 매체를 통해 실행됩니다.



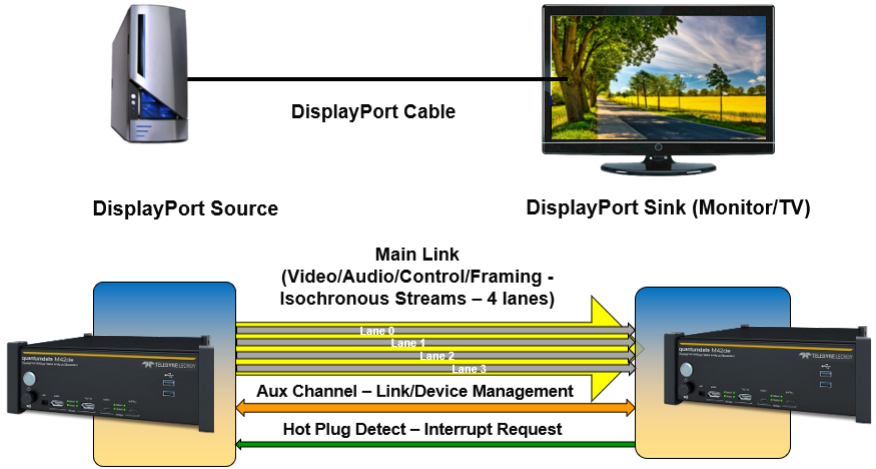
DisplayPort 자동차 확장 기능 안전 구현 테스트

DisplayPort AE – 기능 안전 테스트

DisplayPort 자동차 확장 구현 테스트 방법

DP AE 소스/싱크 테스트.

- 장치 에뮬레이션:
  - DP AE 소스를 에뮬레이션하여 디스플레이를 테스트하고 토폴로지를 표현하세요.
  - DP AE 디스플레이를 에뮬레이션하여 소스를 테스트하고 토폴로지를 표시합니다.
- 비디오 생성 구성:
  - MST 또는 슈퍼프레임 토폴로지를 설정하세요.
  - 관심 지역(ROI) 구성.
- 비디오 및 프로토콜 분석:
  - 들어오는 스트림의 실시간 뷰.
  - 영상과 메타데이터의 캡처, 후처리 분석.
  - VESA DisplayPort 자동차 로고 프로그램 지원을 위한 준수 테스트.





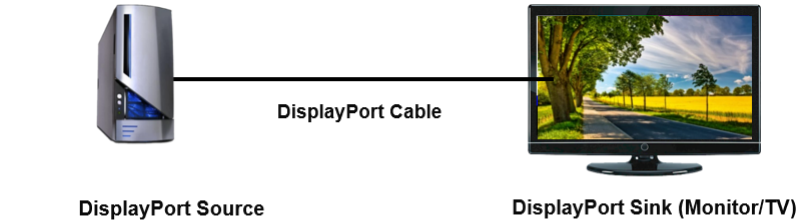
M42DE 80G 비디오 분석기/생성기

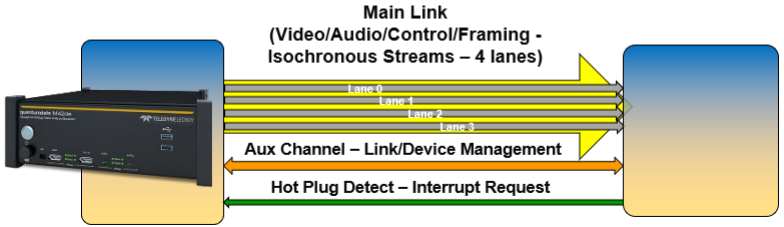
DisplayPort AE – 기능 안전 테스트

DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오 생성기 설정.

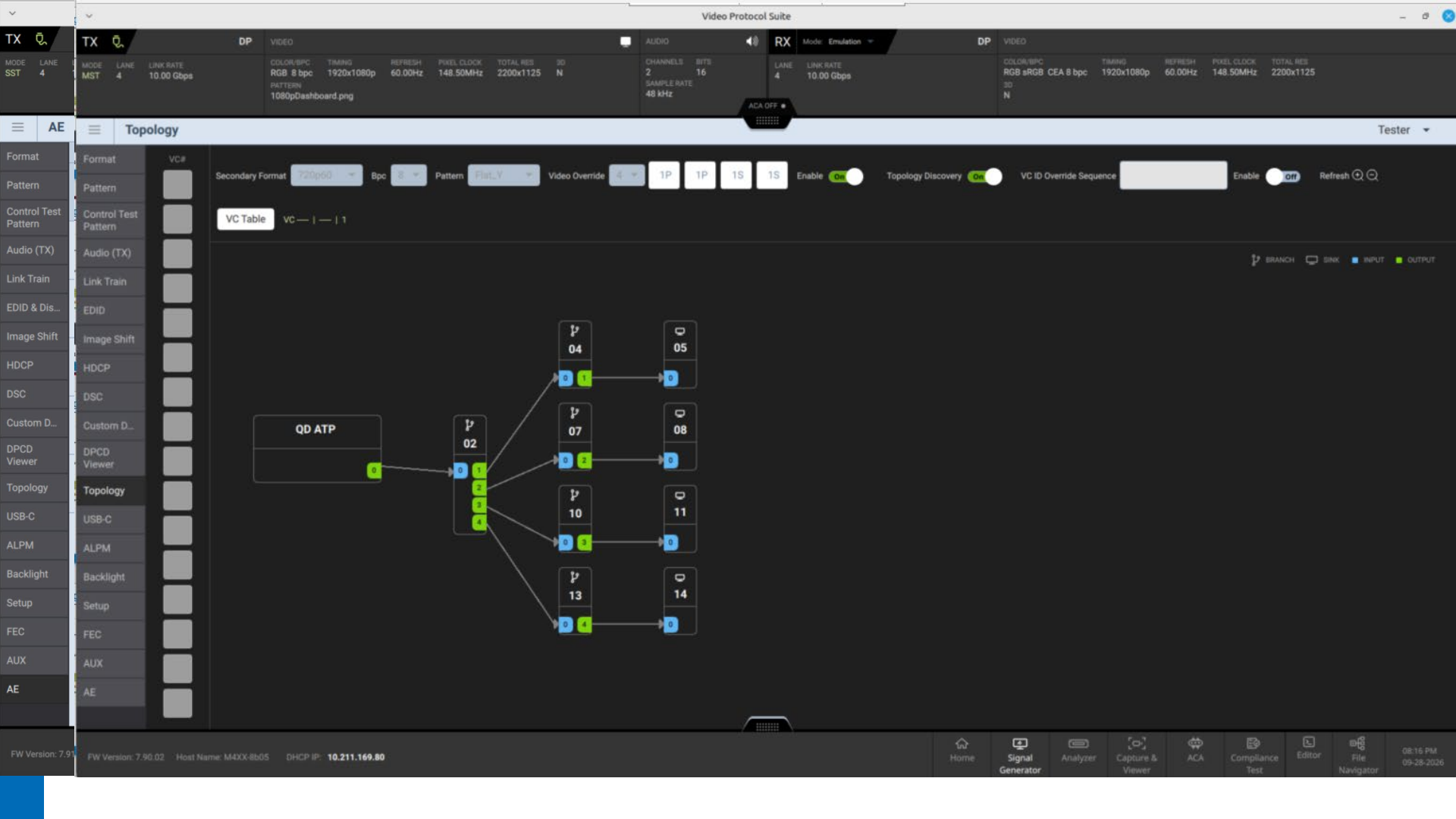
- 토폴로지, 스트림 수, 프로필 및 투자 수익률(ROI) 구성 등.
- 부차적 과정 선택.
- 관심 지역 설정 중.
- 오류 임계값 설정 중입니다.
- Sink DPCD DP AE 레지스터 확인.
- 오류 주입.
- 자동차 확장 상태 보기.







M42DE 80G 비디오 분석기/생성기

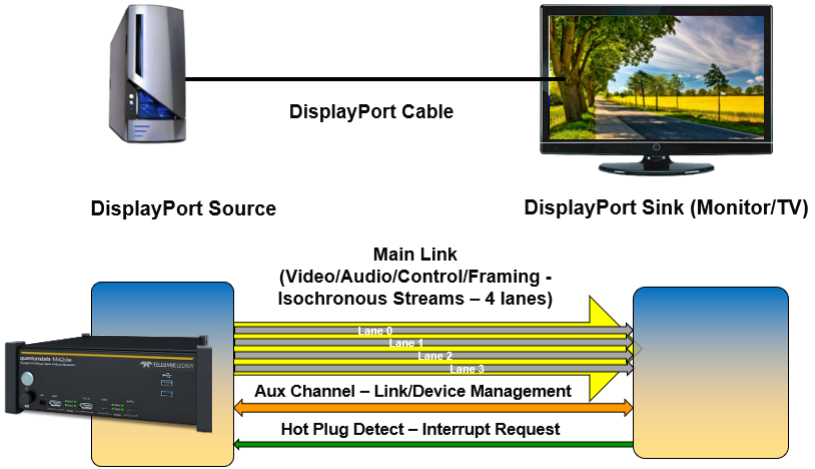

Video Protocol Suite
TX
DP
VIDEO
AUDIO
RX
Mode: Emulation
DP
VIDEO
MODE SST
LANE 4
MODE MST
LANE 4
LINK RATE 10.00 Gbps
COLOR/BPC RGB 8 bpc
TIMING 1920x1080p
REFRESH 60.00Hz
PIXEL CLOCK 148.50MHz
TOTAL RES 2200x1125
3D N
PATTERN 1080pDashboard.png
CHANNELS 2
BITS 16
SAMPLE RATE 48 kHz
LANE 4
LINK RATE 10.00 Gbps
COLOR/BPC RGB sRGB CEA 8 bpc
TIMING 1920x1080p
REFRESH 60.00Hz
PIXEL CLOCK 148.50MHz
TOTAL RES 2200x1125
3D N
ACA OFF
AE
Topology
Tester
Format
Pattern
Control Test Pattern
Audio (TX)
Link Train
EDID
Image Shift
HDCP
DSC
Custom D...
DPCD Viewer
Topology
USB-C
ALPM
Backlight
Setup
FEC
AUX
AE
VC#
Secondary Format
720p60
Bpc
8
Pattern
Flat_Y
Video Override
4
1P
1P
1S
1S
Enable
On
Topology Discovery
On
VC ID Override Sequence
Enable
Off
Refresh
VC Table
VC — | — | 1
BRANCH
SINK
INPUT
OUTPUT
QD ATP
02
04
05
07
08
10
11
13
14
FW Version: 7.90.02
Host Name: M4XX-8b05
DHCP IP: 10.211.169.80
Home
Signal Generator
Analyzer
Capture & Viewer
ACA
Compliance Test
Editor
File Navigator
08:16 PM
09-28-2026

DisplayPort AE – 기능 안전 테스트

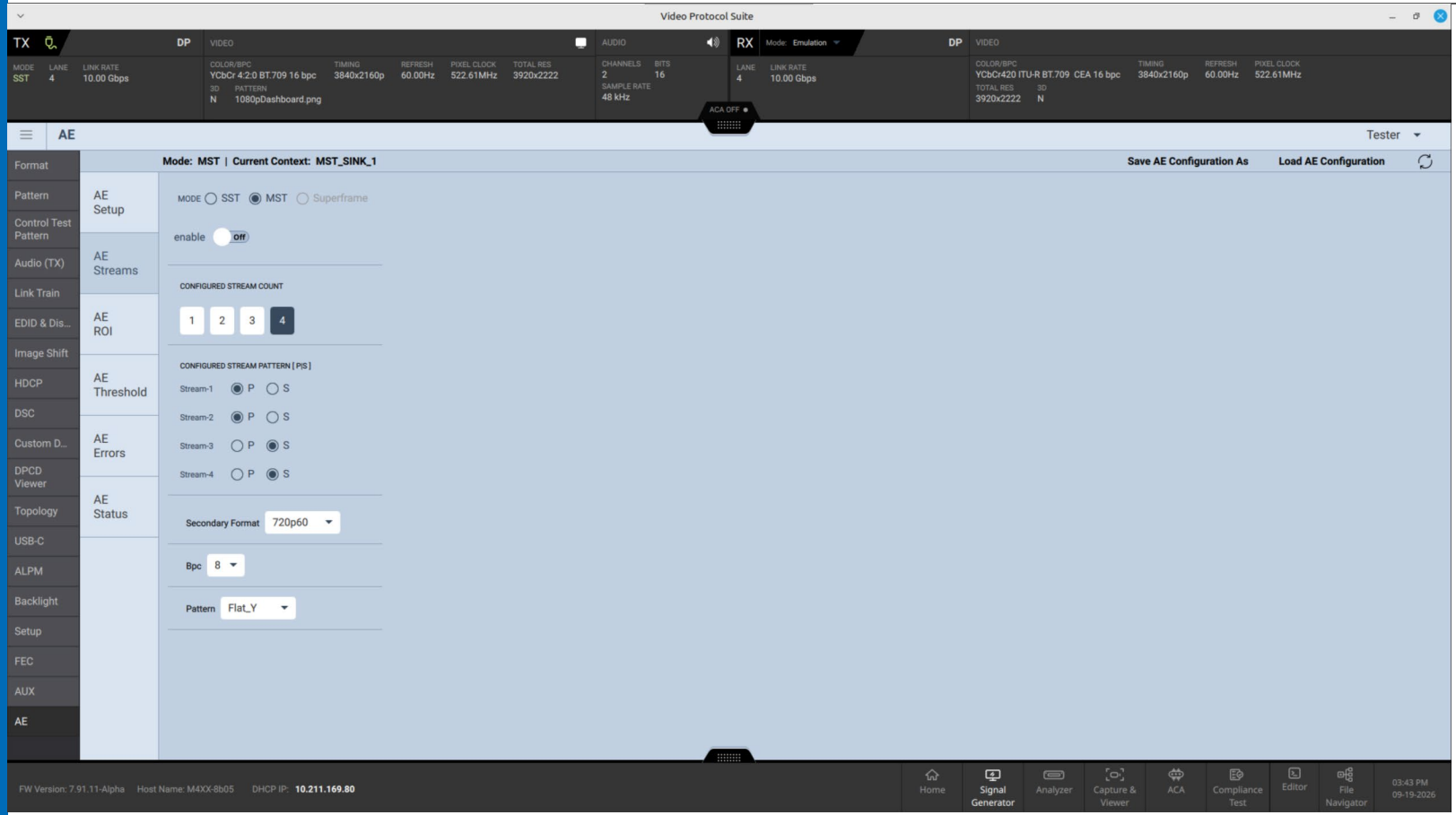
DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오 생성기 설정.

- 토폴로지, 스트림 수, 프로필 및 투자 수익률(ROI) 구성 등.
- **부차적 과정 선택.**
- 관심 지역 설정 중.
- 오류 임계값 설정 중입니다.
- Sink DPCD DP AE 레지스터 확인.
- 오류 주입.
- 자동차 확장 상태 보기.



DisplayPort AE – Testing Functional Safety

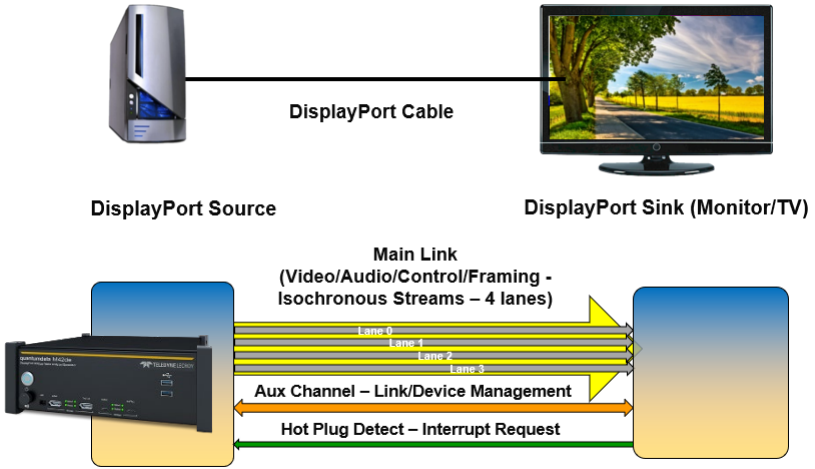


DisplayPort AE – 기능 안전 테스트

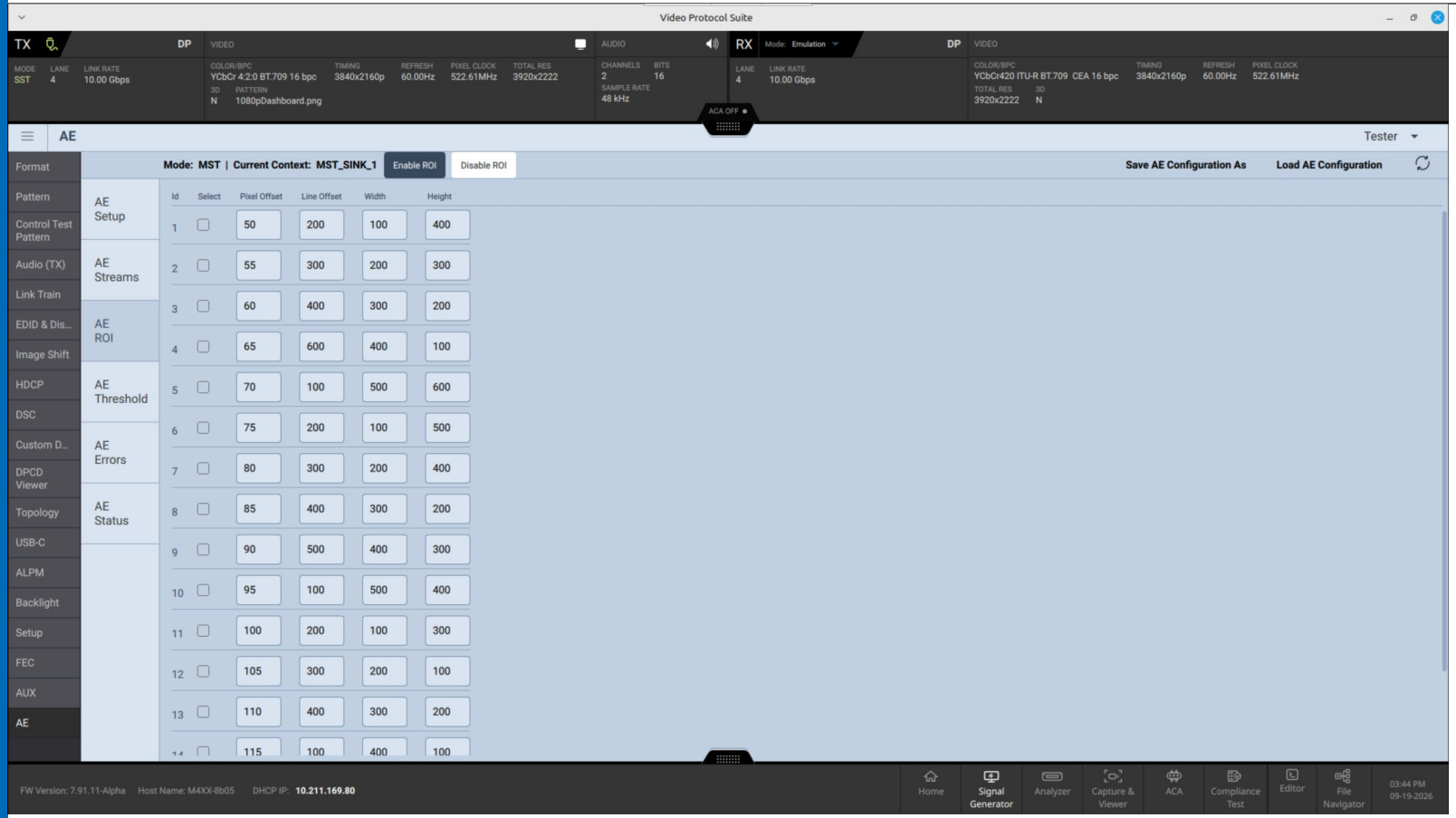
DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오 생성기 설정.

- 토폴로지, 스트림 수, 프로필 및 투자 수익률(ROI) 구성 등.
- 부차적 과정 선택.
- **관심 지역 설정 중**.
- 오류 임계값 설정 중입니다.
- Sink DPCD DP AE 레지스터 확인.
- 오류 주입.
- 자동차 확장 상태 보기.



DisplayPort AE – Testing Functional Safety

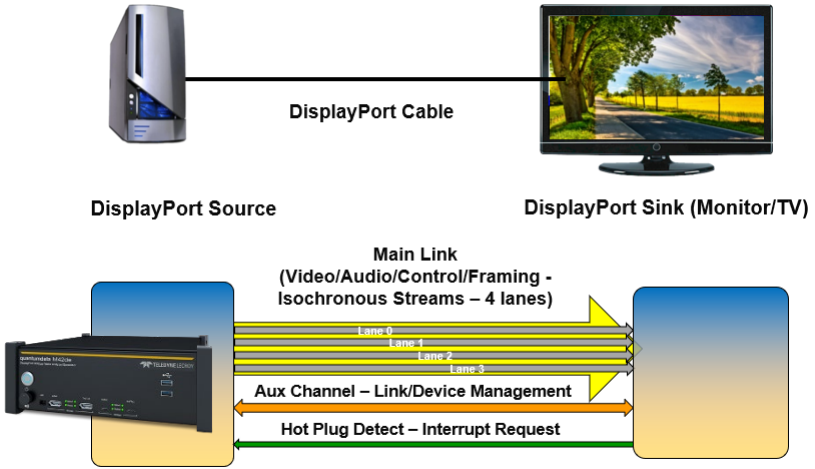


DisplayPort AE – 기능 안전 테스트

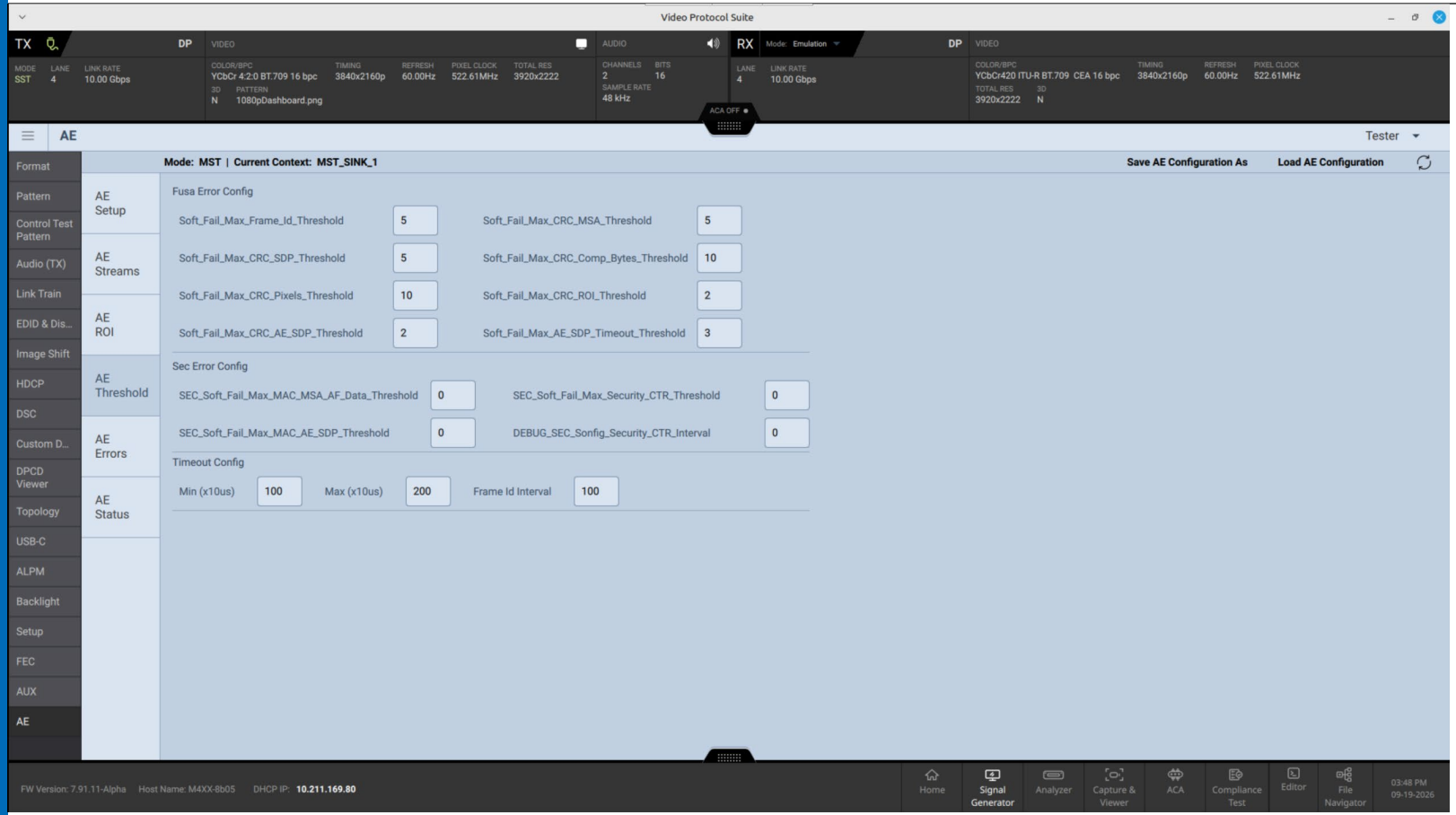
DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오 생성기 설정.

- 토폴로지, 스트림 수, 프로필 및 투자 수익률(ROI) 구성 등.
- 부차적 과정 선택.
- 관심 지역 설정 중.
- **오류 임계값 설정 중입니다**.
- Sink DPCD DP AE 레지스터 확인.
- 오류 주입.
- 자동차 확장 상태 보기.



DisplayPort AE – Testing Functional Safety

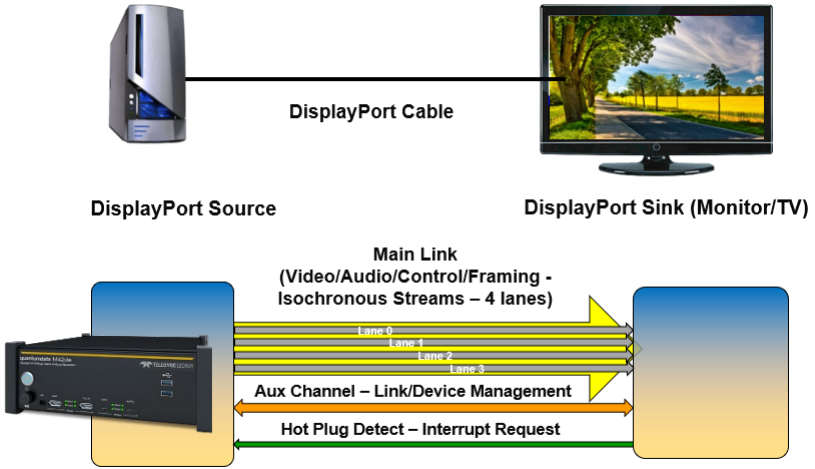


DisplayPort AE – 기능 안전 테스트

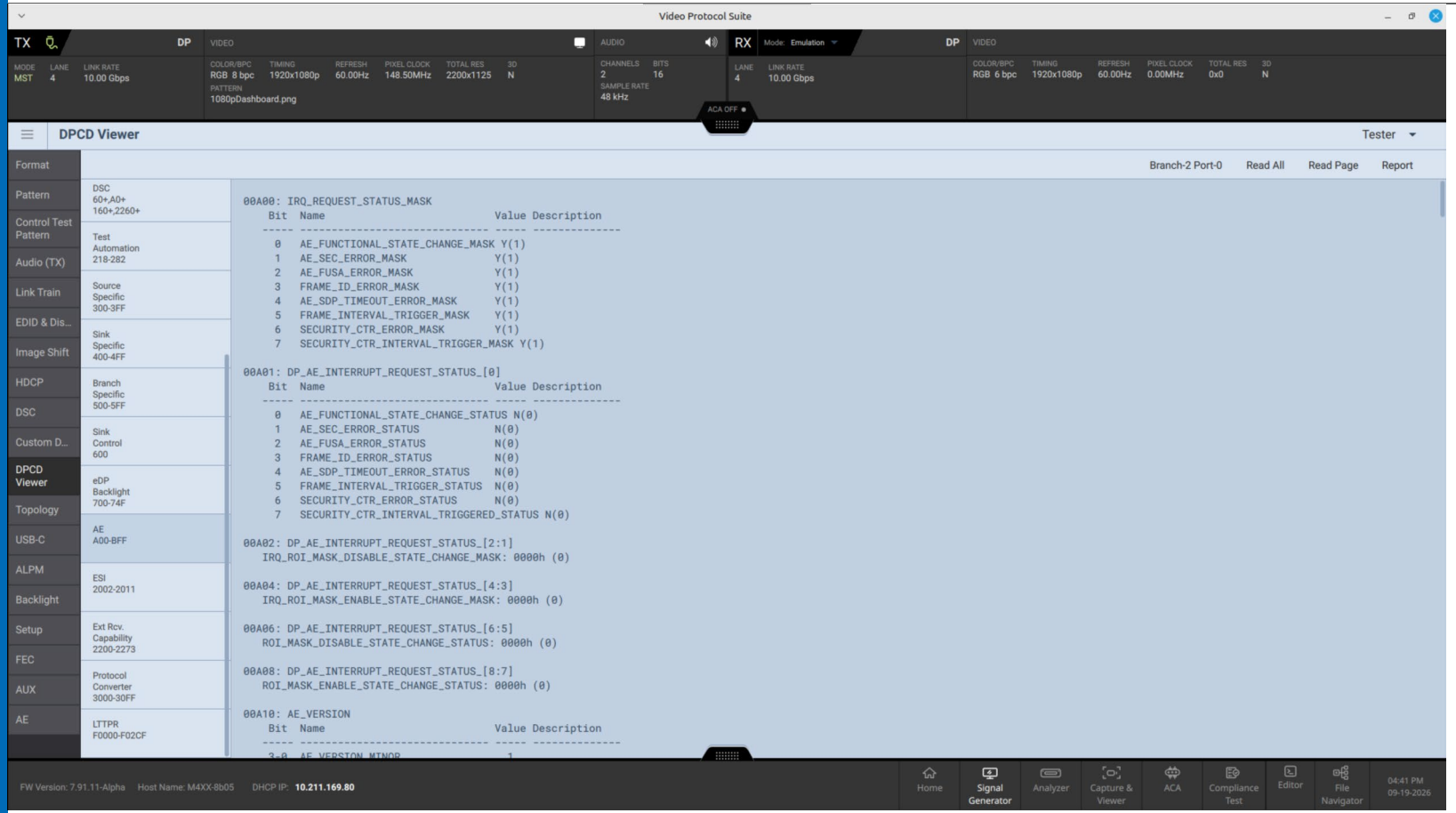
DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오 생성기 설정.

- 토폴로지, 스트림 수, 프로필 및 투자 수익률(ROI) 구성 등.
- 부차적 과정 선택.
- 관심 지역 설정 중.
- 오류 임계값 설정.
- **Sink DPCD DP AE 레지스터 보기.**
- 오류 주입.
- 자동차 확장 상태 보기.



DisplayPort AE – Testing Functional Safety

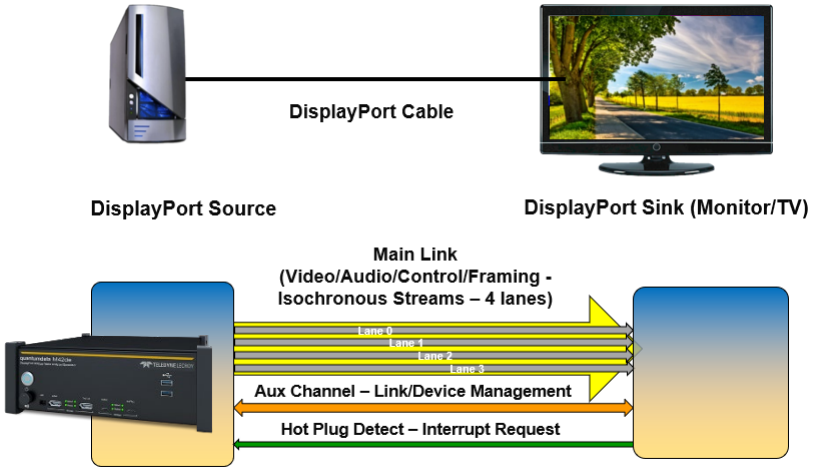


DisplayPort AE – 기능 안전 테스트

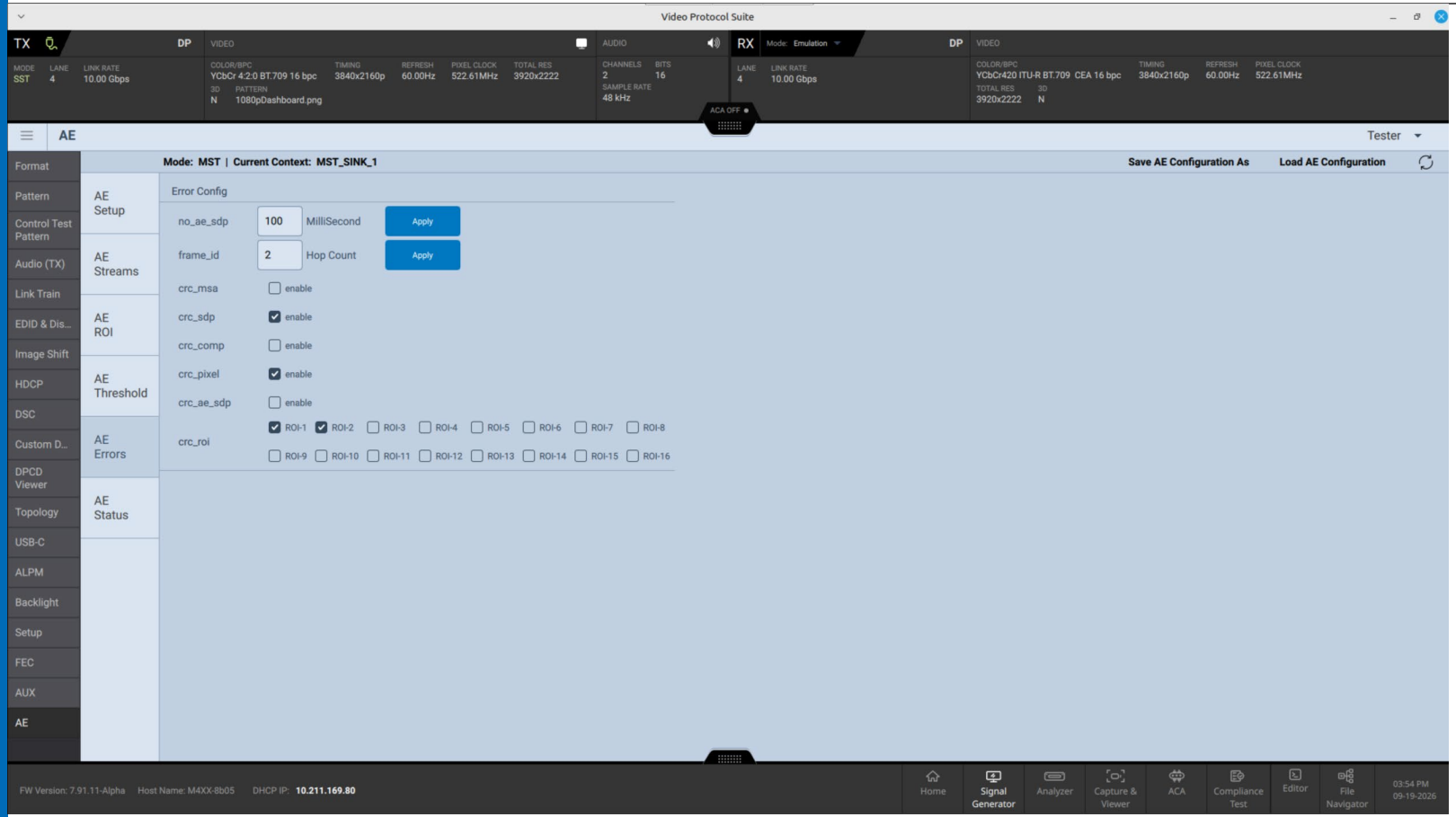
DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오 생성기 설정.

- 토폴로지, 스트림 수, 프로필 및 투자 수익률(ROI) 구성 등.
- 부차적 과정 선택.
- 관심 지역 설정 중.
- 오류 임계값 설정 중입니다.
- Sink DPCD DP AE 레지스터 보기.
- **주입 오류.**
- 자동차 확장 상태 보기.



DisplayPort AE – Testing Functional Safety

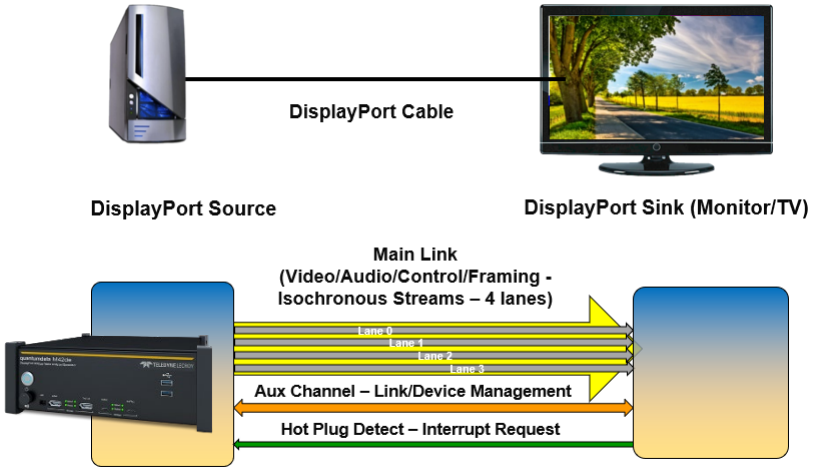


DisplayPort AE – 기능 안전 테스트

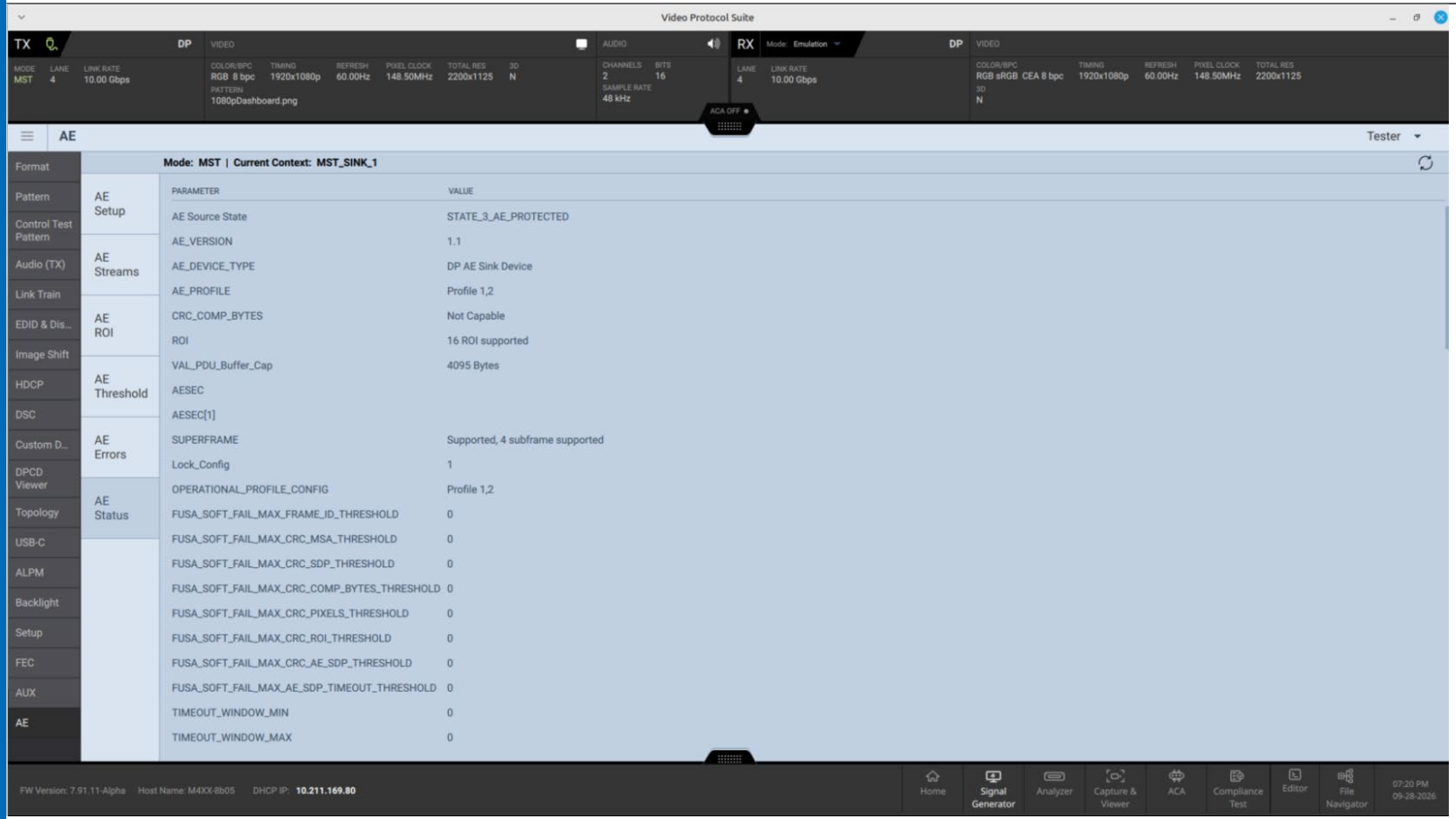
DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오 생성기 설정.

- 토폴로지, 스트림 수, 프로필 및 투자 수익률(ROI) 구성 등.
- 부차적 과정 선택.
- 관심 지역 설정 중.
- 오류 임계값 설정 중입니다.
- Sink DPCD DP AE 레지스터 확인.
- 주입 오류.
- **자동차 확장 상태 보기.**



DisplayPort AE – Testing Functional Safety



DisplayPort AE – 기능 안전 테스트

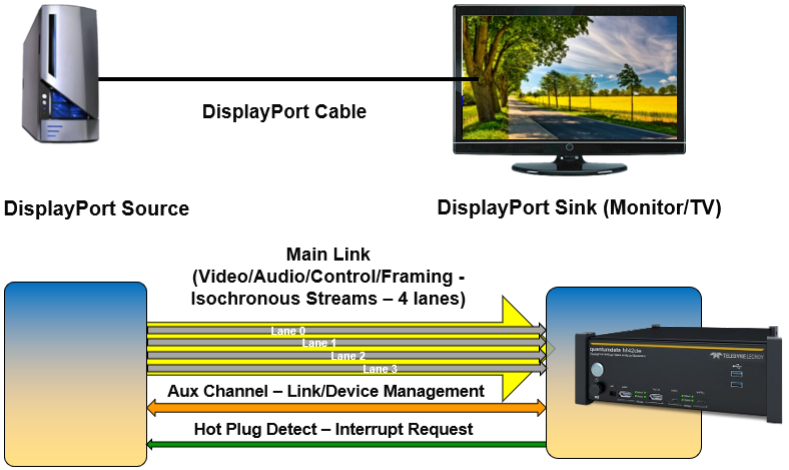
DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오/프로토콜 분석기 설정.

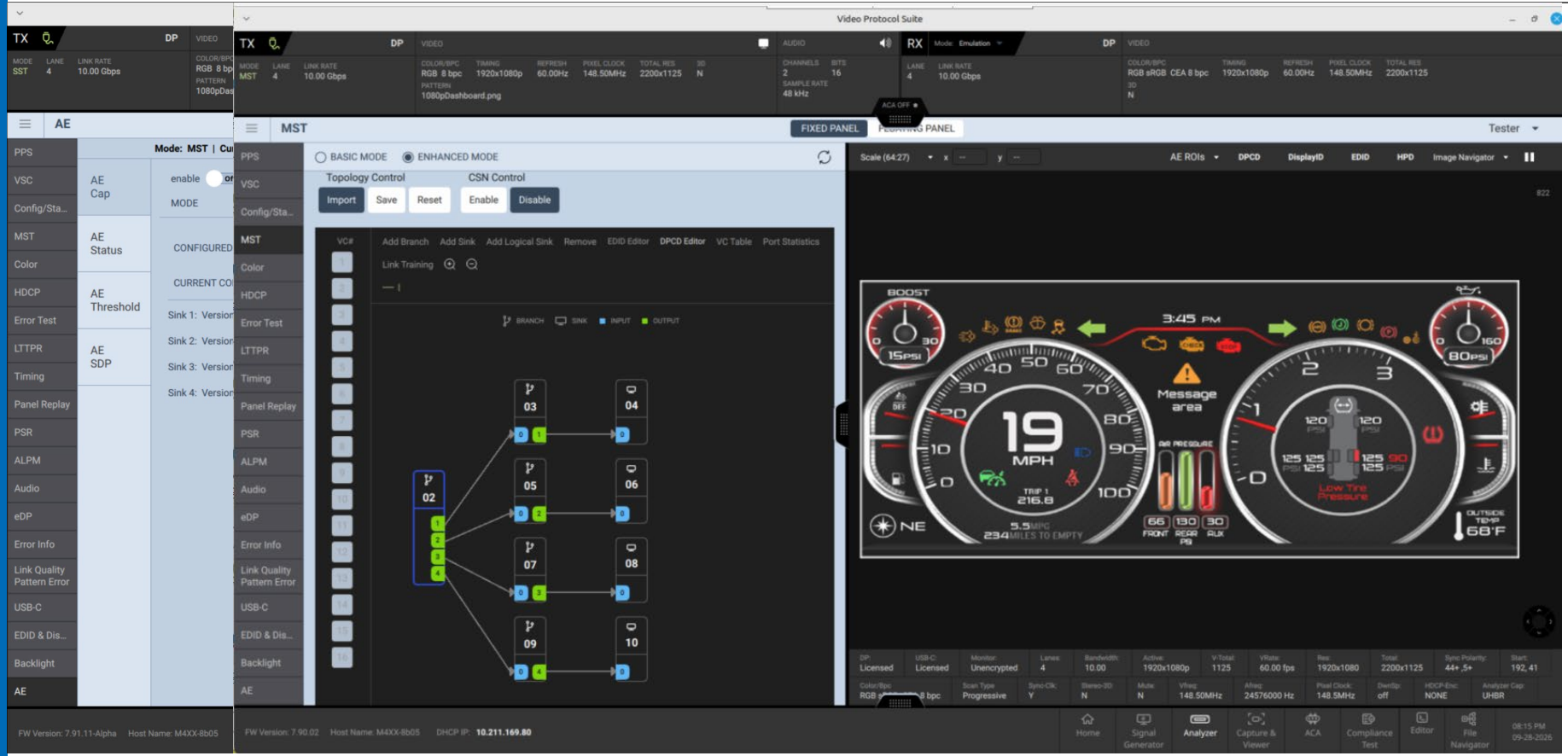
- **토폴로지, 프로필, 스트림 수 및 버전 구성.**

들어오는 DP AE 스트림 분석.

- 시청 상태.
- 보조 채널과 사이드밴드 거래 보기 중입니다.
- 실시간 DP AE 보조 데이터 패킷(SDP) 보기
- 들어오는 DP AE 스트림 캡처 및 분석.



DisplayPort AE – Testing Functional Safety



DisplayPort AE – 기능 안전 테스트

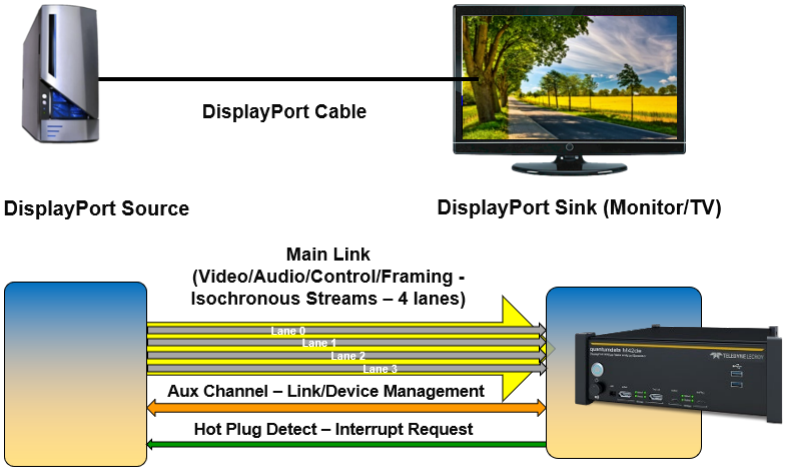
DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오/프로토콜 분석기 설정.

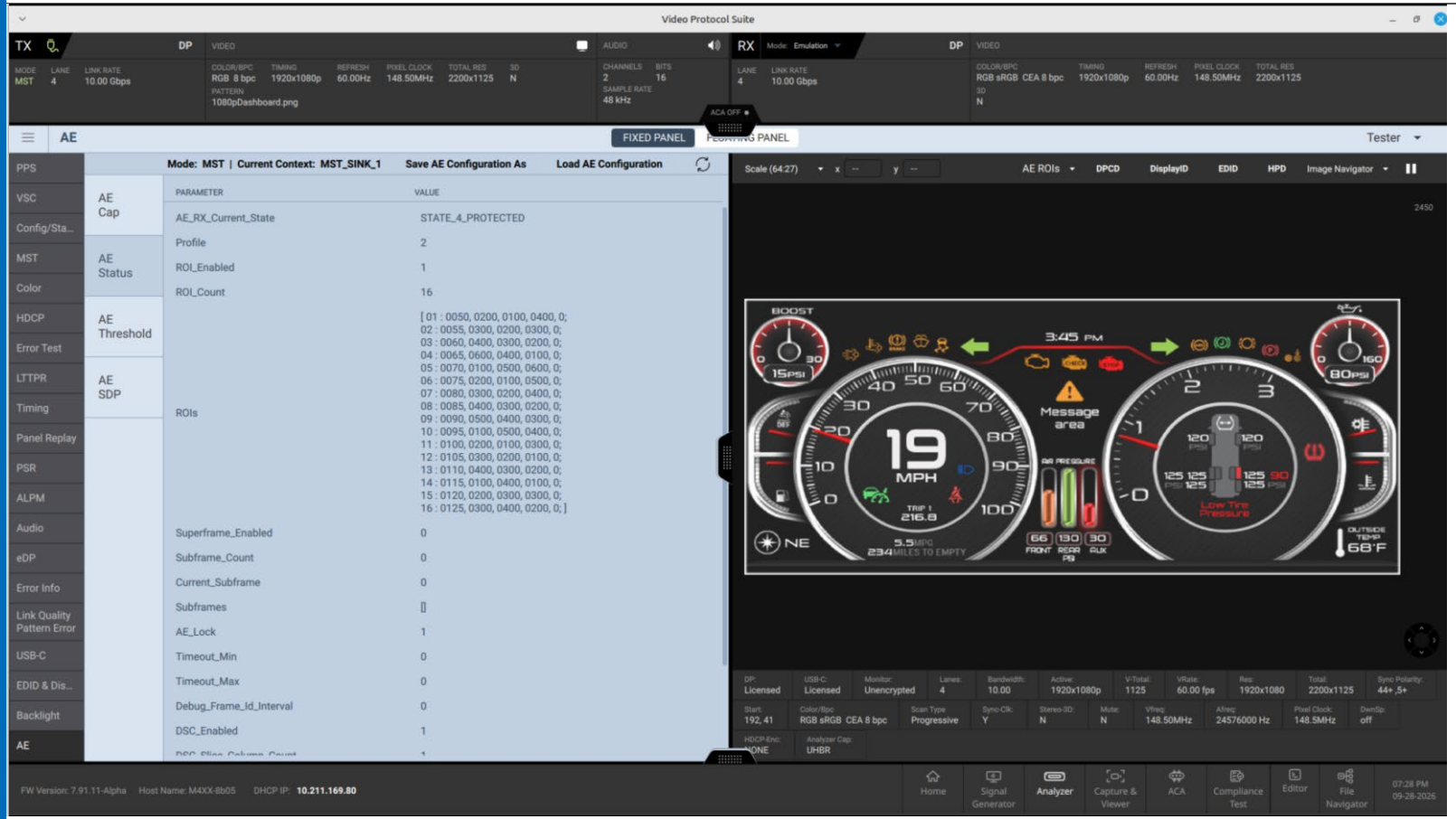
- 토폴로지, 프로필, 스트림 수 및 버전 구성.

들어오는 DP AE 스트림 분석.

- **시청 현황.**
- 보조 채널과 사이드밴드 거래 보기 중입니다.
- 실시간 DP AE 보조 데이터 패킷(SDP) 보기
- 들어오는 DP AE 스트림 캡처 및 분석.



DisplayPort AE – Testing Functional Safety



DisplayPort AE – 기능 안전 테스트

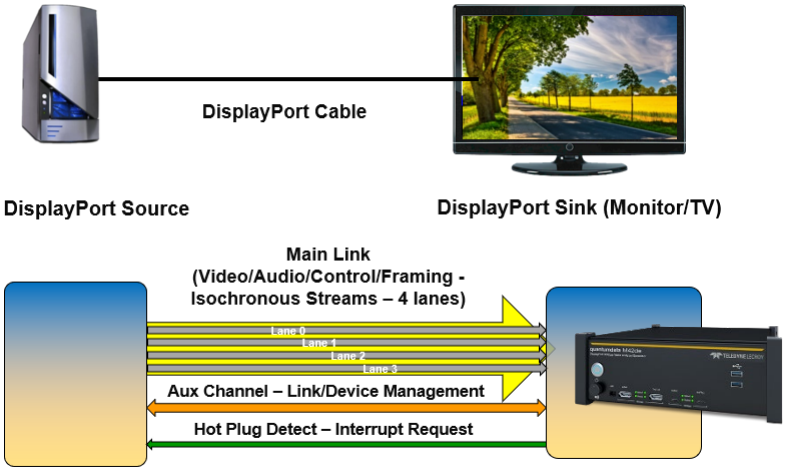
DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오/프로토콜 분석기 설정.

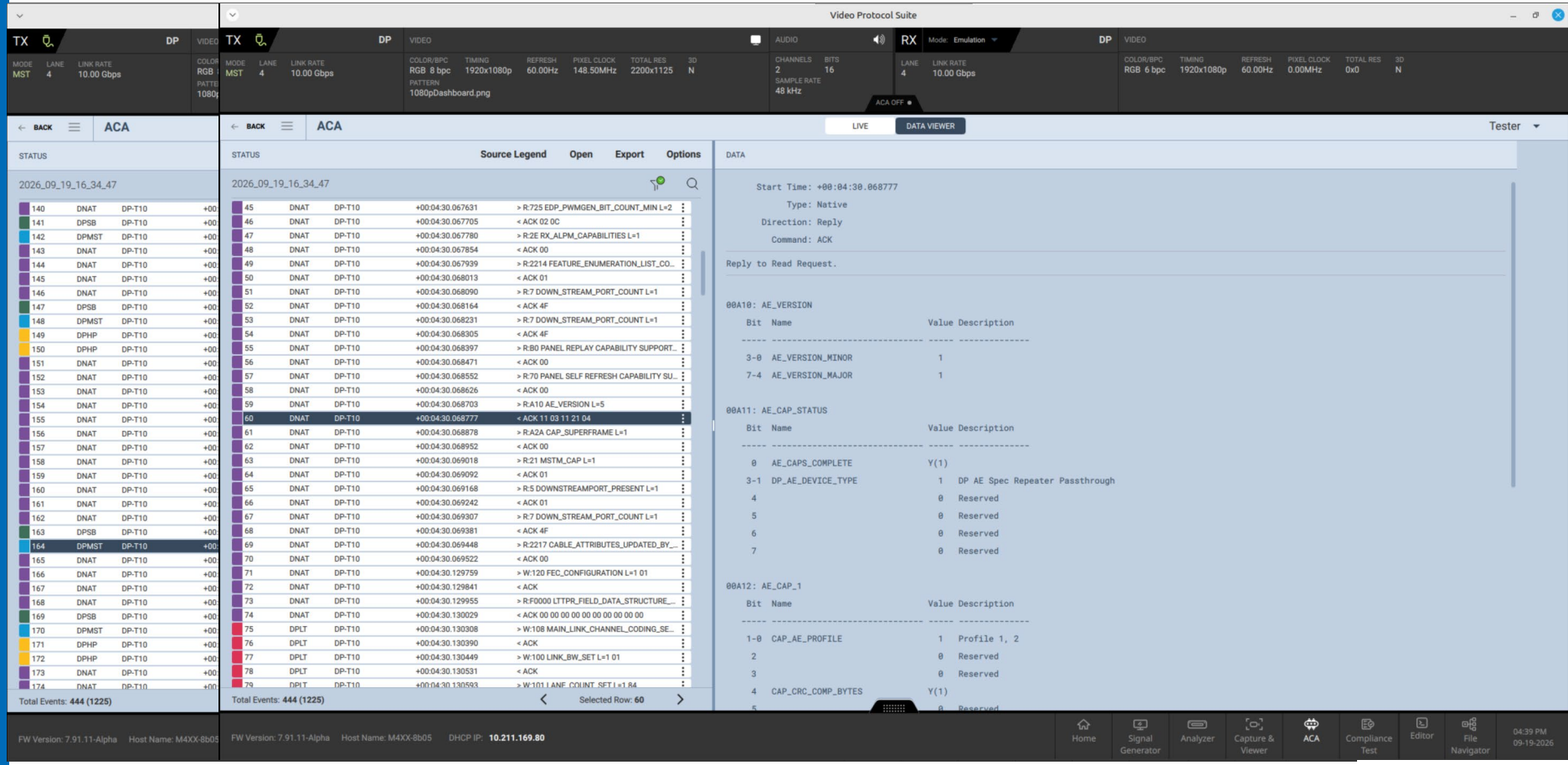
- 토폴로지, 프로필, 스트림 수 및 버전 구성.

들어오는 DP AE 스트림 분석.

- 시청 현황.
- **보조 채널 및 사이드밴드 거래 보기.**
- 실시간 DP AE 보조 데이터 패킷(SDP) 보기
- 들어오는 DP AE 스트림 캡처 및 분석.



DisplayPort AE – Testing Functional Safety



DisplayPort AE – 기능 안전 테스트

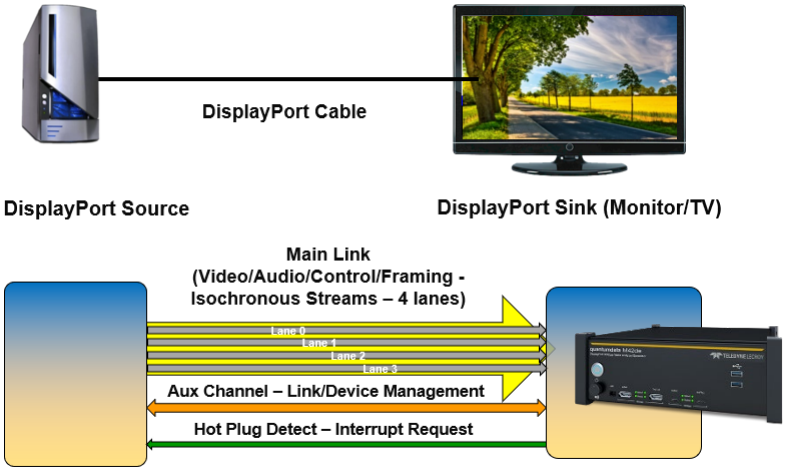
DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오/프로토콜 분석기 설정.

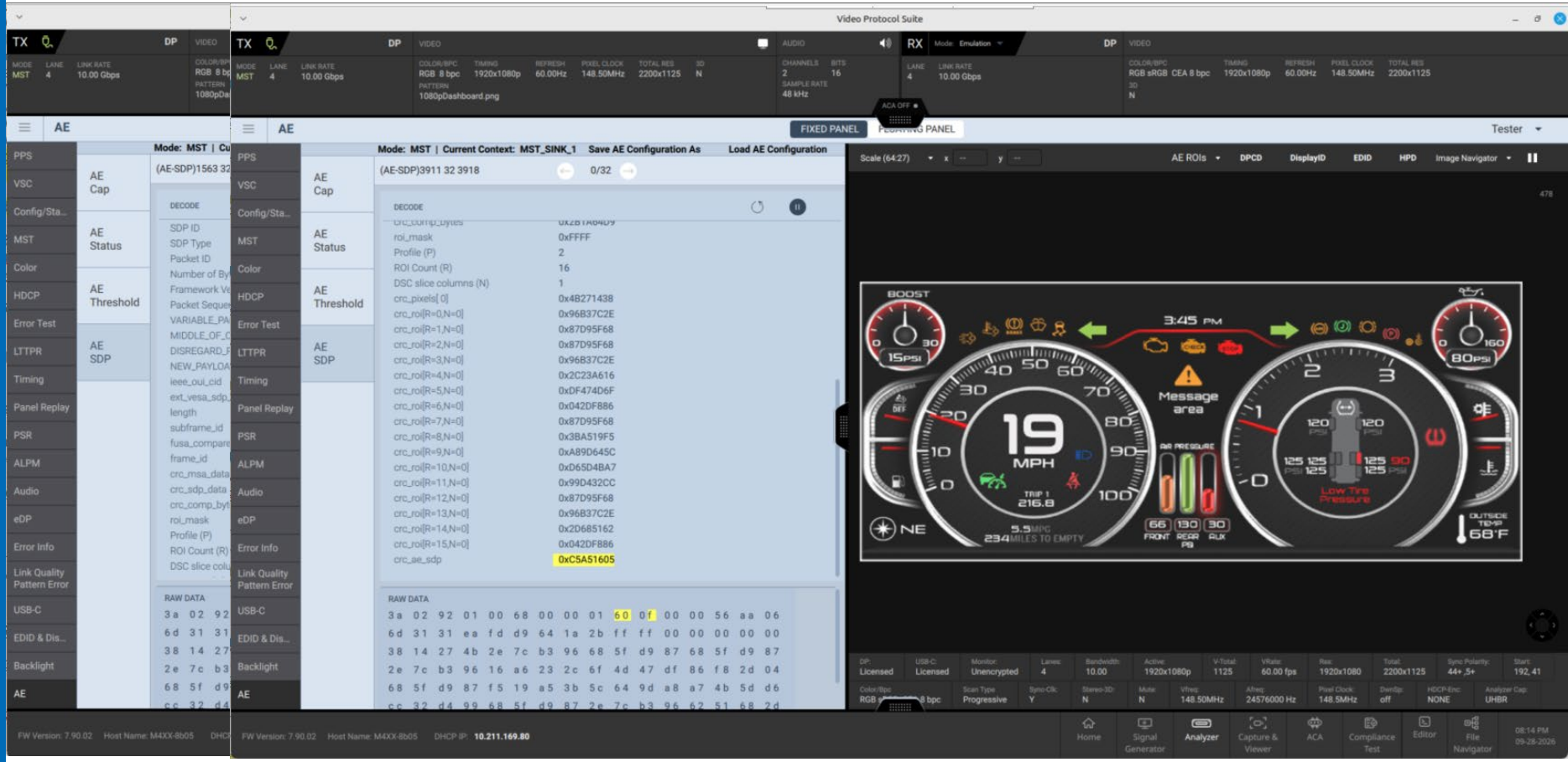
- 토폴로지, 프로필, 스트림 수 및 버전 구성.

들어오는 DP AE 스트림 분석.

- 시청 상태.
- 보조 채널 및 사이드밴드 거래 보기.
- **실시간 DP AE 보조 데이터 패킷(SDP) 보기**
- 들어오는 DP AE 스트림 캡처 및 분석.



DisplayPort AE – Testing Functional Safety



DisplayPort AE – 기능 안전 테스트

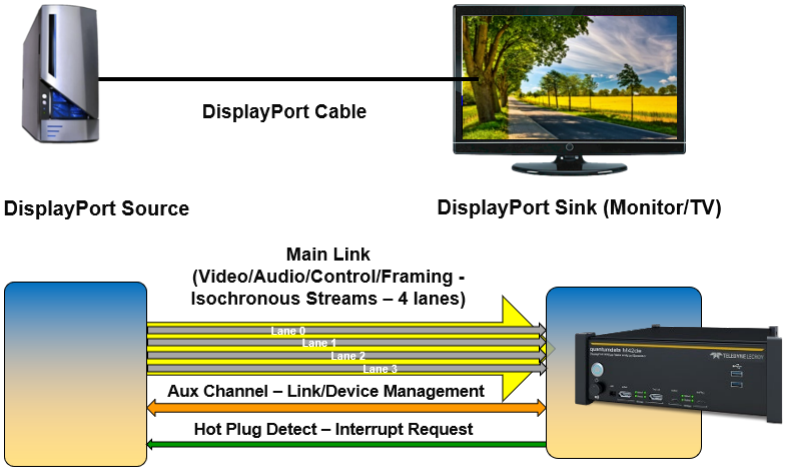
DisplayPort 자동차 확장 구현 테스트 방법

DP AE 비디오/프로토콜 분석기 설정.

- 토폴로지, 프로필, 스트림 수 및 버전 구성.

들어오는 DP AE 스트림 분석.

- 시청 상태.
- 보조 채널과 사이드밴드 거래 보기 중입니다.
- 실시간 DP AE 보조 데이터 패킷(SDP) 보기.
- **들어오는 DP AE 스트림을 캡처하고 분석하며 ROI 보기.**



DisplayPort AE – Testing Functional Safety



VESA 디스플레이포트 자동차 확장 (DP AE) 기능 안전 구현 테스트

Neal Kendall - Thank You!
Teledyne LeCroy
2026년 10월 12일 – 서울, 대한민국

VESA

DisplayPort Electrical Testing Overview

Mike Engbretson

Teledyne LeCroy Product Manager

10/12/2026

Agenda

- DP2.1 Electrical Compliance Test Requirements
- DP2.1 PHY Updates
- DP2.1 Transmitter Test
- DP2.1 Receiver Test
- DP2.1 PHY Vendor Methods of Implementation (MOIs)

DP2.1a Electrical Compliance Test Requirement

DisplayPort Interface

Main Link

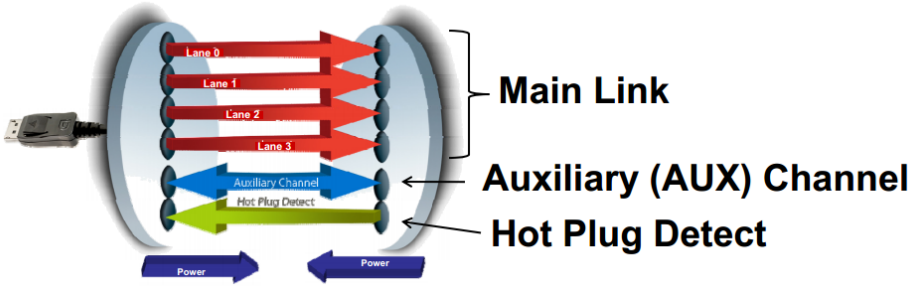
- Display data transfer
- 4 unidirectional high-speed lanes
- Multiple bitrates supported

AUX Channel

- Link management
- Test mode control
- 1 bidirectional low-speed lane

Hot Plug Detect

- Source detects presence of sink
- Sink notifies of status changes via IRQ



Test Points

Test Point	Definition
TP1	Source transmitter pins.
TP2	Test interface of a TPA, next to mated connection to a DP source.
TP2’	RX JTOL signal injection point for DUTs with plug.
TP2_CTLE	RX JTOL calibration and test point for DUTs with plug.
TP3	Test interface of a TPA, next to mated connection to a DP sink.
TP3’	Signal injection point to a DP sink.
TP3_EQ	TP3 using a defined DP cable model with equalization applied.’
TP3_CTLE	TP3 using a defined HBR3 cable model with CTLE applied.
TP3_DFE	TP3 using a defined HBR3 cable model with CTLE and DFE applied.
TP4	Sink receiver pins.

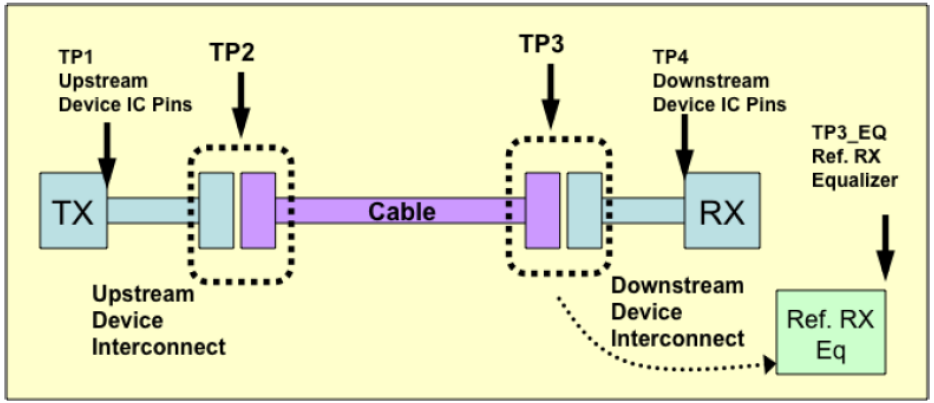


Figure 2-1: Ideal PHY Layer Measurement Points in a DP Interconnect System

Test Point Access Examples

DPTX Testing

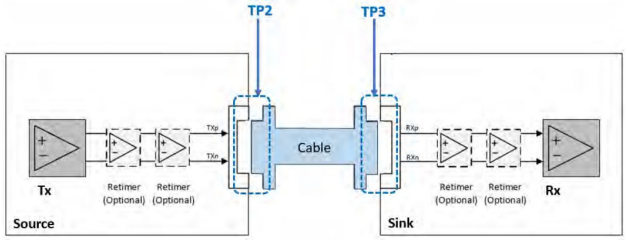
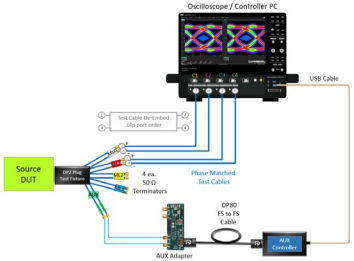
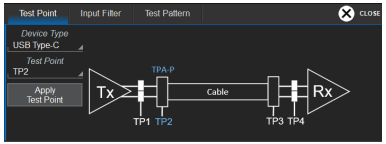
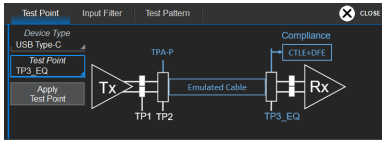


Figure 33. DisplayPort 2.1 Source Test Point definition.







DPRX Testing

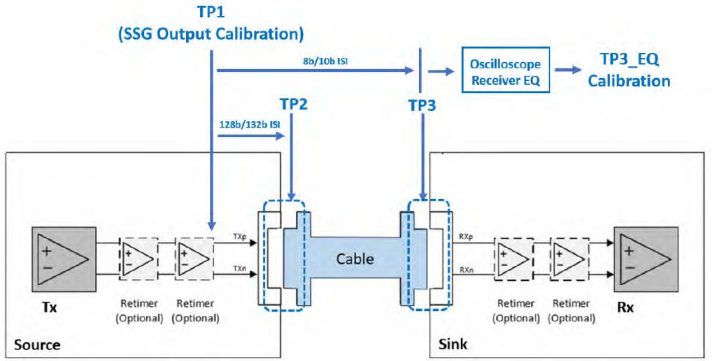


Figure 36. Test Point definition.

How to test the PHY layer?

Source

- Configure the source to output test patterns with certain drive settings → **AUX controller**
- Embed worst-case channels, apply equalization on the oscilloscope
- Run measurements

Sink

- Generate the stress signal with a pattern generator
- Guide the sink through Link Training → **AUX controller**
- Read built-in error counter → **AUX controller**

DP2.1 PHY Updates

Electrical Updates from DP2.1 to DP2.1a to DP2.1b

- There are minimal changes in 8b/10b electrical compliance testing.
- A new DP54 cable has been introduced in DP2.1a for UHBR13.5.
- The UHBR13.5 Source Enhanced FSDP testing will utilize the new DP54 cable model.
- A new DP80LL cable has been introduced in DP2.1b for UHBR20.
- The UHBR20 Source with 9dB loss budget will utilize the DP80LL cable.
- Addition of LRD test section
- Changes in test limits primarily affect Source Testing.

- UHBR10
  - DPTX TP2
    - Total Jitter =380 mUI
    - Data-Dependent Jitter =160 mUI
    - Eye Width = 600 mUI
    - Eye Height = 242 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 185 mV
  - DPTX TP3_EQ
    - Total Jitter =450 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 115 mV
  - DPRX TP3_EQ
    - Total Jitter =485 mUI
    - Data-Dependent Jitter =240 mUI
    - Eye Width = 540 mUI
    - Eye Height = 112 mV
- UHBR20
  - DPTX TP2
    - Total Jitter =435 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 240 mV
  - DPTX TP3_EQ
    - Total Jitter =455 mUI
    - Data-Dependent Jitter =210 mUI
    - Eye Width = 560 mUI
    - Eye Height = 100 mV
  - DPRX TP3_EQ
    - Data-Dependent Jitter =255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV



- UHBR10
  - DPTX TP2
    - Total Jitter =440 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 550 mUI
    - Eye Height = 162 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 200 mV
  - DPTX TP3_EQ
    - Total Jitter =515 mUI
    - Data-Dependent Jitter =245 mUI
    - Eye Width = 520 mUI
    - Eye Height = 80 mV
  - DPRX TP3_EQ
    - Total Jitter =530 mUI
    - Data-Dependent Jitter =260 mUI
    - Eye Width = 520 mUI
    - Eye Height = 73 mV
- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI

- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI



- UHBR20
  - DPTX TP2 EnhDP DP80
    - Total Jitter = 480 mUI
    - Data-Dependent Jitter = 200 mUI
    - Eye Width =540 mUI
    - Eye Height = 240 mV
  - DPTX TP2 EnhDP DP80LL
    - Total Jitter = 495 mUI
    - Data-Dependent Jitter = 220 mUI
    - Eye Width =530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ for all connector Type
    - Total Jitter = 500 mUI
    - Data-Dependent Jitter = 210 mUI
    - Eye Width =560 mUI
    - Eye Height = 100 mV
  - DPRX TP3EQ for all connector type
    - Data-Dependent Jitter = 255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV

DP2.1 PHY CTS Errata

- Clarification on 8b/10b SSC Modulation Deviation Limit
- Test fixture insertion loss update
- FFE Preset 15 measurement update
- LTTPR Frequency Variation test update
- Eye Height and Mask requirement update for UHBR Rates
- BERT Preset Calibration
- UHBR Source Return Loss (Normative)

DP2.1 Transmitter Test

Electrical Source-Tx Tests

Item	Name	Normative/ Informative
3.1	8b/10b DP Source Device Control and Capability	
3.2	Eye Diagram Test	Normative
3.3	HBR/RBR Non-PE Level Verification Test	Normative
3.4	HBR/RBR PE Level Verification and Maximum Differential Peak-to-Peak Voltage Test	Normative
3.5	HBR3/HBR2 PE Level and Equalization Verification Test	Normative
3.6	HBR3/HBR2 $V_{TX_DIFFp\text{-}p_MAX}$ Test	Normative
3.7	Inter-pair Skew Test	Informative
3.8	Intra-pair Skew Test	Informative
3.9	AC Common Mode Noise Test	Informative
3.10	Non-ISI Jitter Measurement Test	Normative
3.11	HBR3 TX Differential RL Test	Informative
3.12	TJ/RJ/DJ Measurement Tests	Normative
3.13	Main-Link Frequency Compliance Test	Normative
3.14	Spread-spectrum Modulation Frequency Test	Normative
3.15	Spread-spectrum Modulation Deviation Test	Normative
3.16	dF/dT Spread-spectrum Deviation High-frequency Variation Test	Informative
3.17	Embedded Re-timer Frequency Variation Test	Normative

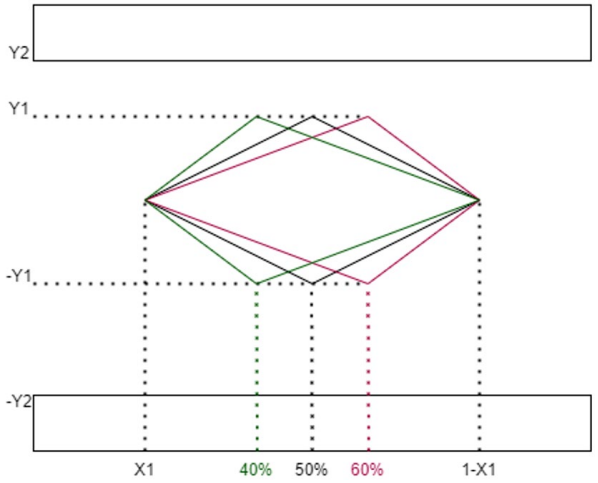
8b/10b

Item	Name	Normative/ Informative
4.1	UHBR Source Test Equipment Requirements	
4.2	Preset and CTLE-DFE Declaration	Normative
4.3	UHBR Source Transmitter Equalization	Normative
4.4	UHBR Bit Rate	Normative
4.4	UHBR Unit Interval	Informative
4.5	UHBR SSC Down Spread Range, Rate, Phase Deviation, and Slew Rate	Normative
4.6	UHBR Embedded Re-timer Frequency Variation	Informative
4.7	UHBR TP2 Eye at 1E-6 BER	Normative
4.8	UHBR TP2 Jitter at 1E-9 BER	Normative
4.9	UHBR AC Common Mode Nosie Test	Informative
4.10	UHBR TP3_EQ Eye at 1E-6	Normative
4.11	UHBR TP3_CTLE Jitter at 1E-9	Informative
4.12	UHBR Transmitter Return Loss	Normative

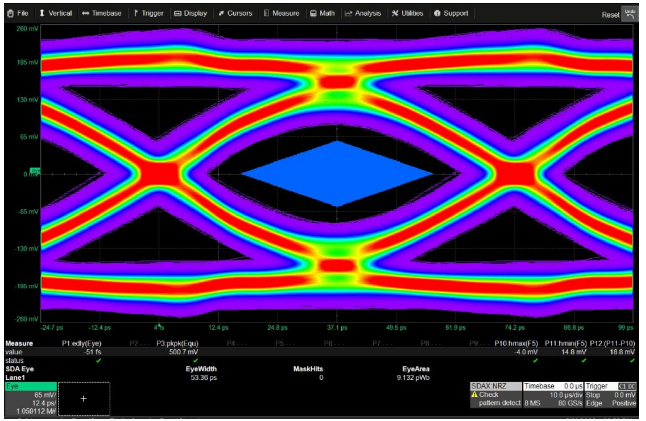
128b/132b

UHBR Eye Mask Update

- If original eye mask fails, then modified mask will be used to re-test.
- Modify mask must comply the Y1 and X1 as per the DP 2.1 PHY CTS



TE Vendor Specific MOI



LTTPR Frequency Variation Test

- LTTPRs are needed as total channel loss increases with the PHY rate
  - Longer channel
  - More complex link training
- LTTPR Re-timer Clock Switch Test Mode
  - DPCD 0x0010B – 0x0010Eh [7] =1
- Initial Test Challenges
  - **Entering** Clock Switch test mode
  - **Triggering** on LTTPR local clock event

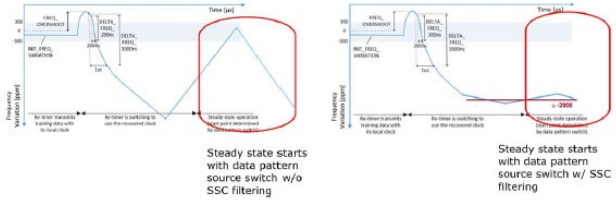
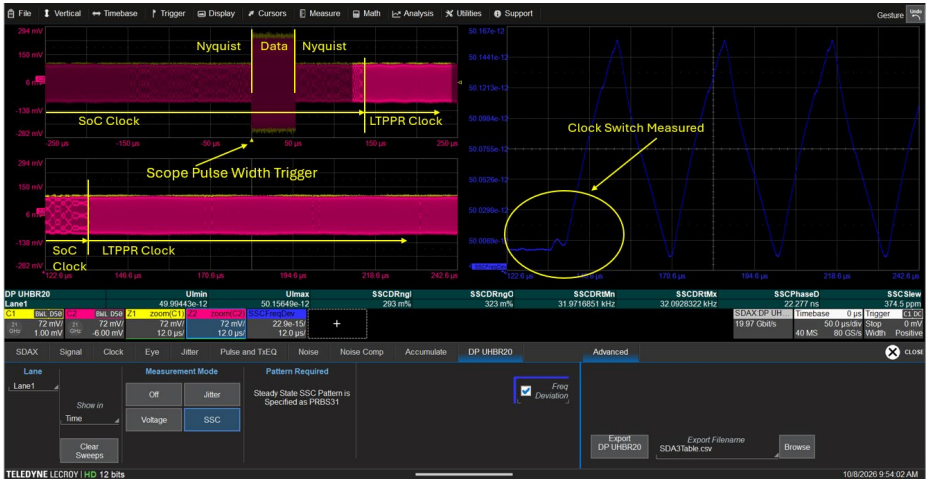


Figure 3-10: LTTPR SSC Filtering Examples

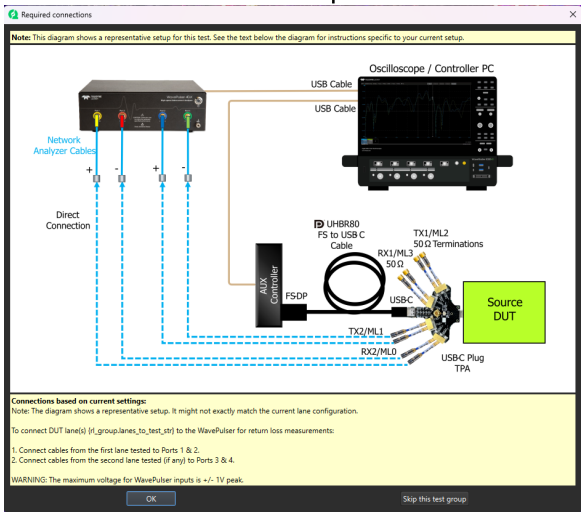
TE Vendor Specific MOI

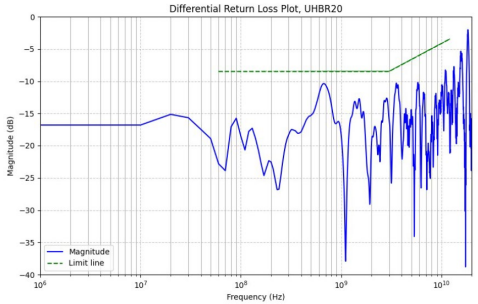


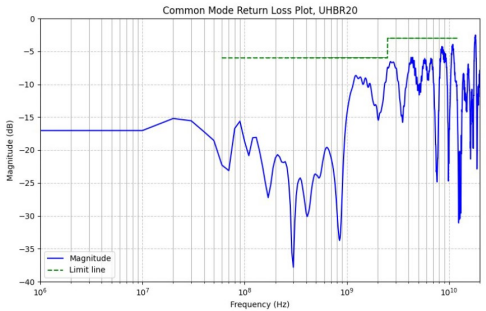
UHBR Tx Return Loss

- Normative requirement
- Vendor MOIs provide techniques for consistent P/F results

TE Vendor Specific MOI







DP Source-TX testing challenges

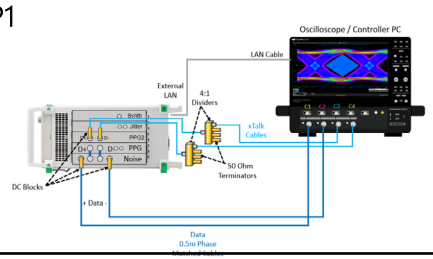
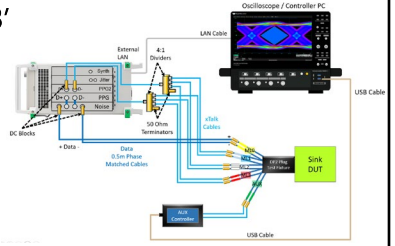
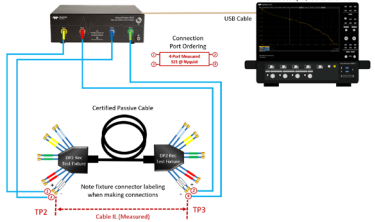
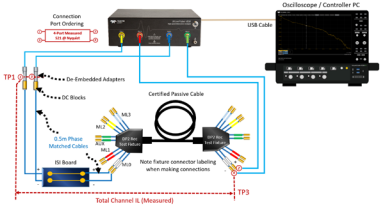
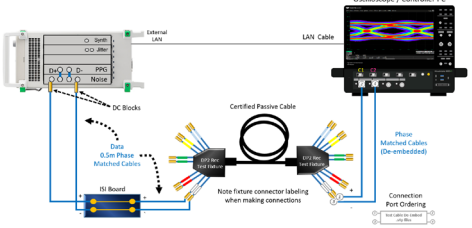
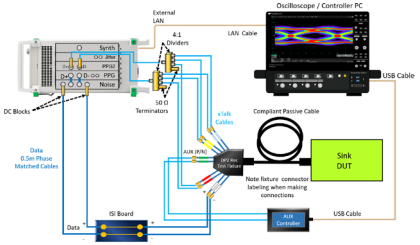
- The test time for DP TX is significant
- DP Source not supporting PHY Test Automation
  - DP Source does not transmit the compliance pattern
- VESA is currently discussing DP TX and DP RX reduced PHY test plan for reducing test time

DP2.1 Receiver Test

UHBR Sink-Rx Testing

- SSG Calibration
  - TP1
  - TP3
- Channel Calibration
  - TP2-TP3
  - TP1-TP3
- BER
  - TP3’ (Short Channel)
  - TP3 (Long Channel)

TE Vendor Specific MOI

Calibration	BER Test
TP1 	TP3’ 
TP2-TP3 Certified Cable 	TP1-TP3 Total Channel 
TP3 	

Electrical Receiver Tests

Item	Name	Normative/ Informative
5.1	8b/10b DP Sink JTOL Test	Normative

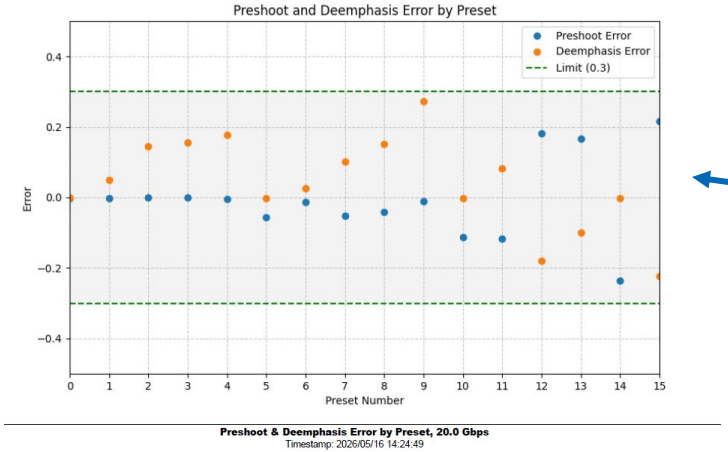
Item	Name	Normative/ Informative
6.1	128b/132b DP UHBR Sink JTOL Test	Normative

Item	Calibration Point	Name
5.1.3.1.1	TP1-TP3	HBR3 Jitter Calibration
5.1.3.1.2	TP1-TP3	HBR2 Jitter Calibration
5.1.3.1.3	TP1-TP3	HBR Jitter Calibration
5.1.3.1.4	TP2/TP3	HBR3 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR2 Eye Height and Total Jitter Calibration
5.1.3.1.4	TP3	HBR Eye Height and Total Jitter Calibration
5.1.3.1.5	TP1/TP3	HBR3/HBR2/HBR Crosstalk Calibration
5.1.3.2	TP2/TP3	RBR Jitter Calibration
5.1.3.2	TP3	RBR Eye Height Calibration
5.1.3.2.1	TP3	RBR Crosstalk Calibration

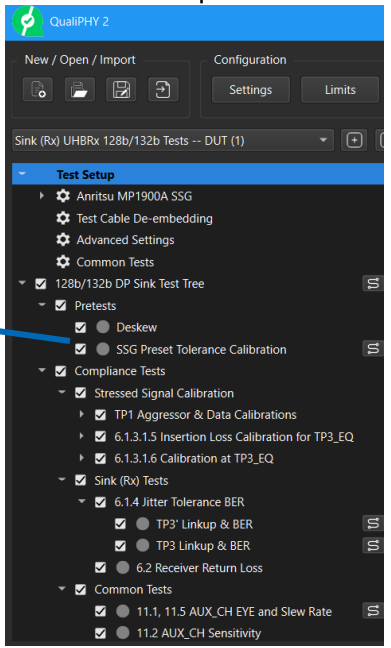
Item	Calibration Point	Name
6.1.3.1.4.1	TP1	AC Common-Mode Interference Calibration
6.1.3.1.4.2	TP1	Random Jitter Calibration
6.1.3.1.4.3	TP1	Periodic Jitter Calibration
6.1.3.1.4.4	TP1	Total Jitter Calibration
6.1.3.1.4.5	TP1	Eye Height Calibration
6.1.3.1.5	TP3	Insertion Loss Calibration
6.1.3.1.6	TP3	Eye Diagram Calibration

SSG Preset Calibration

- To verify the SSG FFE as outlined in the DP 2.1 PHY CTS specification
- The Preset calibration check can assist in identifying setup problems.



TE Vendor Specific MOI



SSG – Stressed Signal Generator

DP Sink-Rx testing challenges

- Error count registers not enabled in DP Sink
  - Error count register always report 0 errors
  - USB-C Lane orientation causing failure in error counter and link training
- Calibrations take a significant amount of time
  - Different setup needs for 8b/10b and 128b/132b

Vendor MOI Process

Vendor Specific Methods of Implantation (MOIs)

- Submitted by TE vendors to Test Implementation Working Group
- Reviewed by WG members
- General Member Review (GMR)
- Approved and posted at https://vesa.org/authorized-test-tools/

VESA

Thank You!

DisplayHDR & Adaptive-Sync Display CTS

DoKyun Kim (keneth.kim@lge.com)
SeungHyun Yoo (seunghyun.yoo@lge.com)
LG Electronics, Inc.

12 Oct 2026

Agenda

01 **VESA Display Performance Metrics Standards**
Scope / Key Metrics

02 **DisplayHDR CTS 1.2**
Overview / Test

03 **Adaptive-Sync Display CTS 1.1a**
Overview / Test

04 **What is the Next?**

PART 01

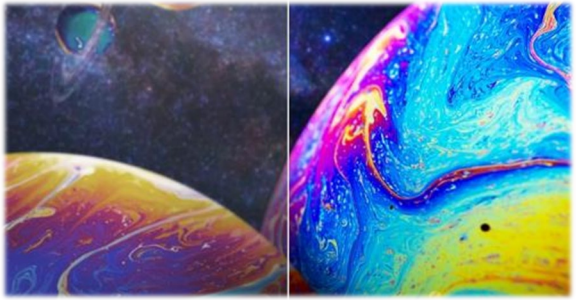
VESA Display Performance Metrics Standards

Scope / Key Metrics

VESA Display Performance Metrics (DPM) Group

VESA CERTIFIED DisplayHDR™

- ✓ Brightness, Black and contrast
- ✓ Accurate color reproduction



VESA CERTIFIED AdaptiveSync

- ✓ Static/ Variable refresh rate performance
- ✓ Tearing / stutter check



VESA CERTIFIED ClearMR

- ✓ Motion response speed
- ✓ Clear-to-blurry pixel ratio



VESA Display Certification Standards Timeline

2023 Oct

ClearMR CTS r1.1

· Tool improvements

2024 Jan

Adaptive-Sync Display CTS r1.1a

· Dual Mode certification added

2024 Apr

DisplayHDR CTS r1.2

· Color test enhanced
· Test range expanded

2025 Jan

ClearMR CTS r1.1

· New tier 15,000-21,000

2026 Jul

DisplayHDR CTS r1.2 SCR

· True Black 1400 added

2026 Sep

Adaptive-Sync Display CTS r1.1

· HDMI-only products eligible

Global market Certified products per year	2023	2024	2025
DisplayHDR	397	556	780
ClearMR	45	53	115
AdaptiveSync	80	75	146

* Source: VESA Annual Meeting 2025

Certification Logos in Product Marketing



DisplayHDR

World's 1st certified gaming monitor



VESA AdaptiveSync

Tear-free, motion-clear gameplay

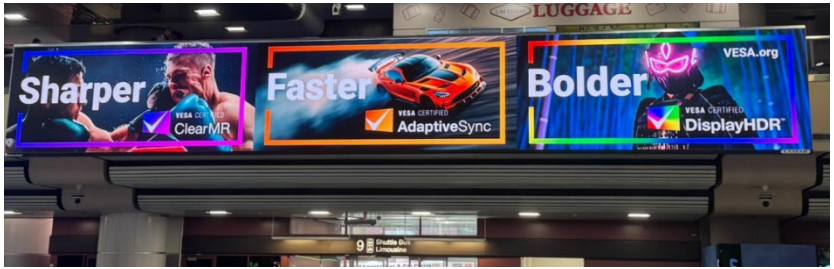


ClearMR

UltraGear OLED GX7, 480Hz

* Source: LGE.co.kr

VESA DPM Promotion at CES 2026



Airport digital signage · ClearMR / AdaptiveSync / DisplayHDR campaign



VESA Certified ClearMR demo



DPM live demo station









VESA suite · member & press demo sessions and technical briefings

DPM logos actively promoted at CES 2026 — airport signage and live demos in the VESA suite

* Source: VESA Marketing Group

VESA Adaptive-Sync Certification Process

If the ATC and in-house Self-Test results of two reference models match, the VESA CPM grants Self-Certification qualification

STEP 1 Qualify for self-certification

1. **Reference models #1 / #2 — official ATC test**
2. **In-house Self-Test on the same criteria**
   Results secured for both reference models
3. **VESA CPM review**
   ATC vs. Self-Test results compared for both models

Qualification granted when the CPM confirms the two sets of results agree
CPM : Compliance Program Manager

STEP 2 Certify follow-up models

Self-Certification qualified

1. Follow-up model · new / derivative products
2. VESA certification request · submit test results

✓ **Certification granted**
Model listed on the VESA certified product list

PART 02

DisplayHDR

Overview / Test

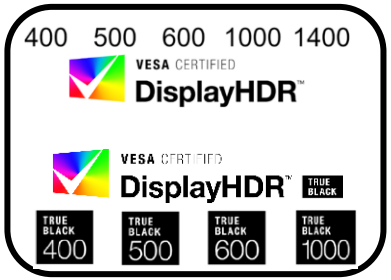
DisplayHDR CTS

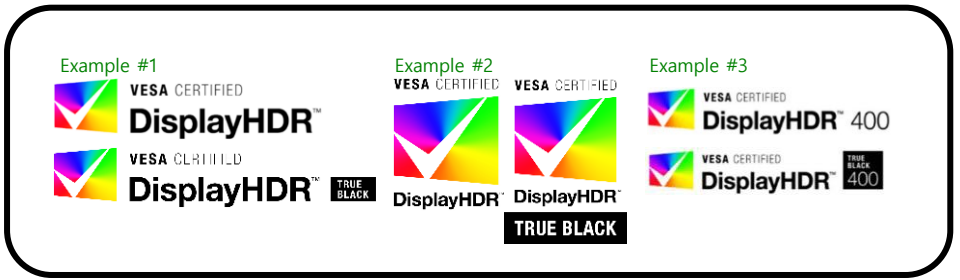
Tier / Logo – Tiers (400, 500, 600, 1000, 1400, True Black) are defined by luminance and black-level performance











HDR Tone Mapping

HDR metadata describes the content; tone mapping adapts it to what the display can show

1 HDR Metadata

Brightness information carried with the content

MASTERING RANGE / MaxCLL / MaxFALL

"This is how bright the content was designed to be."

It only describes the content — it does not change the picture

2 Tone Mapping

The display remaps that brightness range into its own output range



Certified Product Specifications (1/2)

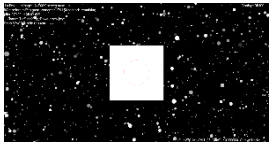
Test / Specification	DisplayHDR					DisplayHDR TrueBlack				
	400	500	600	1000	1400	400	500	600	1000	1400
Min. white luminance · 8% center patch · Min (cd/m²)	400	500	600	1000	1400	400	500	600	1000	1400
8% center patch · Min–Max deviation	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%
Full-screen flash test · Min (cd/m²)	400	500	600	1000	1400	250	300	350	500	700
Full-screen long duration · Min (cd/m²)	320	320	350	600	900	250	300	350	500	700
Dual corner box · Screen center · Max (cd/m²)	0.4	0.1	0.1	0.05	0.02	0.0005	0.0005	0.0005	0.0005	0.0005
Both white corners · Min (cd/m²)	300	375	450	750	1050	300	375	450	750	1050
Active dimming · Log_2(8% white / 5 nit black) / $Log_2$2	11	11.6	12	13	13.5	N/A	N/A	N/A	N/A	N/A
Log_2(8% white / 50 nit black) / $Log_2$2	12	12.6	13	14	14.5	N/A	N/A	N/A	N/A	N/A
Checker board · Checkerboard black level at max EDID white luminance	N/A	N/A	N/A	N/A	N/A	0.0005	0.0005	0.0005	0.0005	0.0005
Color gamut · ITU-R BT.709 – 8% and full screen	99%	99%	99%	99%	99%	99%	99%	99%	99%	99%
DCI-P3 CIE D65 – 8% and full screen	90%	95%	95%	95%	95%	95%	95%	95%	95%	95%
RGB combined color luminance – 8%	400	500	600	1000	1400	400	500	600	1000	1400
RGB combined color luminance – full screen	320	320	350	600	900	250	300	350	500	750
Min. bit-depth · 10-bit video signal, per channel	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Temporal or spatial dithering	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC	8b + 2b FRC
Minimum 8-bit digital-to-analog	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Backlight control 8-bit accuracy	✓	✓	✓	✓	✓	N/A	N/A	N/A	N/A	N/A
Rise time · Luminance 10% → 90% at 60 Hz	8 Frame	8 Frame	8 Frame	8 Frame	8 Frame	2 Frame	2 Frame	2 Frame	2 Frame	2 Frame

Certified Product Specifications (2/2)

Test / Specification	DisplayHDR					DisplayHDR TrueBlack				
	400	500	600	1000	1400	400	500	600	1000	1400
White point accuracy · Delta-ITP error · ≤ 5 cd/m²	20	20	20	20	20	20	20	20	20	20
Delta-ITP error · 15 cd/m²	15	15	15	15	15	15	15	15	15	15
50 / 100 / 200 cd/m², 50% & 100% tier level	10	10	10	10	10	10	10	10	10	10
Static contrast ratio · 1D test pattern	13000:1	70000:1	80000:1	N/A	N/A	N/A	N/A	N/A	N/A	N/A
2D test pattern	N/A	N/A	N/A	30K:1	50K:1	N/A	N/A	N/A	N/A	N/A
Black HDR vs SDR · HDR C/R > SDR C/R × 0.9	>90%	>90%	>90%	>90%	>90%	>90%	>90%	>90%	>90%	>90%
Black level crush · Required number of distinct shadow levels	5	5	5	5	5	5	5	5	5	5
Subtitle flicker · 10 cd/m² max brightness vs subtitle presence	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%
X-Rite Color 96 Delta-ITP · 50 cd/m²	8	8	8	6	6	8	8	8	6	6
100 cd/m²	8	8	8	6	6	8	8	8	6	6
50% of DisplayHDR logo	8	8	8	6	6	8	8	8	6	6

Luminance Performance Test

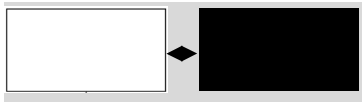
1. 8% Patch



How to measure 8% white patch, at screen center

Min 400–1400 cd/m² by tier

2. Full-screen Flash



How to measure White 2 s / Black 10 s, ×5

Min 400–1400 (TB 250–700)

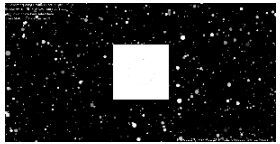
3. Long-duration



How to measure Full-screen white, 1/min for 30 min

Min 320–900 cd/m²

4. White Delta accuracy

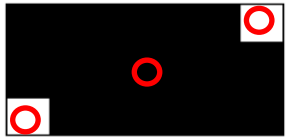


How to measure 8% patch, 6 levels → Delta-ITP

Delta-ITP ≤ 20 / 15 / 10

Black Level / Contrast Ratio Test

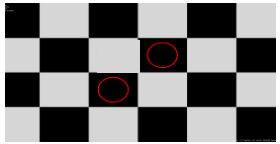
5. Dual Corner Box



How to measure Center + 5% corners, ≤10 s

Center ≤ 0.4–0.0005 cd/m²

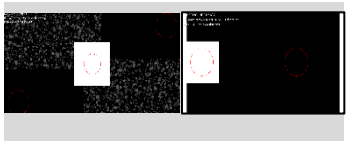
6. Checker board



How to measure Average of two center black squares

TrueBlack ≤ 0.0005 cd/m²

7. Static Contrast Ratio



How to measure 1D / 2D dimming patterns

13,000:1 – 80,000:1

8. Black Level Crush



How to measure 5 near-black levels

5 levels distinguishable

Color Test

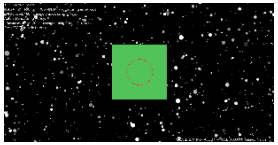
1. Color Gamut



How to measure Full-screen & 8% R/G/B, CIE x/y/Y

BT.709 99% / DCI-P3 90–95%

2. Xrite 96color



How to measure 96 patches at 3 luminance levels

Delta-ITP ≤ 8 (1000/1400: 6)

HDR Performance Test

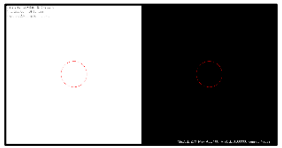
3. Rise-time Sequence



How to measure Black 5 s / patch 5 s, 10→90%

≤ 8 frames (TB ≤ 2 frames)

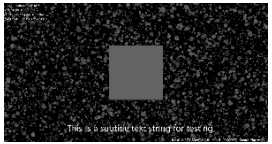
4. HDR vs. SDR Black Level



How to measure Measure CR in HDR & SDR (PQ 592)

CR(HDR) ≥ 0.9 × CR(SDR)

5. Subtitle Flicker



How to measure Gray patch min/max, subtitle ON/OFF

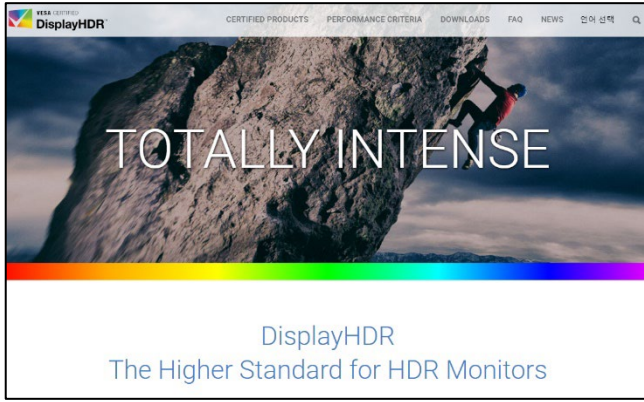
Flicker ≤ 10%

Certified Products

Cumulative

Tier	2024.10	2025.10	2026.10	Growth vs 2025
DisplayHDR 400	714	885	980	10.7%
DisplayHDR 500	18	31	39	25.8%
DisplayHDR 600	101	132	152	15.2%
DisplayHDR 1000	126	164	179	9.1%
DisplayHDR 1400	12	22	37	68.2%
DisplayHDR True Black 400	89	167	205	22.8%
DisplayHDR True Black 500	194	282	357	26.6%
DisplayHDR True Black 600	65	123	138	12.2%
DisplayHDR True Black 1000	0	33	146	342.4%
DisplayHDR True Black 1400	0	0	2	X
SUM	1319	1839	2235	21.5%

Excluding Family models



https://displayhdr.org/

PART 03

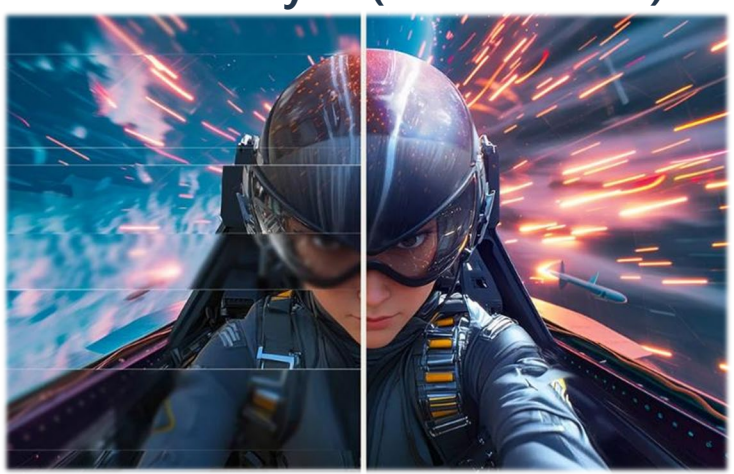
Adaptive-Sync Display CTS 1.1a

Overview / Test

Adaptive-Sync Display CTS

Tier / Logo – AdaptiveSync (Max ≥ 144 Hz, Min ≤ 60 Hz)

MediaSync (Max ≥ 60 Hz)





VESA CERTIFIED AdaptiveSync
Gaming

VESA CERTIFIED MediaSync
Broadcast video

Example #1
VESA CERTIFIED AdaptiveSync

Example #2
VESA CERTIFIED AdaptiveSync DISPLAY 144
Refresh Rate Display

Example #3
VESA CERTIFIED AdaptiveSync DISPLAY 144 2160P | DISPLAY 280 1080P
Dual Mode

Example #4
VESA CERTIFIED MediaSync

VESA CERTIFIED MediaSync DISPLAY
'Display' label shown

VRR synchronizes the display with the GPU to prevent tearing

Why does the image split horizontally?

① Display scans top to bottom

A frame is not shown all at once; it is scanned in order from top to bottom

② GPU swaps frame mid-scan

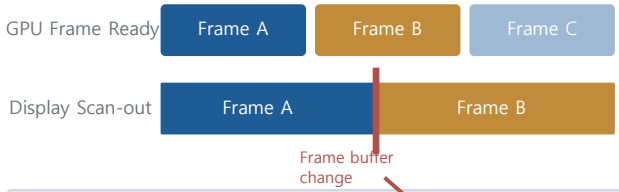
After the top is scanned, a new frame arrives with the car moved right

③ Two moments in one frame

Top = previous car position
Bottom = next car position

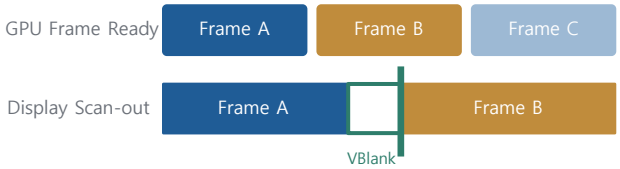
V-Sync OFF

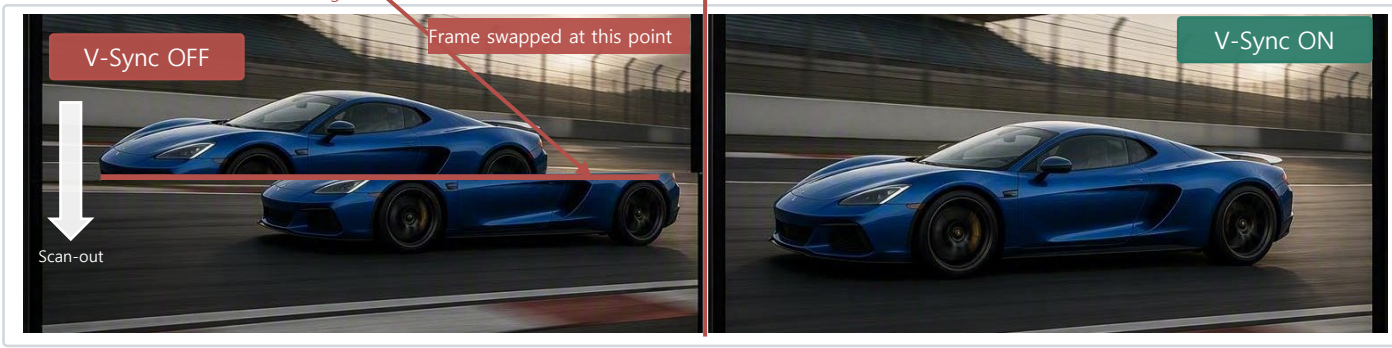
Frame updates are not synchronized with scan-out



V-Sync ON

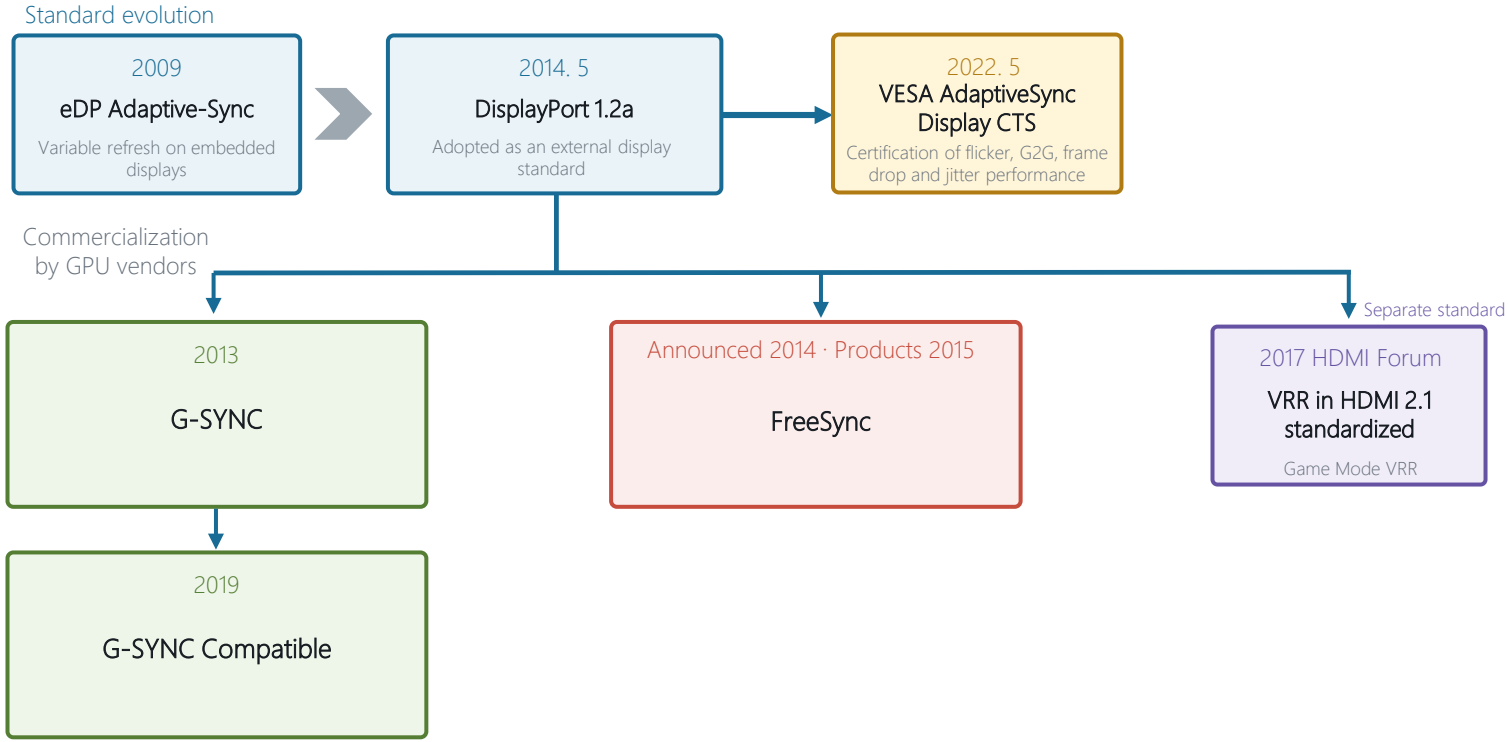
Frame updates are synchronized to VBlank



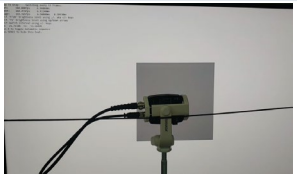
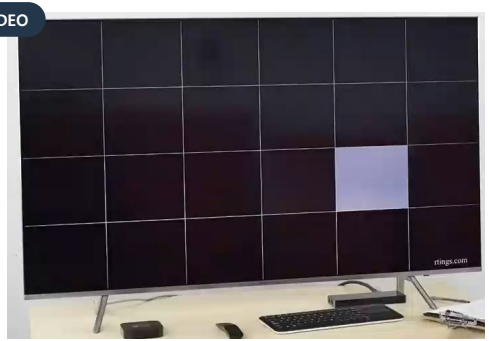
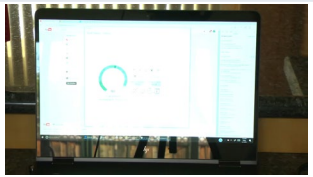


Adaptive-Sync History

VESA Adaptive-Sync-based GPU ecosystem expansion



Phenomenon & Measurement Setup by Test Item

Test Item	Phenomenon / Pattern	Measurement Setup
Flicker Brightness flicker caused by refresh rate changes Color Meter (CA-410)	▶ VIDEO 	
Gray to Gray Pixel transition delay and ghosting Photo Sensor, DAQ, PC		▶ VIDEO 
Frame Drop Frame loss during VRR operation DSLR Camera	▶ VIDEO 	▶ VIDEO 
Jitter Frame display interval non-uniformity DSLR Camera	▶ VIDEO 	

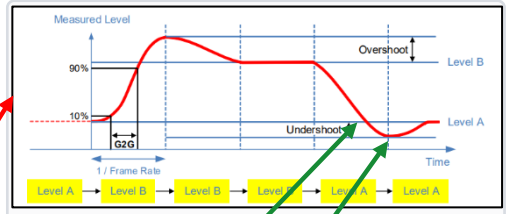
Tier Certification Criteria

1 Tier Performance Requirements

Evaluation Item	AdaptiveSync	MediaSync
Refresh Rate	Max ≥144 Hz Min ≤60 Hz	Max ≥60 Hz Min ≤48 Hz
Flicker	Static Low / High variation each ≤ -50 dB	Static Low var. ≤ -50 dB High var. N/A
G2G Response Time	Avg. ≤5 ms	No requirement
G2G Over / Undershoot	ΔPQ limit per range	ΔPQ limit per range
Frame Drop	0	0
Frame-to-Frame Jitter	±0.5 ms	±0.5 ms
Operation in HDR	HDR supported	HDR supported

Test sequence: Refresh Rate → Flicker → G2G → Frame Drop → Jitter → HDR operation

2 G2G Over / Undershoot ΔPQ Calculation



Level A Luminance
8.56 cd/m²
PQ 294

Undershoot minimum
5.56 cd/m²
PQ 261

Undershoot ΔPQ
$PQ_{Level\ A} - PQ_{Dip}$
294 - 261 = 33

Level A : reference level for the undershoot dip evaluated by PQ difference, not by absolute luminance ratio

PQ Code Value : luminance converted to match human brightness perception (0–1024)

Test Pattern

1. Flicker Test



How to measure Static and dynamic VRR patterns, 23.976–60 Hz

40 cd/m² ±5% (38–42)

2. G2G Test



How to measure 64 transitions, Gamma 2.2 / SDR

Avg. G2G ≤ 5 ms

3. Frame Drop Test



How to measure Moving white box, 1 sec. traversal

Dropped frame = 0

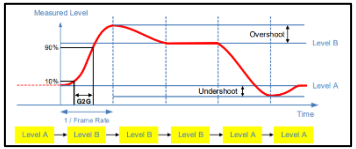
4. Video Frame Rate Jitter



How to measure Fixed media rates 23.976–60 Hz

Jitter ≤ ±0.5 ms

5. Overshoot / Undershoot

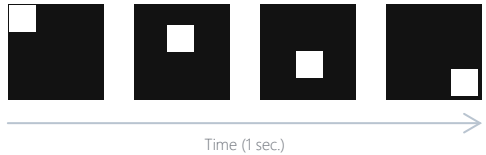


Ideal (blue) vs. Overshoot (red)

How to measure Delta-PQ limit on each transition

Within Delta-PQ limits

6. HDR Test



How to measure HDR ON, 24 / 25 Hz, 1 sec. exposure

Dropped frame = 0

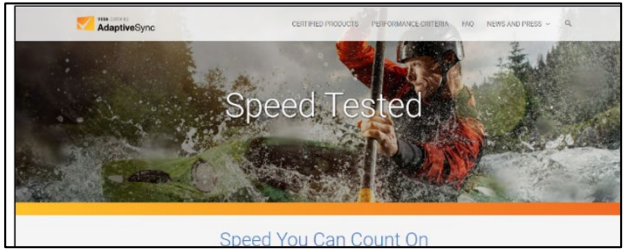
Certified Product Growth & CTS Enhancements

Certification Status & CTS Roadmap

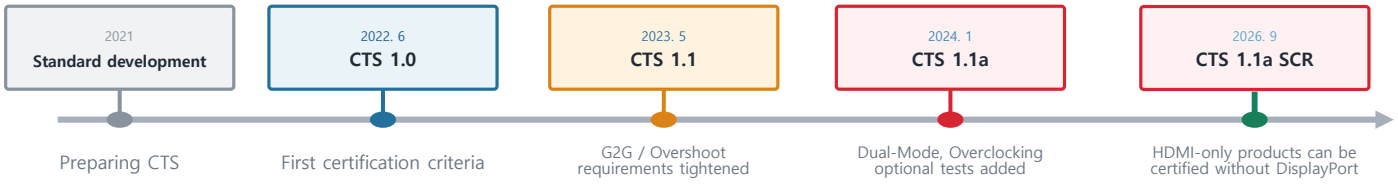
Certification Status

Certified Products(2026.09.08)

AdaptiveSync Display	283	Family incl. 397
MediaSync Display	37	Family incl. 45



Official certified product list: adaptivesync.org



Certified products keep growing, while CTS expands coverage with stronger G2G and Dual-Mode support

PART 04

What is the Next?

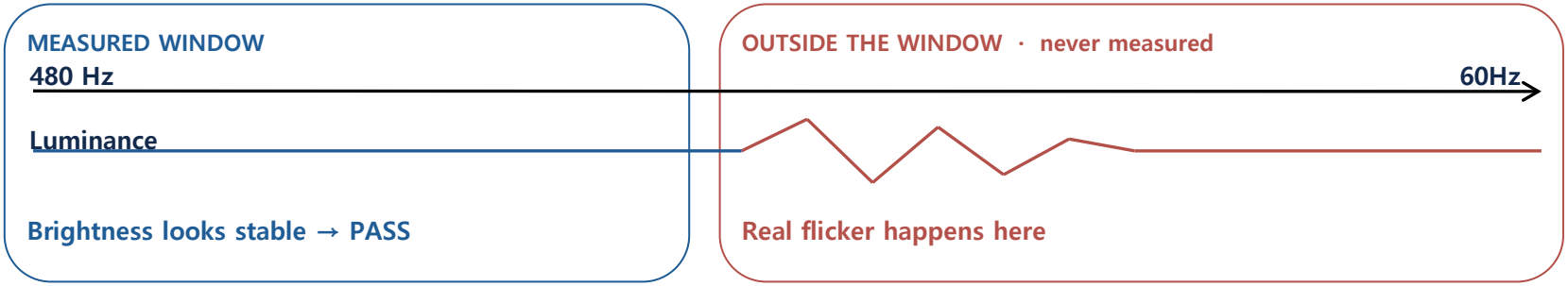
Scope · Key Metrics

What is the Next? (1/3)

Flicker

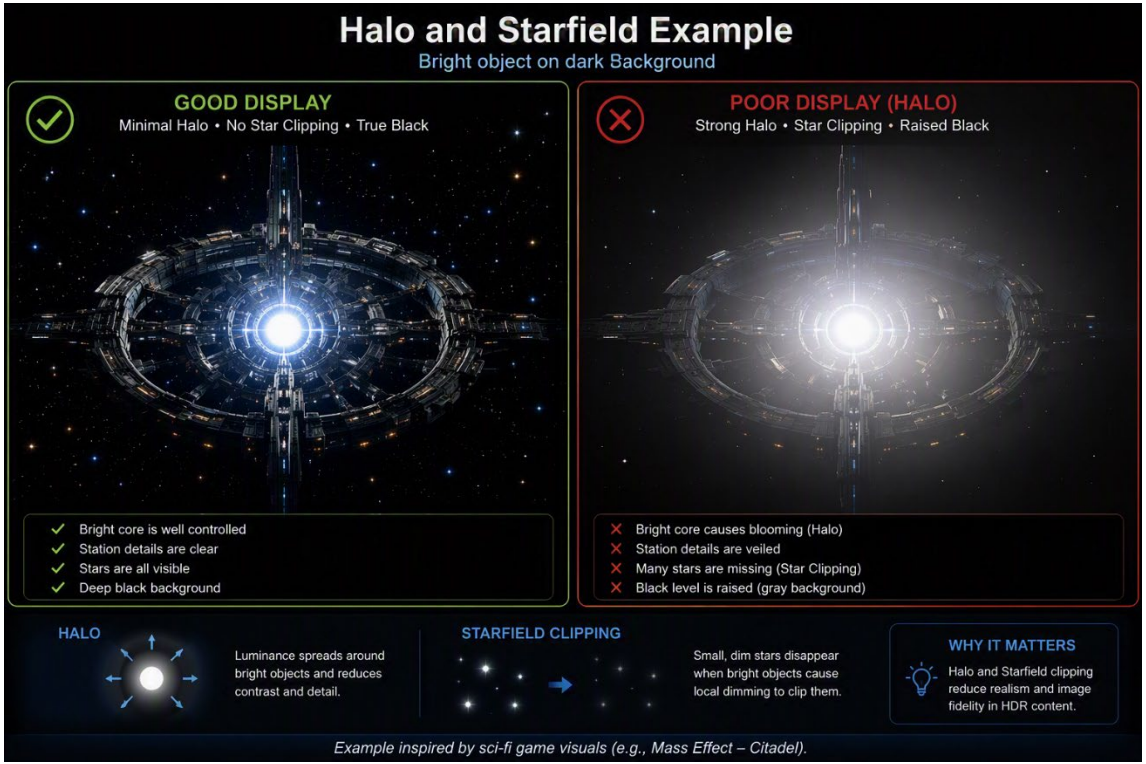
Refresh rate 480 Hz → **drops to 60 Hz**

Brightness can swing every time the refresh rate changes



Limited visibility into transient changes and their causality

Halo and star clipping



01 Test Pattern

02 Measurement

03 Metric & Limit

How DPM Builds an Industry Standard

From open discussion to an industry-wide specification

01

Define what to measure

Test pattern · APL · Measuring point · Timing

02

Gather industry data

Cross-vendor measurement, checked for repeatability

03

Reach consensus

Member agreement on Pass / Fail limits, released as CTS

Conclusion **DisplayHDR, AdaptiveSync and ClearMR give the industry one common, measurable yardstick for display quality.**

Better displays, clearer choices — built together through measurable performance

The DPM Group turns measurable display performance into meaningful quality for users.



HELP SHAPE THE NEXT STANDARD

Your expertise can move display quality forward.

Join the discussion. Share your data. Everyone is welcome to contribute.

Let's define display quality from the user's point of view.

Q & A

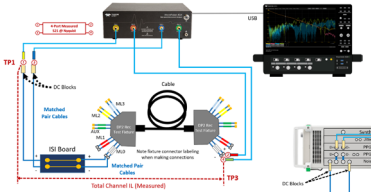
Thank you for your attention

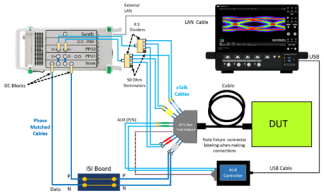
DoKyun Kim (keneth.kim@lge.com)
SeungHyun Yoo (seunghyun.yoo@lge.com)
LG Electronics, Inc.

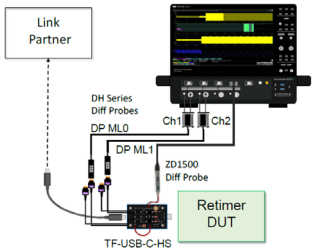
VESA 2026 Seoul Workshop
Demo Tables

DisplayPort 2.1 PHY Compliance and PHY-Logic Debug



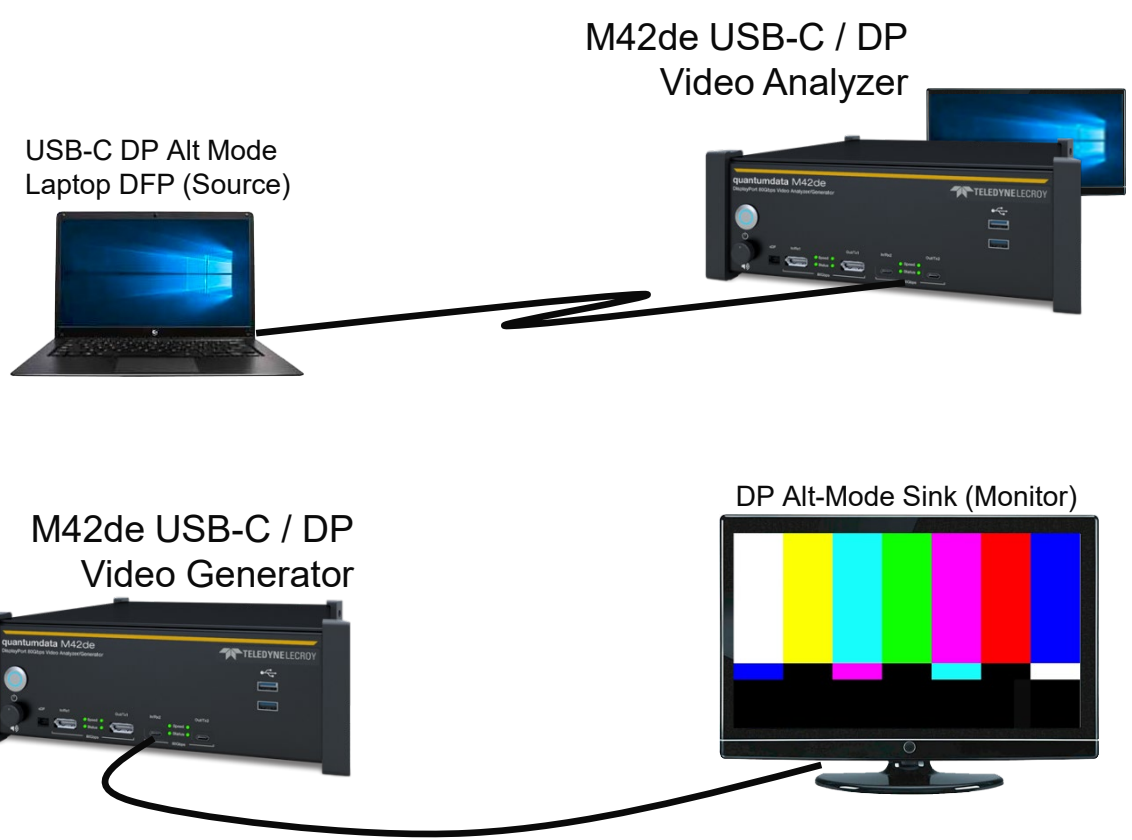






- DisplayPort 2.1 Source (Tx) Compliance
  - WaveMaster/SDA 8000HD with QualiPHY® 2 software
  - SDAX-DP expert analysis – Find Best CTLE/DFE
  - Reduced test times with QPHY2-PC
  - Automated Return Loss with WavePulser 40iX
- DisplayPort 2.1 Sink (Rx) Compliance
  - WaveMaster/SDA 8000HD with QualiPHY 2 software
  - SSG Cal and BER testing using Anritsu MP1900 SQA
  - Automated Channel Cal with WavePulser 40iX
- PHY-Logic (Interop) Debug
  - AUX Triggered + Main Link capture
  - TF-USB-C-HS – probing access
  - DP-AUX, USB-PD TDMP software
  - Clock switch testing on live link

M42de Supports DP2.1 SRC/SNK Testing



- Protocol Analysis - Source Testing
  - Sink emulation EDID, DPCD.
  - Protocol Analysis – Main Link & Aux
  - Compliance Testing - Link Layer, (including FEC), DSC, HDCP.
- Video Generation - Sink Testing
  - Source emulation and Link Training control.
  - Video Pattern Testing –generation of Display Stream Compression (DSC) Panel Replay and FEC.
  - Compliance Testing (Link Layer, FEC, HDCP).
- DP Alt Mode Testing
  - Run all VESA source and sink testing through the USB-C DP Alt Mode ports.

Voyager M4120

Complete USB4® v2 Solution

Analyzer, Exerciser, & Compliance Tester

Asymmetric Link Capture

Capable of capturing and testing 120Gb/s Asymmetric Link Configurations

Traffic Decoding & Unified Workflow

HopIDs Automatically Detected; **Tunneled DisplayPort Decoded**

Single Click Export Native **DisplayPort Traffic**, view in VPS



All Speeds, One Unit

- USB4 v2 120Gb/s (PAM3, Asymmetric)
- USB4 v1 40Gb/s (NRZi)
- Thunderbolt™ 5, 4, & 3
- USB 3.2, USB 2.0
- USB-PD, & Type-C

TELEDYNE | LECROY

Protocol Analysis and Validation

FuturePlus Systems

Advancing Technology Development

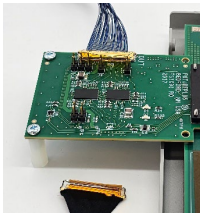
Real Time
ANY Source to *ANY* Sink





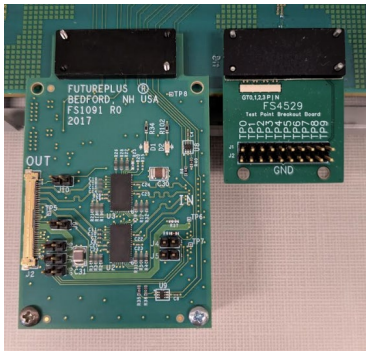
NEW

eDP 2.0 Protocol Analysis With 128b/132b Decode!



NEW

eDP Status and Timing Breakout Board



Features:

- ***Panel Self Refresh (PSR) and Selective Update Status***
- Connect Test Points to oscilloscope, mixed-signal oscilloscope, or timing analyzer
- ***Test Points can be customized!***

All Supported!

- ***eDP 2.0 with 128b/132b Decode***
- Panel Replay
- Aux-Less ALPM
- **UHBR13.5**



Something Special?

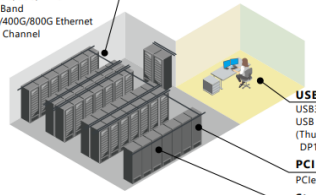
We Like Challenges!

Anritsu MP1900A Signal Quality Analyzer

DP1.4/2.1 SINK Compliance Test Structure

Target Applications

General Interfaces
CEI-28G/56G/112G
InfiniBand
100G/400G/800G Ethernet
Fibre Channel



USB
USB3.2, 4
USB Type-C
(Thunderbolt3/4,
DP1.4/2.0/2.1)

PCI Express
PCIe 1-7

Storage Device
SAS-3/-4

Various Applications
Internal and external interfaces, such as Ethernet, PCIe, SAS, and DDR5, are supported along with USB3.2, 3.4, and Thunderbolt via USB Type-C connectors and cables, and Display Port.

MP1900A supports PCIe 3.0, 4.0, 5.0, 6.0 and 7.0 as well as SAS using the same configuration.



All-in-One Test Support

MP1900A

PCIe 3/4/5/6/7* Receiver Test
Base Specification
- Stressed Eye Test

CEM Specification*
- Transmitter initial Tx Equalization
- Transmitter Link Equalization response
- Receiver Link Equalization
- PLL Bandwidth
- Retimer

USB Type-C Receiver Test (USB4, Thunderbolt3/4, DP1.4/2.0/2.1)
Receiver Test
SJ Margin Test
Amplitude Margin Test

USB 3.2 Gen1/2 Receiver Test
Transmitter Eye Test
Receiver Jitter Tolerance Test
LFPS Test

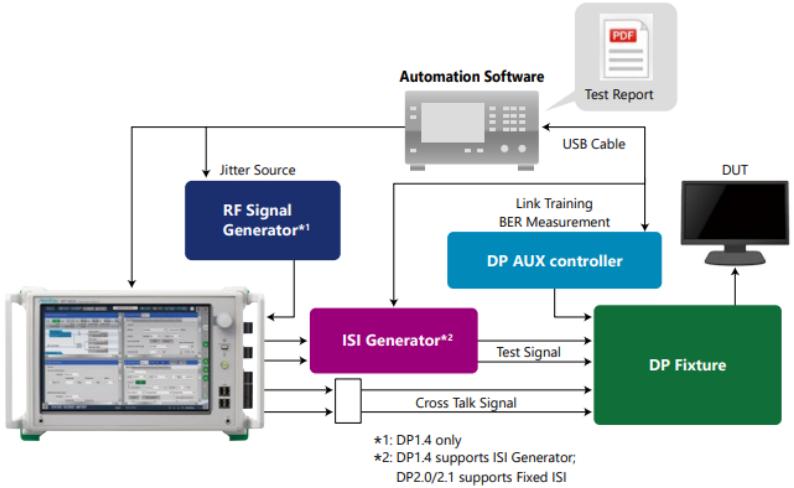
Storage Receiver Test (SAS-3/-4)
Receiver Jitter Tolerance Test

Memory/Memory Controller Receiver Test
- CXL2/3
- DDR5

Jitter Tolerance Test
SJ/RJ/BUJ Injection
Low-rate estimated BER measurement

*: PCIe CEM SPEC supports PCIe 3 to 6.

DisplayPort 1.4/2.0/2.1 Sink Test



Required Functions

- 2.7 Gbit/s to 20 Gbit/s PPG
- Stressed Signal Calibration and Test
- USB Type-C Alternative Mode Operation

UCD-500 Gen3

16K DP 2.1b Generator & Analyzer



- DP 2.1b Sinks and Sources up to 8K@60Hz
- Supports DP and USB-C connectors
- DP 2.1b and DP 1.4a Link Layer CTS including DSC, LTTPR, DisplayID/EDID, MST, Adaptive-Sync and more.

UTC-274

USB Type-C Tester for Test Automation



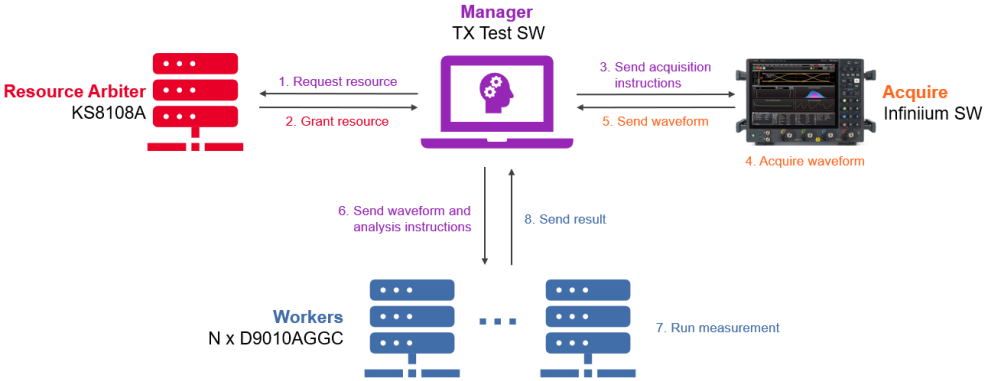
- Test DP Alt Mode, Power Delivery and USB speed
- 2 upstream USB-C test ports
- EPR function test up to 240W Source and Sink

KEYSIGHT

Maximizing Time Efficiency & Prepared for the Future

- Contact Information
  - Abhijeet Shinde
  - Abhijeet.Shinde@keysight.com

Keysight Technologies





XR8 + Disaggregation = Time Efficiency

What are your costs?

- A comprehensive test plan leads to prolonged testing durations.
- A majority, about 75%, of the testing period is consumed by data processing.

What would be an optimal solution?

- Considerable reduction in test time through Measurement Disaggregation.
- Maximizes the use of your existing investment.
- $$$ Cost-effective savings.
- Enhances your current equipment and expertise.

M8050A: Prepared for the future

What are your costs?

- Investment in hardware to meet next-generation requirements
- Reduced passing margin

What would be the optimal solution?

- Reliable support for up to 120GBd and various PAM types
- Provides the lowest intrinsic noise, enhancing passing margin
- Facilitates hassle-free stress calibration, saving both time and money

GRL VESA Certification Testing Services

GRL Taiwan | VESA Workshop 2026

graniteriverlabs.com

GRL VESA Certification Testing Services

Supporting Your VESA Certification Journey

DisplayPort

DP Source & Sink Certification

- DP 1.4 & DP 2.1 (UHBR 10 / 13.5 / 20)

VESA CERTIFIED AdaptiveSync DISPLAY 144

Variable Refresh Rate Certification

- Variable refresh rate performance validation



VESA CERTIFIED DisplayHDR™

HDR Picture Quality Certification

- Multiple performance tiers (400 ~ 1400 / True Black)

VESA CERTIFIED ClearMR 13000

Motion Clarity Certification

- Multiple performance tiers (ClearMR 3000 ~ 21000)

GRL Service Scope

Pre-Compliance
Early issue identification

Compliance Testing
VESA compliance testing

Debug Support
Analysis & troubleshooting

Certification Support
Certification follow-up

Why GRL

- VESA Authorized Test Center with **10+ years** of VESA compliance testing experience
- **3000+ products tested** across DisplayPort, DisplayHDR, AdaptiveSync, and ClearMR
- Global labs, local support in your time zone

Copyright © 2021 Granite River Labs. All rights reserved



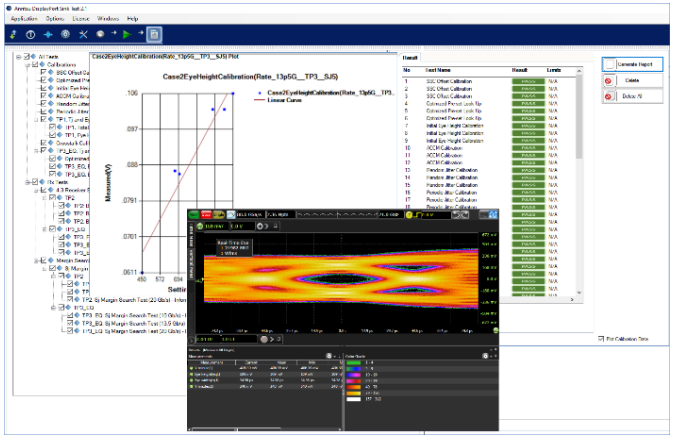
GRL PLATFORM SOLUTIONS
FOUNDATIONAL - INTELLIGENT - PRECISE

GRLPS DisplayPort

DP2.1 Tx PHY Test Solution
DP2.1 Rx PHY Test Solution
DPAM Test Solution

GRL Platform Solutions

DisplayPort 2.1 Tx/Rx Test Automation Solution



USB Type-C® Power Delivery Tester & Analyzer - EPR (new.grlsys.com)



- USB Power Delivery Specification 3.2
- Type-C ® Functional Specification
- IEC Functional Safety (IEC 62368-1)
- **DisplayPort™ Alternate Mode Tests**
- Thunderbolt 3/4/5 Alternate Mode Tests
- Thunderbolt 3/4/5 Power Tests
- Qualcomm® Quick Charge 2™
- Qualcomm® Quick Charge 3™ and 3+™
- Qualcomm® Quick Charge 4™ and 4+™
- Qualcomm® Quick Charge 5™
- BC 1.2 for QC Sink products
- IEC 63680-1-2



The only instrument you need for validating compliance, inter-operability, and reliability of your designs

VESA

BEYOND 1000Hz

CHANGES TO VESA STANDARDS FOR HIGH-FRAME-RATE DISPLAYS

DoKyun Kim (keneth.kim@lge.com)
LG Electronics, Inc.

12 Oct 2026

Agenda

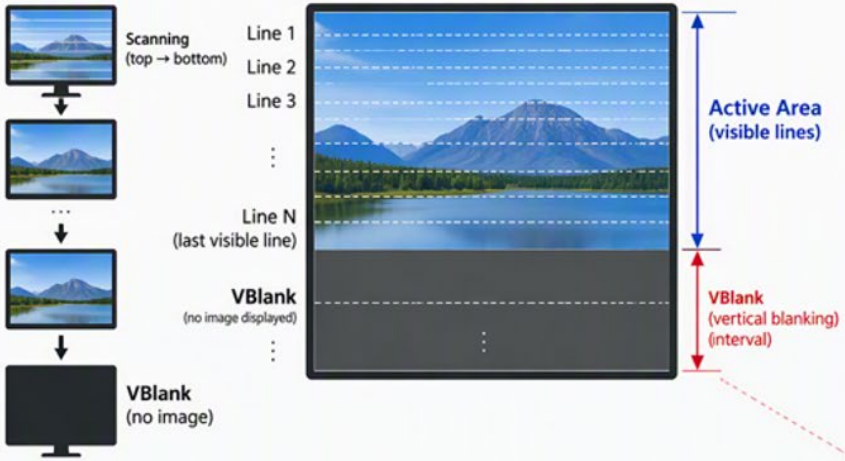
01	**Why now**	The industry has entered the 1,000 Hz era
02	**Where the standard breaks**	Fixed VBlank and limited capability signaling
03	**What VESA is changing**	CVT-RB v4 and DisplayID extensions
04	**What this enables**	Efficient, discoverable, interoperable HFR timing

VESA

What is Vertical Blanking?

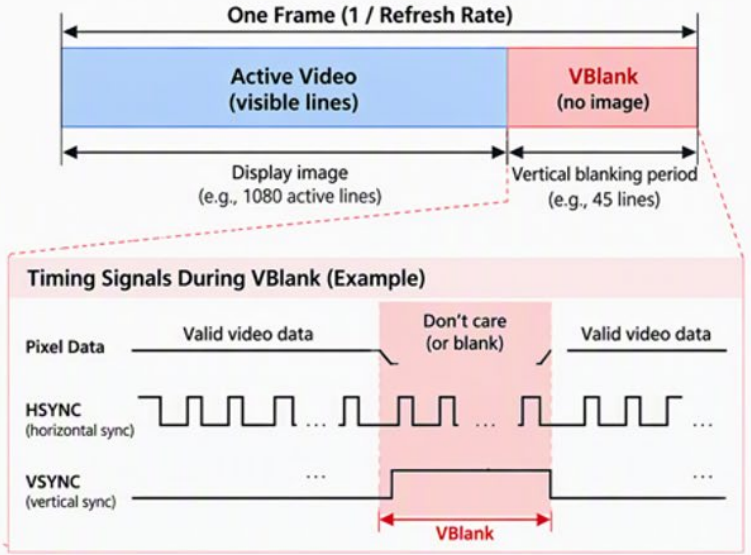
1. What is VBlank?

A display is scanned from top to bottom, line by line.
After the last visible line is transmitted, there is a short period called VBlank, during which no visible image is shown.
Then the next frame begins.



2. Frame Timing Example

A frame consists of the active video period and the vertical blanking period.



3. Key Points

- VBlank is the time between frames.
- No image is shown, and VSYNC usually occurs.

4. What Happens During Vblank?

- The Source prepares the next frame.
- The frame buffer is updated, and control data can be sent.

5. Why Vblank is Important?

- VBlank helps prevent screen tearing and keeps timing stable.
- Its length can affect the maximum refresh rate.

VESA

WHY NOW

1,000 Hz Changes the Timing Budget

1 ms

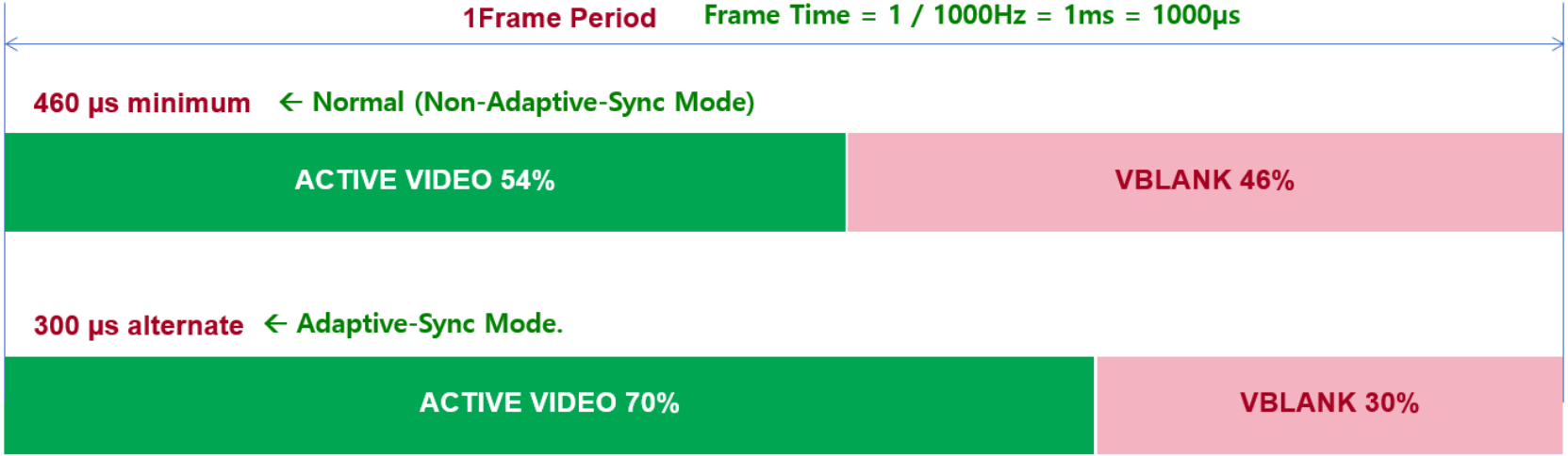
Total frame period at 1,000 Hz

At 1,000 Hz,
blanking time directly reduces active video time.

The link must carry the pixels,
and the timing must be efficient.

Product innovation encourages the continued evolution of timing formulas

Fixed VBlank Becomes the Bandwidth Bottleneck



More Blanking → Higher VTotal → Higher Pixel Clock → Higher Link Bandwidth

VESA

REQUIREMENTS

Two Standards Gaps Must Be Closed Together

GAP 1

Timing generation

How can the Source generate an efficient timing above 1,000 Hz?

CVT-RB v4

GAP 2

Capability discovery

How does the Sink advertise the formula and parameters it supports?

DisplayID Descriptor Extension

VESA
TIMING GENERATION

Solution 1: CVT Reduced Blanking Timing v4

- Default nominal refresh rate above 266 Hz
- **Minimum VBlank based on 8% of nominal frame period**
- Minimum Requirement
  - Subject to a 50 µs absolute minimum and line-count constraints
    * A minimum duration must be guaranteed to carry audio and DP information.
- Targets high-refresh-rate progressive timings
- Designed for Adaptive-Sync or similar variable-refresh operation
- 0.001 MHz pixel-clock precision and +350 ppm offset

At 1,000 Hz

8% × 1,000 µs = 80 µs

A proportional rule, not a fixed legacy duration

Hz	1/Hz, us	Ratio(8%)	us
270	3704	0.08	296
300	3333	0.08	267
330	3030	0.08	242
360	2778	0.08	222
400	2500	0.08	200
480	2083	0.08	167
500	2000	0.08	160
600	1667	0.08	133
720	1389	0.08	111
750	1333	0.08	107
800	1250	0.08	100
900	1111	0.08	89
1000	1000	0.08	80
2000	500	0.08	40
3000	333	0.08	27
4000	250	0.08	20

50 µs
As a minimum value

VESA

DESIGN PRINCIPLE

From Fixed Time to Frame-Proportional Blanking

Timing method	Minimum VBlank basis	High-rate behavior
RB v2 / v3	Fixed 460 µs or 300 µs	Blanking share rises rapidly
RB v4	**8% of nominal frame period**	**Blanking scales with frame time**

Key idea: Enough blanking for stability, but no more than needed.

VESA

CAPABILITY DISCOVERY

Solution 2: Extend DisplayID Capability Signaling

Type X Formula-based Timing Data Block, Block Revision 1

- CVT-RB Timing v4 enumeration
- Refresh-rate range extended to 4,096 Hz
- 8-byte descriptor for expanded capability fields
- HBlank and Early VSync options
- Additional VBlank and alternate-minimum information
- Existing 6-byte and 7-byte variants remain unchanged



SOURCE CAN SELECT

the right timing formula

with supported blanking parameters

for refresh rates beyond 1,024 Hz

VESA

RELATED WORK

Adaptive-Sync Granularity: A Related DisplayID Extension

High frame rate is not only about the maximum rate.
Frame-period adjustment granularity can also affect visual quality.

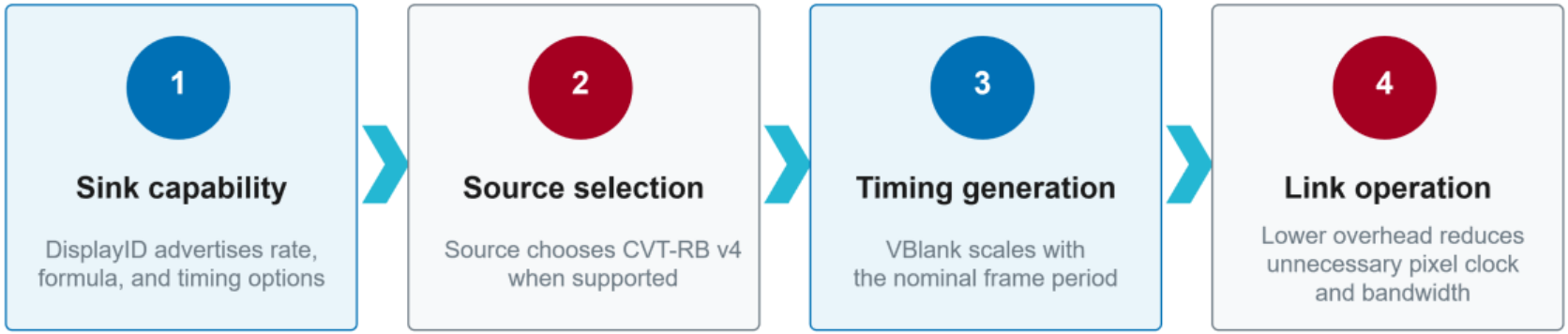


This work complements high-rate timing by making frame adjustment behavior explicitly discoverable.

VESA

END-TO-END VIEW

The Standards Must Work as One System



Timing formula + capability signaling + interface mandates
= interoperable high-frame-rate operation

VESA

CURRENT STATUS

Standardization Status and Decisions Ahead

CVT SCR	2026	**RB Timing v4 formula and mandates**
DisplayID SCR	2026	**Type X descriptor extension**

KEY REVIEW QUESTIONS

- Are the thresholds and constraints appropriate?
- Is capability signaling complete?
- Are legacy behavior and future extensibility balanced?
- What CTS and interoperability updates are required?

The CVT and DisplayID changes are being reviewed together because neither is sufficient alone.

VESA

CONCLUSION

Key Takeaways

01	**1,000 Hz exposes a structural issue**	Fixed blanking consumes too much of a 1 ms frame.
02	**CVT-RB v4 improves timing efficiency**	VBlank scales with frame time while retaining minimum constraints.
03	**DisplayID makes the capability discoverable**	The Sink explicitly communicates high-rate timing support to the Source.
04	**Coordinated revisions enable interoperability**	Formula, signaling, and interface behavior must align.

Goal: Coordinated CVT and DisplayID updates are essential for efficient high-frame-rate operation.

VESA

Q & A

DP LRD Active Cable Testing

Jim Choate
VESA Compliance Program Manager
Material courtesy of Lexus Lee from Allion Labs
2026/10/12

Overview

- Why VESA Defines LRD Active Cable Spec
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA Connector Certification Introduction
- Cable Next - Active Optical Cable?

Why VESA Defines LRD Active Cable Spec

- Enable UHBR20 transmission over a 2-meter or longer cable
  - Without adding extra cost/thickness passive cable limited to < 1.5m cable, which cannot meet all use-case requirements
- LRD Active Cable Type for VESA Certification

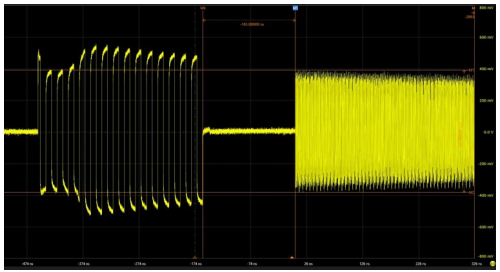


Overview

- Why VESA Defines LRD Active Cable Spec
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA Connector Certification Introduction
- Cable Next - Active Optical Cable?

What Is Inside VESA LRD Cable CTS?

- Time Domain test
  - Eye Diagram
  - Instantaneous Common Mode Voltage
  - CONFIG2 Voltage and No DP_PWR thru Cable
  - AUX-Less ALPM
  - LOS Test
  - Inrush Current Test
  - AUX Voltage Clamping
  - Preset Distortion Thru the cable



What Is Inside VESA LRD Cable CTS? Cont’

- Functional test
  - Successful Link Training
    - All data rate(from RBR to UHBR20)
    - All lane count (1-Lane, 2-Lane,4-Lane)
    - Bidirectional (Swap Sink/Source end)
    - These tests are typically performed using DP 2.1 Link Layer TE in loopback
    - Power management (Active Power ,Wake/Sleep, Aux-less ALPM)
    - USB-C Orientation (Flip/Normal)



  - SOP/SOP’ Response Check(SVDM2.0/SVDM2.1)

What Is Inside VESA LRD Cable CTS? Cont’

- Frequency Domain test
  - Insertion Loss Fit
  - Receiver Margin Evaluation
  - IRL Integrated Return Loss

Table 4-14: DP80LL Nyquist Frequencies and their ILFitAtNq Mandates (Normative)

Nyquist Frequency (GHz)	DP-to-DP and USB-C-to-DP ILFitAtNq Mandate (dB)[a]
15.00	> -10.40
12.50	> -9.50
10.00	> -6.50
6.75	> -5.20
5.00	> -4.55
2.70	> -3.25
0.10	> -1.00

a. *Cable values are measured mated pair-to-mated pair.*

8.3.3 Receiver Margin Evaluation

Channel Operating Margin (COM) ≥ 3 dB

Table 8-6: LRD Cable IRL Limits

Mode	IRL Limit
DP80	*if (-4 dB ≤ ILfit@Nq): IRL ≤ -13 dB* *if (ILfit@Nq < -4 dB): IRL ≤ ILfit@Nq – 9*
DP54	$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 8.784$

Update About LRD Active Cable in DP 2.1b Spec

- DP80LL (Low Loss)
  - The only difference between the DP80LL and DP80 cable spec is the IL FitAtNq requirement.

Table 4-14: DP80LL Nyquist Frequencies and their ILFitAtNq Mandates (Normative)

Nyquist Frequency (GHz)	DP-to-DP and USB-C-to-DP ILFitAtNq Mandate (dB)[a]
15.00	> -10.40
12.50	> -9.50
10.00	> -6.50
6.75	> -5.20
5.00	> -4.55
2.70	> -3.25
0.10	> -1.00

a. Cable values are measured mated pair-to-mated pair.

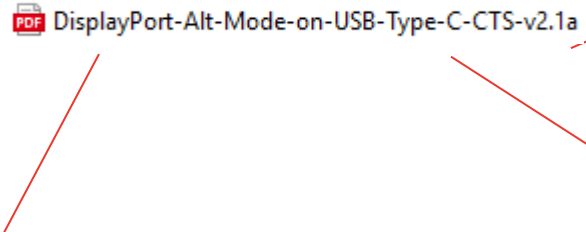
Table 4-12: DP80 Nyquist Frequencies and their ILFitAtNq Mandates (Normative)

Nyquist Frequency (GHz)	ILFitAtNq Mandate (dB)	
	DP-to-DP[a]	USB-C-to-DP[b]
15.00	> -12.0	> -12.25
10.00	> -7.50	> -8.10
6.75	> -6.00	> -6.20
5.00	> -5.25	> -5.30
2.70	> -3.75	> -3.80
0.10	> -0.75	> -1.00

a. Cable values are measured mated pair-to-mated pair.
b. Cable values are measured plug-to-mated pair.

What Is Inside VESA LRD Cable CTS? Cont'

- Additional Tests Added for USB-C to DP LRD Active Cable
  - From DP Alt Mode 2.1 CTSa



10.6

9.5

10.4

10.7

DisplayPort Alternate USB-C to DP Adapter Tests 141
10.6.1 DP Connector Attached to DP Sink 141
10.6.2 DP Connector Attached to DP Source 142

9.4.5 Pass/Fail Criteria 55
HPD and IRQ_HPD Tests (Normative) 56
9.5.1 HPD-to-PD Conversion Test 56
9.5.1.1 Test Objective 56
9.5.1.2 Test Setup 56
9.5.1.3 Initial Conditions 56
9.5.1.4 Test Method 57
9.5.2 PD-to-HPD Conversion Test 58
9.5.2.1 Test Objective 58
9.5.2.2 Test Setup 58
9.5.2.3 Initial Conditions 58
9.5.2.4 Test Method 59

DisplayPort Alternate Mode on USB Type-C Tests for Cables 131
10.4.1 SOP' Cable Discovery Process & Mode Entry 131
10.4.2 SOP' (SOP") DisplayPort Configurations and Exit Mode 133
10.4.3 DPAM Version 2.1 Cable Connected to DPAM Version 2.0 or 2.1 DFP_U 134

DisplayPort Alternate Mode VIF Consistency Check 149
10.7.1 SOP' Discover Identity and SOP' DisplayPort Discover Modes 149
10.7.2 SOP Discover Identity and SOP DisplayPort Discover Mode 150

CTS Testing Challenges

- Knowledge to get DP LRD cable to work up
  - AUX and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Aux P: Pull down to GND
2. Aux N: Pull high to 2.89~3.6V.
3. DP_PWR:2.89~3.6V
4. Aux transaction if needed



1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull high to 2.25~3.6V
5. Aux transaction if needed

CTS Testing Challenges Cont’

- Knowledge to get USB-C to DP LRD cable to work up
  - Vconn, AUX, and DP_PWR Electrical setting
    - Sink devices and Source devices

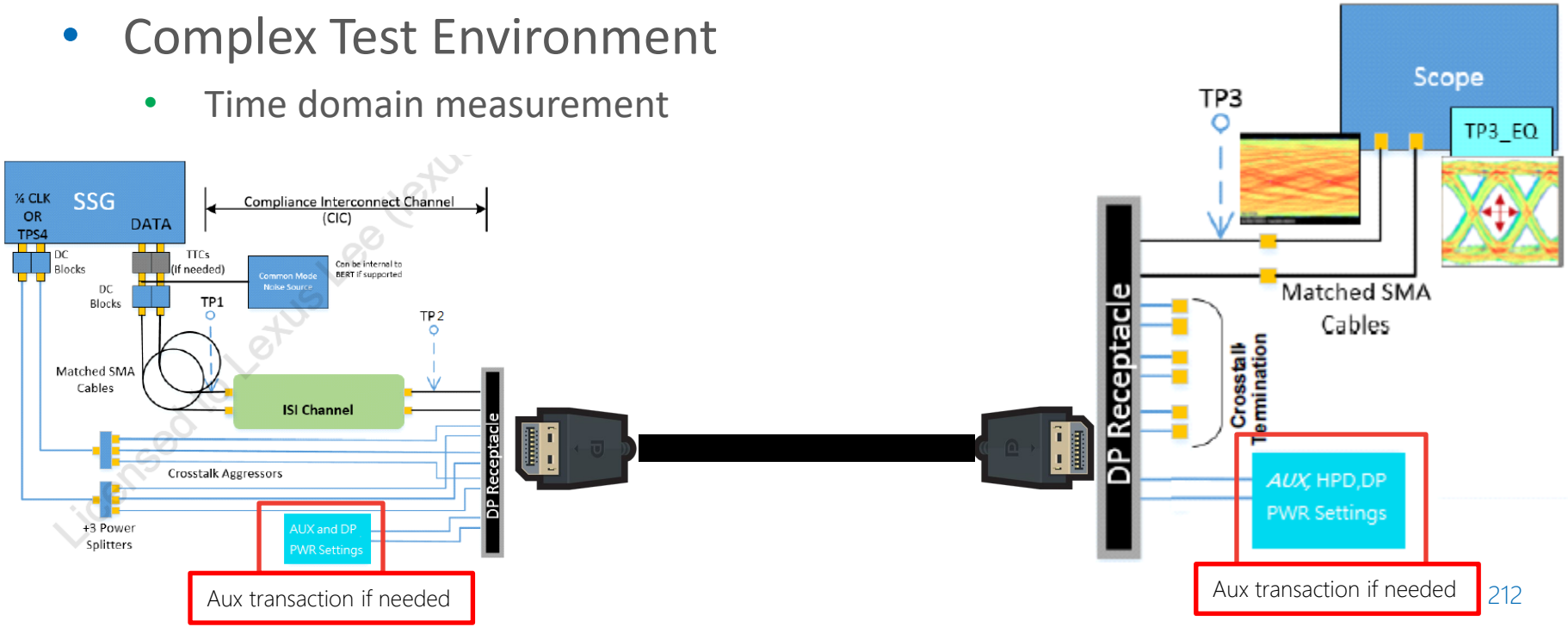
1. Vconn:3.0~5.5V
2. DP alt mode exerciser if needed.
3. Aux circuitry if needed.
4. Aux transaction if needed



1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull High to 2.25~3.6V
5. Aux transaction if needed

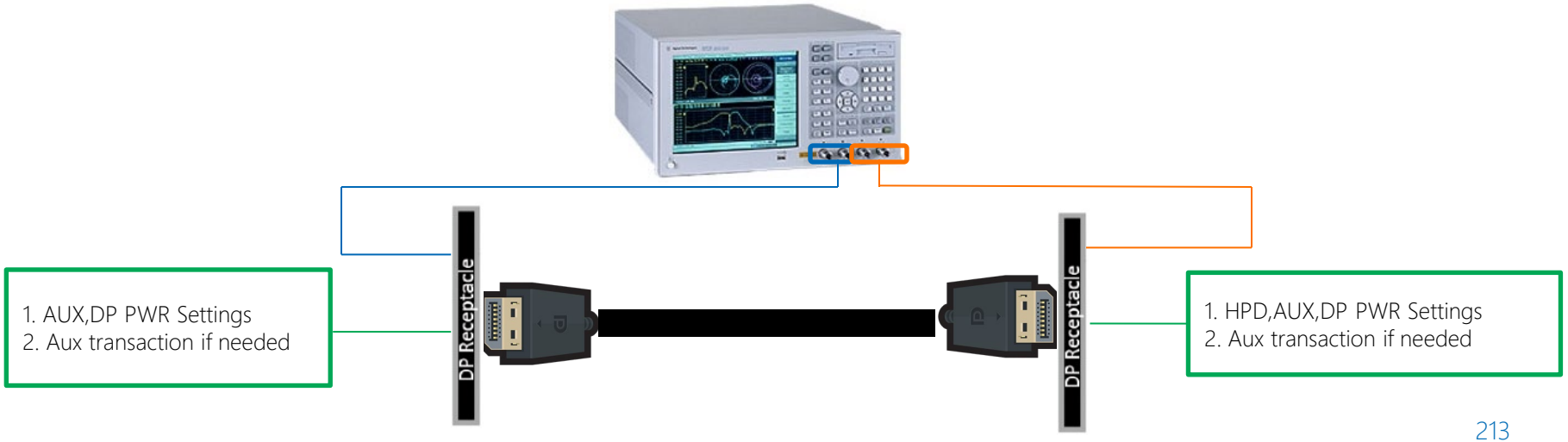
CTS Testing Challenges Cont’

- Complex Test Environment
  - Time domain measurement



CTS Testing Challenges Cont’

- Complex Test Environment
  - Frequency domain measurement



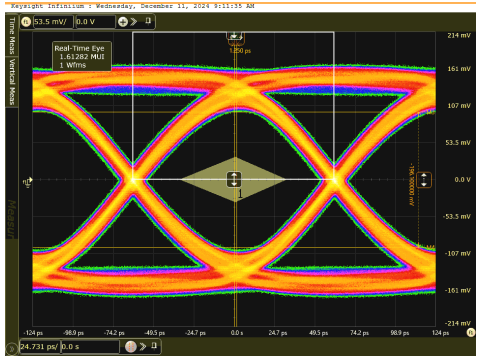
Overview

- Why VESA Defines LRD Active Cable Spec
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA Connector Certification Introduction
- Cable Next - Active Optical Cable?

The Most Frequently Failed Items

- Eye Diagram
  - UHBR20 Criteria
    - TP3_EQ-Inner Eye Height: 100mV
    - TP3_EQ-Eye Width: 560mUI
    - Cannot hit the eye mask
  - Requirement: Need to pass with 3 TxFFE Presets and average of 5 times.

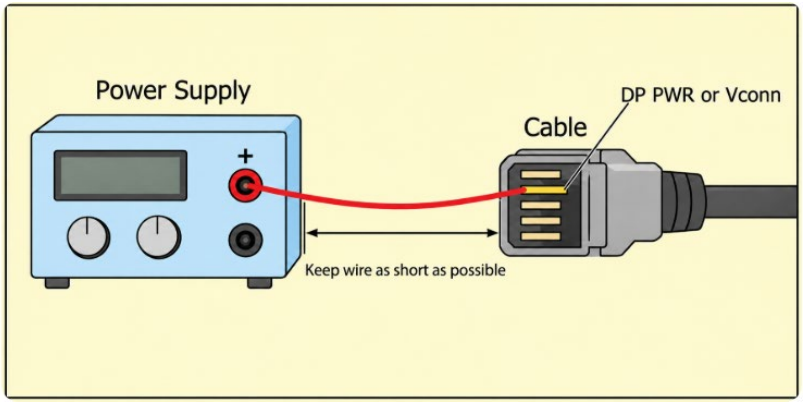
Preset Configuration #	Preshoot (dB)	De-emphasis (dB)
0	0	0
1	0	-1.9
2	0	-3.6
3	0	-5.0
4	0	-8.4
5	0.9	0
6	1.1	-1.9
7	1.4	-3.8
8	1.7	-5.8
9	2.1	-8.0
10	1.7	0
11	2.2	-2.2
12	2.5	-3.6
13	3.4	-6.7
14	3.6	0
15	1.7	-1.7



  - Caused by Raw cable material quality and cable vendor manufacturing capability

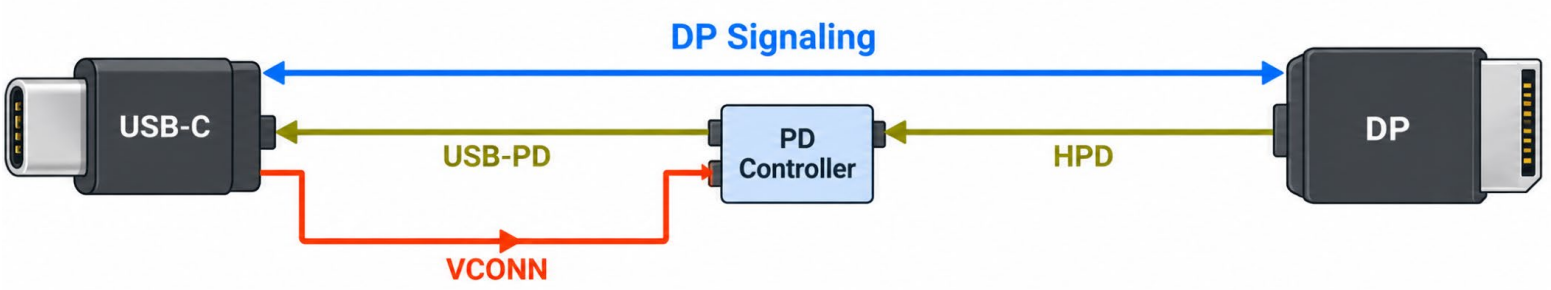
The Most Frequently Failed Items Cont’

- The Minimal Required Voltage
  - DP PWR Range: 2.89-3.6V for DP-DP Cable
    - Voltage Range : 2.89-3.6V
    - 2.89V → Failure
  - Vconn Range for USB-C to DP Cable
    - Voltage Range: 3.0-5.5V
    - 3.0V → Failure



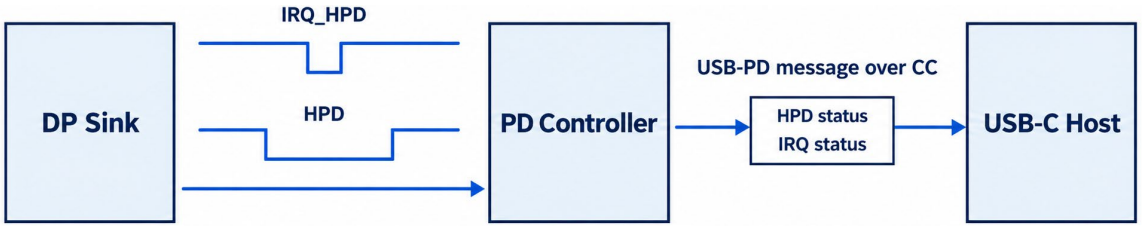
The Most Frequently Failed Items Cont'

- USB-C to DP Cable Structure



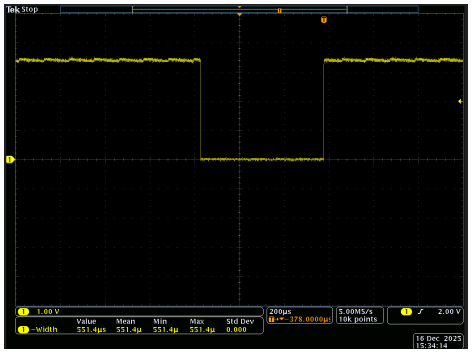
The Most Frequently Failed Items Cont'

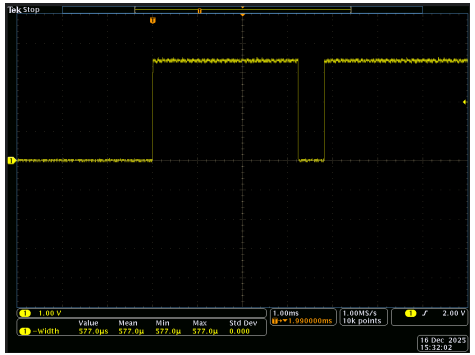
- HPD to PD Conversion
  - Different IRQ_HPD width
    - 2.05 to 2.1msec
    - 1.9 to 1.95msec
    - **2.60 to 270usec**
    - 230 to 240usec
  - Different HPD width
    - 5ms
    - 150ms

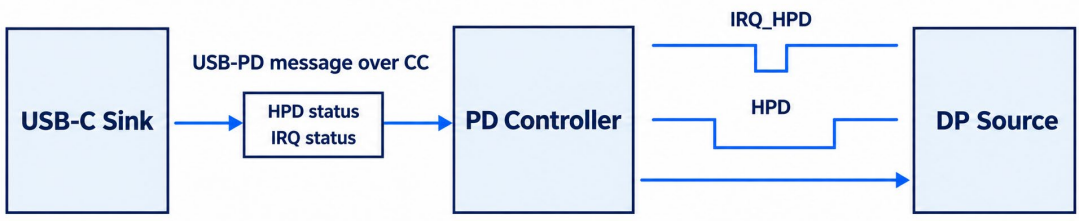


The Most Frequently Failed Items Cont'

- PD to HPD Conversion
  - IRQ_HPD status flag is set
  - HPD_Low is set
    - HPD_High is set
  - HPD_Low is set for 100ms
  - HPD_High and IRQ_HPD are set
    - In a single message

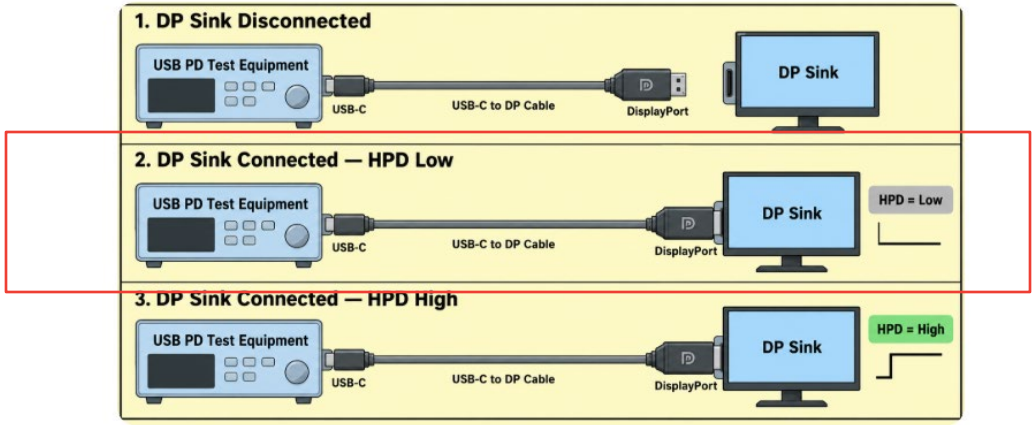






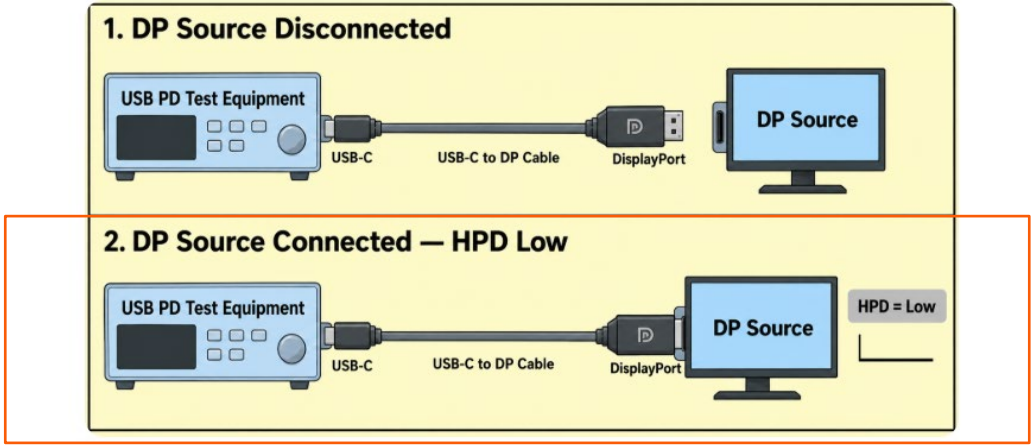
The Most Frequently Failed Items Cont'

- Attach to DP Sink
  - 3 test cases
    - Middle one→Failure
      - Assertion of DP Sink Disconnected



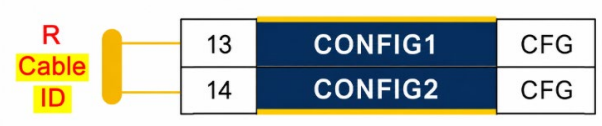
The Most Frequently Failed Items Cont'

- Attach to DP Source
  - 2 test cases
    - Buttom one→Failure
      - Assertion of "DP Source Disconnected" when HPD is low



The Most Frequently Failed Items Cont'

- Cable ID at Fs/mDP connector for Passive cable
  - Connect the Config2 pin to Config1 pin with a resistor
    - 680Kohm for UHBR13.5
    - 220Kohm for UHBR20
      - CTS Requirement: Verify The "Resistor" Value

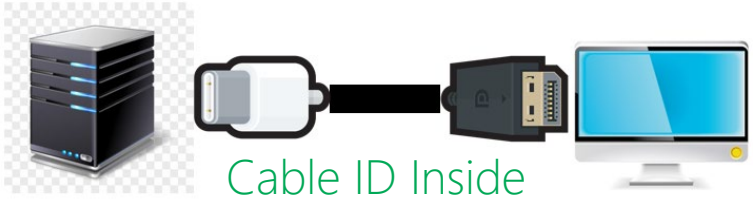


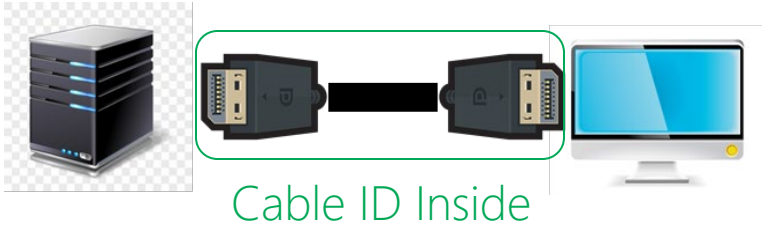
- Cable ID at Fs/mDP connector for Active cable
  - The LRD IC Is Adopted
    - Making the circuit design more complicated
      - CTS Requirement: Verify The Voltage Value on Config2



The Most Frequently Failed Items Cont'

- Typical Application of Cable ID





Rx: Read Cable ID from Cable

Rx: Read Cable ID from Cable

Tx: Read Cable ID from The Cable at USB-C end

Tx: Inform Rx of Cable ID at USB-C end

Tx: Read Cable ID from Rx

The Most Frequently Failed Items Cont'

- Cable ID at USB-C Connector
  - Rely of SOP' Discover Modes
- If UHBR20 Is Set
  - UHBR13.5 shall be set accordingly
- Active or Passive Declaration
  - SOP' Discover Identity
  - TBT3 host compatibility

Bit(s)	Description	Values
1:0	**RESERVED**	RESERVED (always 00b).
5:2	**Signaling for Transport of DisplayPort Protocol**[b]	XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10. X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20). All other values are RESERVED for higher bit rates.[c]
7:6	**RESERVED**	RESERVED (always 00b).
15:8	**DP Source Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported. 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
23:16	**DP Sink Device Pin Assignments Supported**	0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable). 10h = *USB-C* and *DP* connector Pin Assignment E is supported. All other values are RESERVED.
25:24	**RESERVED**	RESERVED (always 00b).
26[d]	**UHBR13.5**	0 = UHBR13.5 is not supported. 1 = UHBR13.5 is supported.[e]
27	**RESERVED**	RESERVED (always 0).
29:28[d]	**Active Component**	00b = Passive. 01b = Active re-timer. 10b = Active re-driver. 11b = Optical.
31:30	**DPAM Version**	00b = Version 2.0 or earlier. 01b = Version 2.1 or higher.

Overview

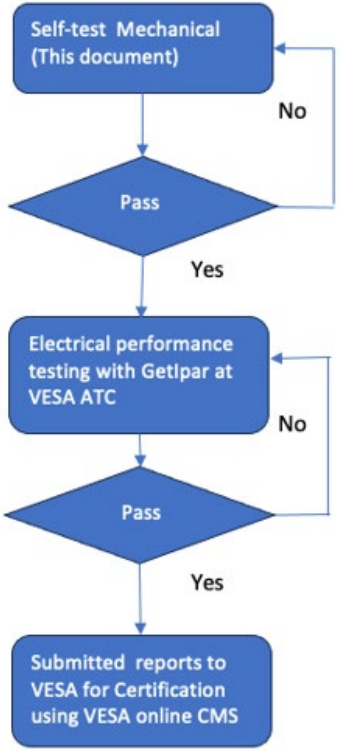
- Why VESA Defines LRD Active Cable Spec
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA Connector Certification Introduction
- Cable Next - Active Optical Cable?

DP Connector Certification Status

- Connector certification
  - Legacy Connector(HBR2 and below)
    - Has been phased out from end of 2025
  - DP8K & Enhanced Connector
    - Self-test Mechanical

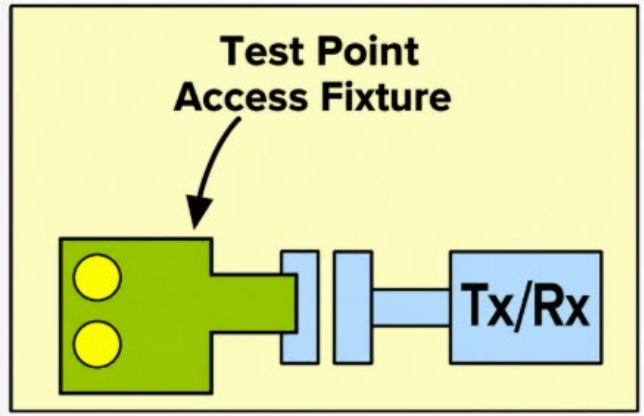
VESA® DisplayPort™ Self-Test Report for Connectors v2.1

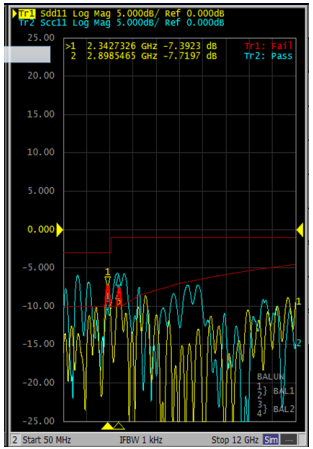
VESA® DisplayPort™ Self-Test Report for DP Connectors Supporting HBR3 Link Rate and DP8K Cables

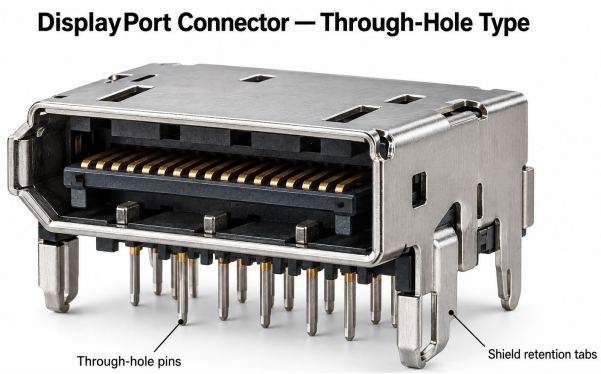


DP Connector Certification Status Cont'

- Enhanced DP Connector (DIP Type)
  - Possibly causing Sink/Source Return Loss test to fail
    - Even if it is a certified EnDP connector
    - Test method different between Connector and Sink/Source in CTS







Overview

- Why VESA Defines LRD Active Cable Standard
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA Connector Certification Introduction
- Cable Next - Active Optical Cable?

Active Optical Cable

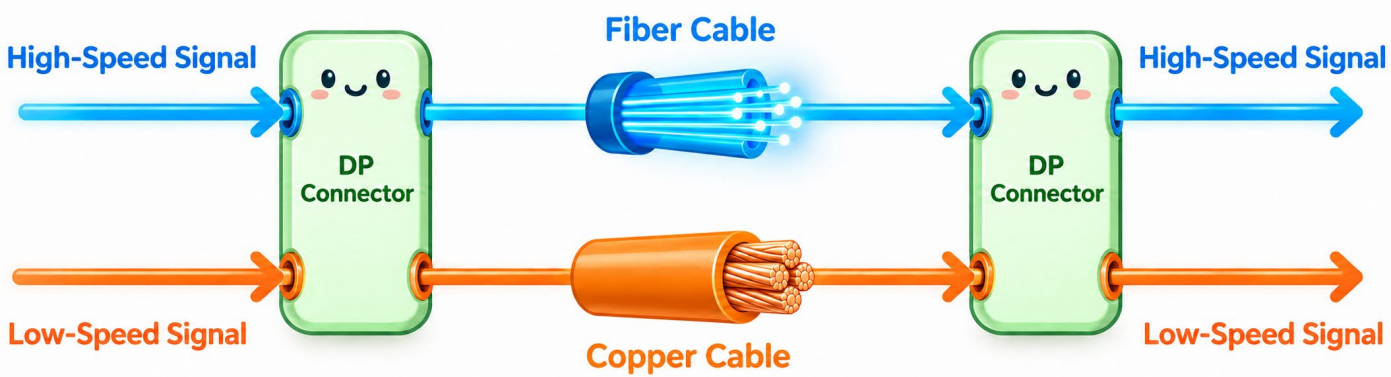
- Definition of DPCD 02217h and 00110h
  - Will add optical cable type in Bit 5:3 Cable Type field: 100b = Optical cable

	5:3	**Cable Type** 000b = Cable type is unknown (default; a DPRX device with a DP receptacle connector shall keep this value). 001b = Passive cable. 010b = LRD cable. 011b = LTTPR re-timer active cable. All other values are RESERVED.
	7:6	**RESERVED**

Licensed to

Active Optical Cable Cont’

- The Optical Cable’s Structure
  - Fiber used for Main-Link channels (High-Speed Data)
  - Copper used for Non-Main-Link channels



Active Optical Cable Cont'

- Allion has been verifying AOC performance
  - Equalization Setting on Each Lane
    - USB-C to USB-C Ends
      - Could be different due to the loss different definition between DP and USB specs while in Pin Assignment D Mode
    - USB-C to DP/mDP Ends and DP/mDP to DP/mDP Ends
      - Should be the same or be closer.
  - Creating PHY test proposal
    - Test items Include common items like Jitter/Eye/SSC/Skew
    - More focus on "Stressed Signal Condition" verification for TP3/TP3_EQ Eye

Thank you

VESA

Design Considerations for USB-C® Products

Abel Astley
Unigraf
October 2026

Design Considerations for USB-C



==



Design Considerations for USB-C

Agenda

- **Back to Basics**: Sources, Sinks, and how they interoperate
- **Common Mistakes** and how to avoid them
- **Factory Testing** Challenges and Solutions
- **Recent Updates** to DP Alt Mode

Back to Basics

Fundamental Concepts of USB-C

Back to Basics: Vocabulary

- From *USB Type-C® Cable and Connector Specification*, Rev 2.5 (March 2026)

Source	Port asserting ***Rp*** on CC and when attached is providing power over VBUS; most commonly a Host or Hub DFP.

Sink	Port asserting ***Rd*** on CC and when attached is consuming power from VBUS; most commonly a Device.

- In USB Speak, ***Source*** and ***Sink*** refer to a device's ***power role***, not its video role
- Where possible, this presentation will explicitly state which role is being referenced

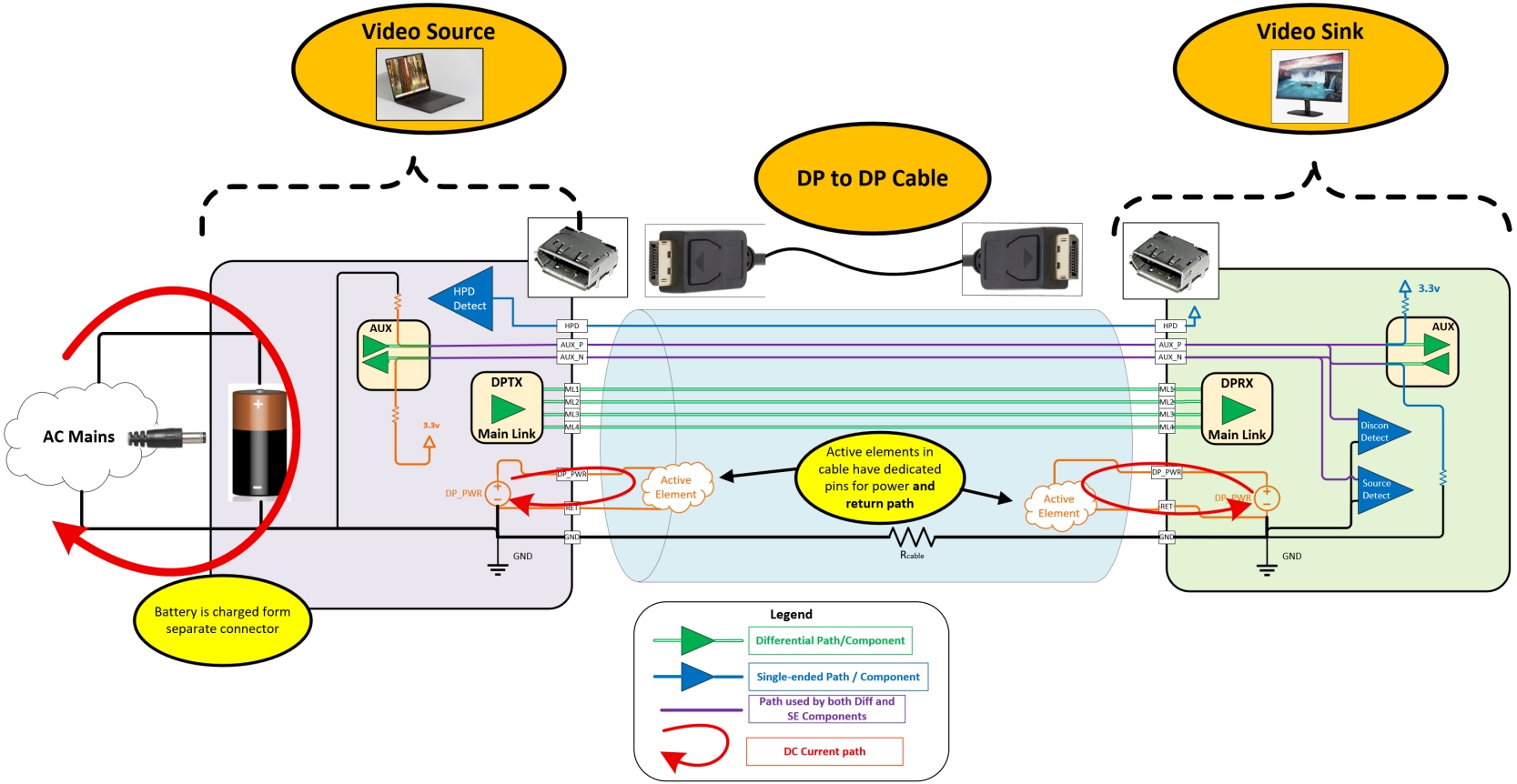
Common Mistakes

The Impact of Ground Current

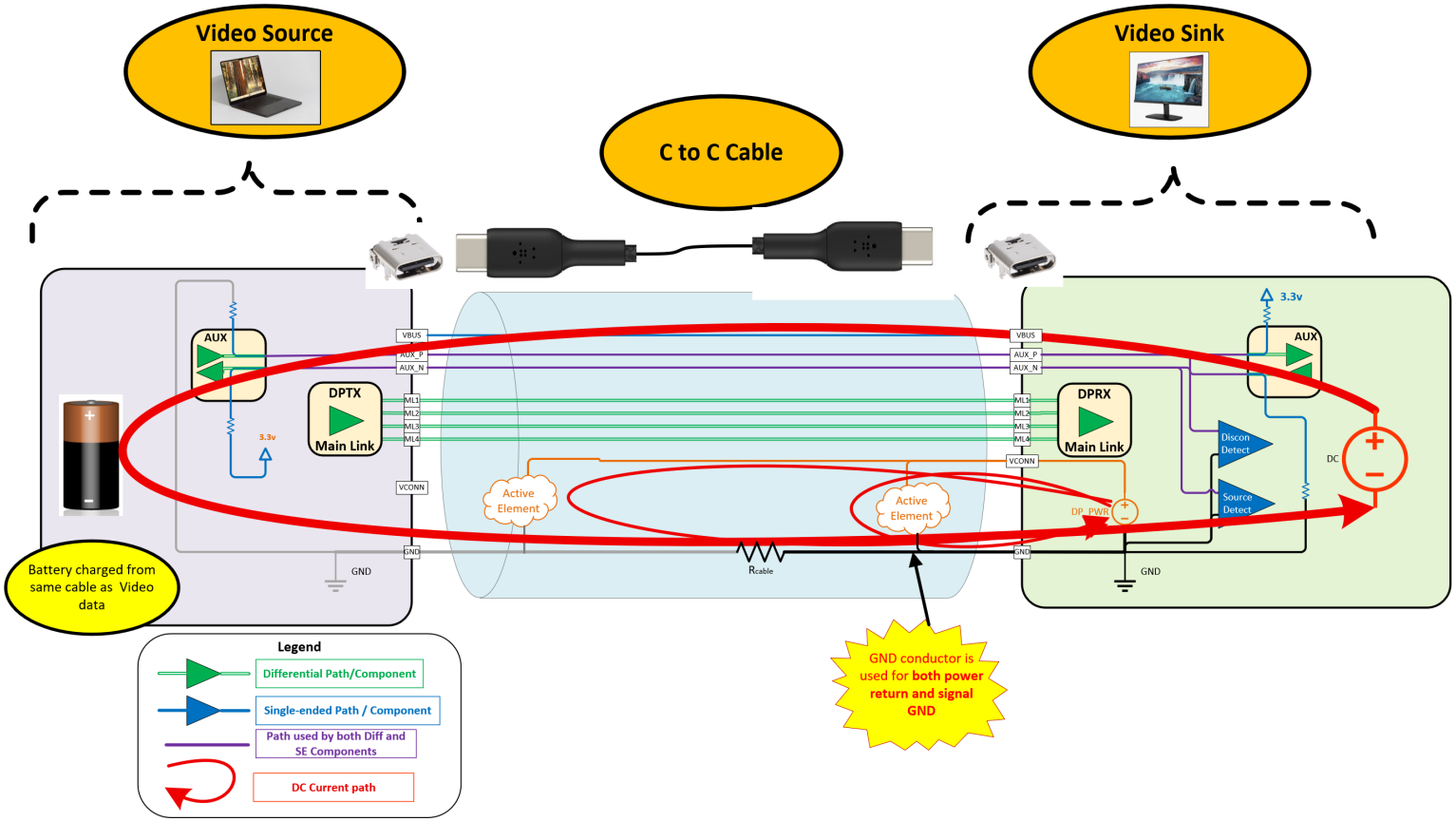
Ground Current

- ***Ground current*** refers to current flowing through the cable GND conductors
- For Native DP, this current should be close to zero
- For USB-C, ***ground current*** can be **5 amps** in either direction, and can **change dynamically**

Native DP Link



USB-C Link


Video Source
Video Sink
C to C Cable
AUX
DPTX
Main Link
DPRX
Main Link
3.3v
VBUS
AUX_P
AUX_N
ML1
ML2
ML3
ML4
VCONN
GND
Active Element
Active Element
Rcable
Discon Detect
Source Detect
DP_PWR
DC
Battery charged from same cable as Video data
Legend
Differential Path/Component
Single-ended Path / Component
Path used by both Diff and SE Components
DC Current path
GND conductor is used for both power return and signal GND

Notes on Ground Current

- Bad/old cable will increase effect
- Usually can't fix in fw
- From *Universal Serial Bus Power Delivery Specification*, Release 3.2, Version 1.2, May 20, 2026:

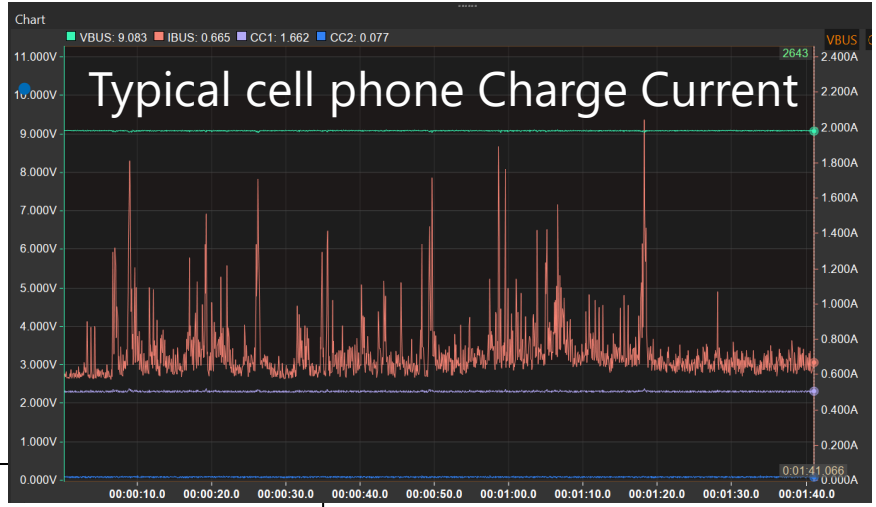


Table 4.7. Sink Electrical Parameters

Parameter Name	Min Value	Nom Value	Max Value	Unit	Description
cSnkBulk			See [USB3]		Sink bulk capacitance on VBUS at Attach and during FRS after the Initial Source stops sourcing and prior to establishing the First Explicit Contract.
cSnkBulkPd			100	µF	Bulk Capacitance that a Sink is allowed to present on VBUS after a successful Negotiation.
iLoadReleaseRate	-150			mA/ µs	Load release di/dt.
iLoadStepRate			150	mA/ µs	Load step di/dt.
iPpsCLLoadStep	-500		500	mA	Maximum Current set-point change while operating in CL Mode.

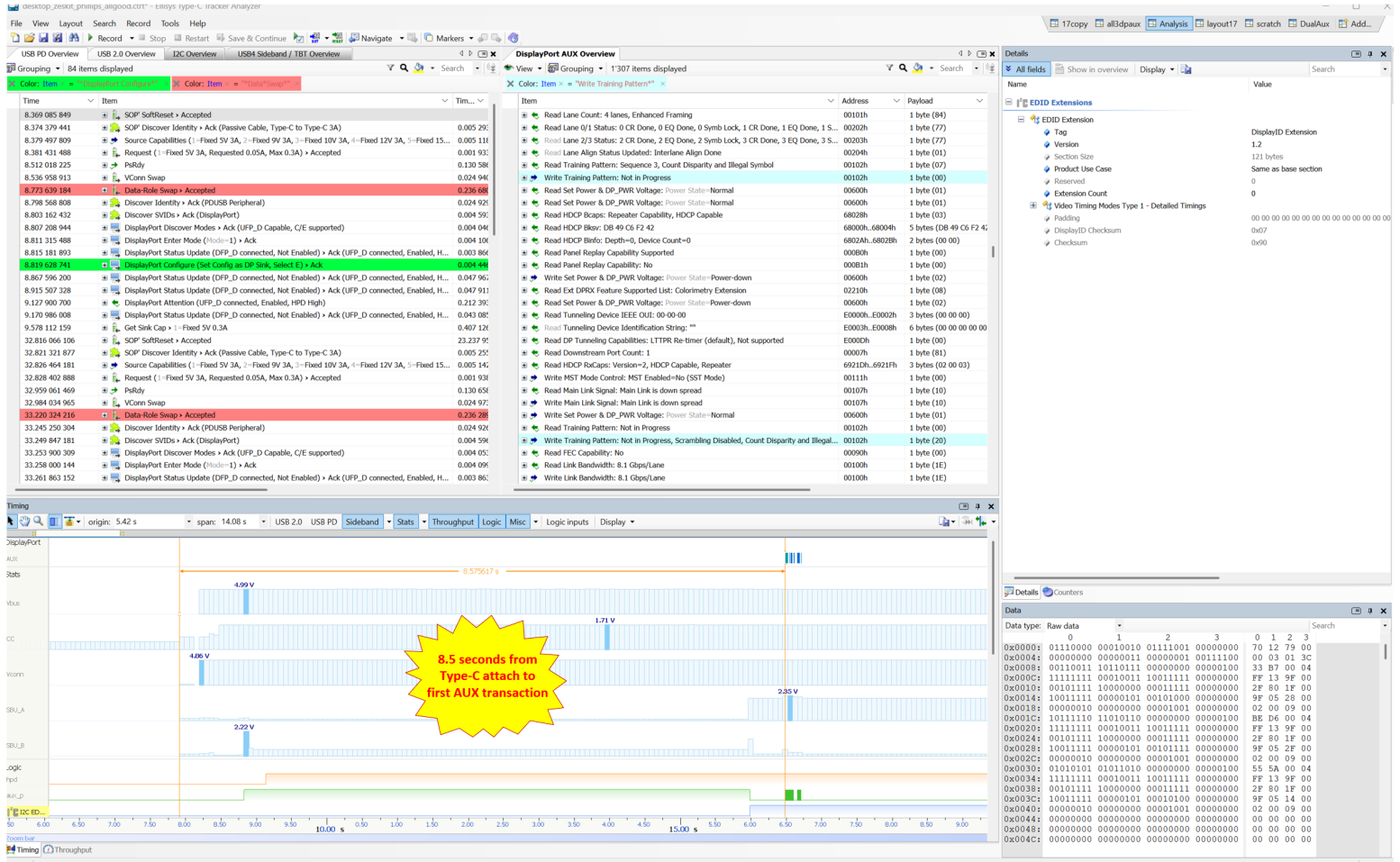
Common Mistakes

Time from plug-in to display light-up

Time from plug-in to Display “light-up”

- USB-C and DP Subsystems are typically developed by independent engineering teams
- This sometimes leads to sub-optimal interactions between the two
- This can be noticed in certain DP Alt Mode scenarios, in which the display takes several seconds to light up after cable plug-in

Time from plug-in to Display “light-up”



Factory Testing

Considerations for improving accuracy in production line test environments

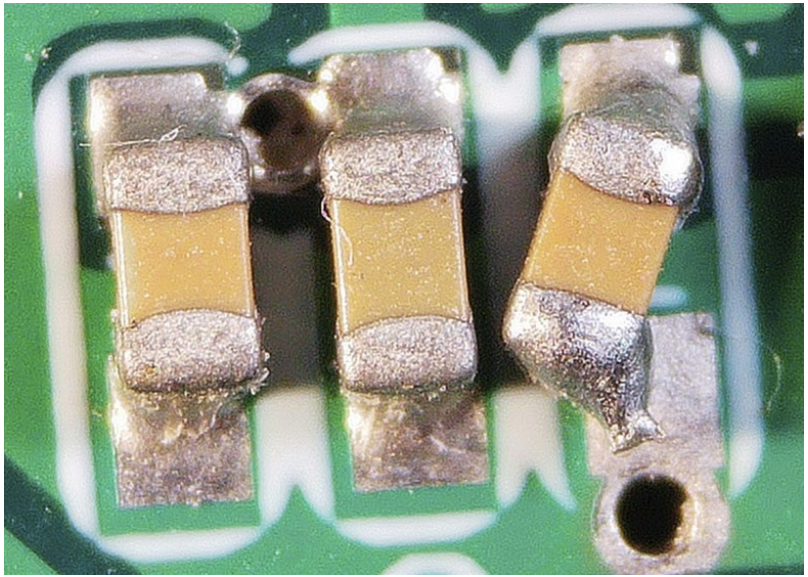
Factory Testing: Definitions

False Pass: when a defective product erroneously passes (even though it should have failed)

DPPM: Defective Parts Per Million

Factory Testing Basics

- Purpose: Detect manufacturing defects, such as **cold solder joint** or **misaligned component**



Factory Testing: Why it matters

2022 RECALL

HYPER

Stackable GaN USB-C Chargers



65W / 100W

OVERHEATING

Product design issue identified
Potential fire hazard
Approx. three confirmed incidents

Design and thermal risks can trigger a market recall.

Ref : https://reurl.cc/k9gGYn

OCT 2024 RECALL

ANKER

Portable Charging Power Banks



≈ 2,100 units

FIRE & BURN HAZARD

Lithium-ion batteries could overheat
28 reported incidents
Two reported burn injuries

Charging products require robust safety validation.

Ref : https://reurl.cc/dOAKjy

NOV 2023 RECALL

BELKIN

BoostCharge Pro Power Bank 10K



≈ 83,500 units

FIRE HAZARD

Lithium-ion battery could overheat
One reported product fire
House fire with property damage

A field failure can affect safety and customer trust.

Ref : https://reurl.cc/dOAKkg

A product recall can cost far more than investing in proper validation.

Factory Testing Basics

- For USB-C connector testing, it is critical that **all pins are connected**, and **none of them are shorted**

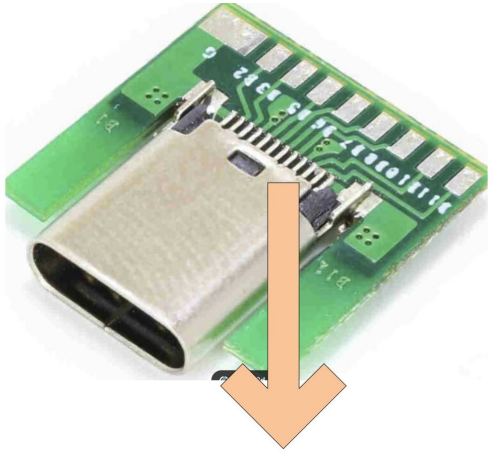
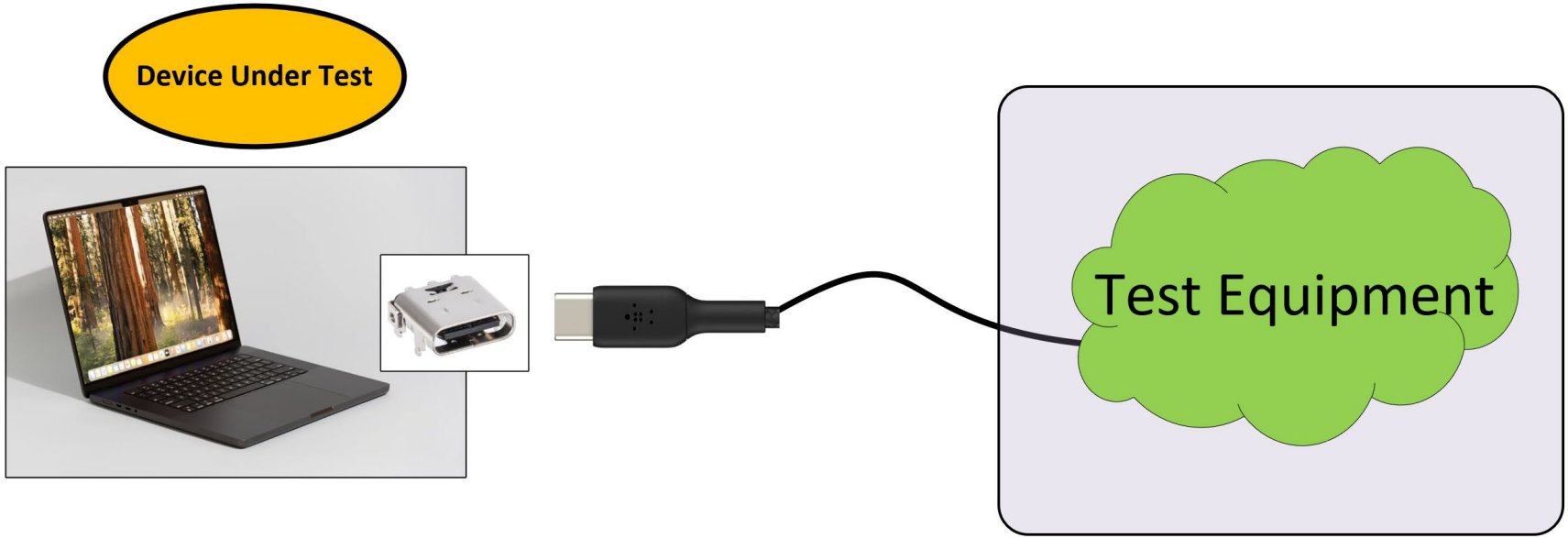


Figure 2-1 USB Type-C Receptacle Interface (Front View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

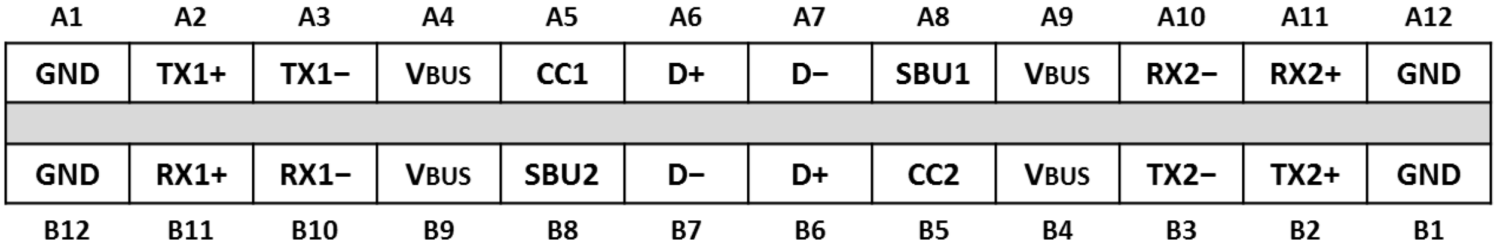
Factory Test Setup



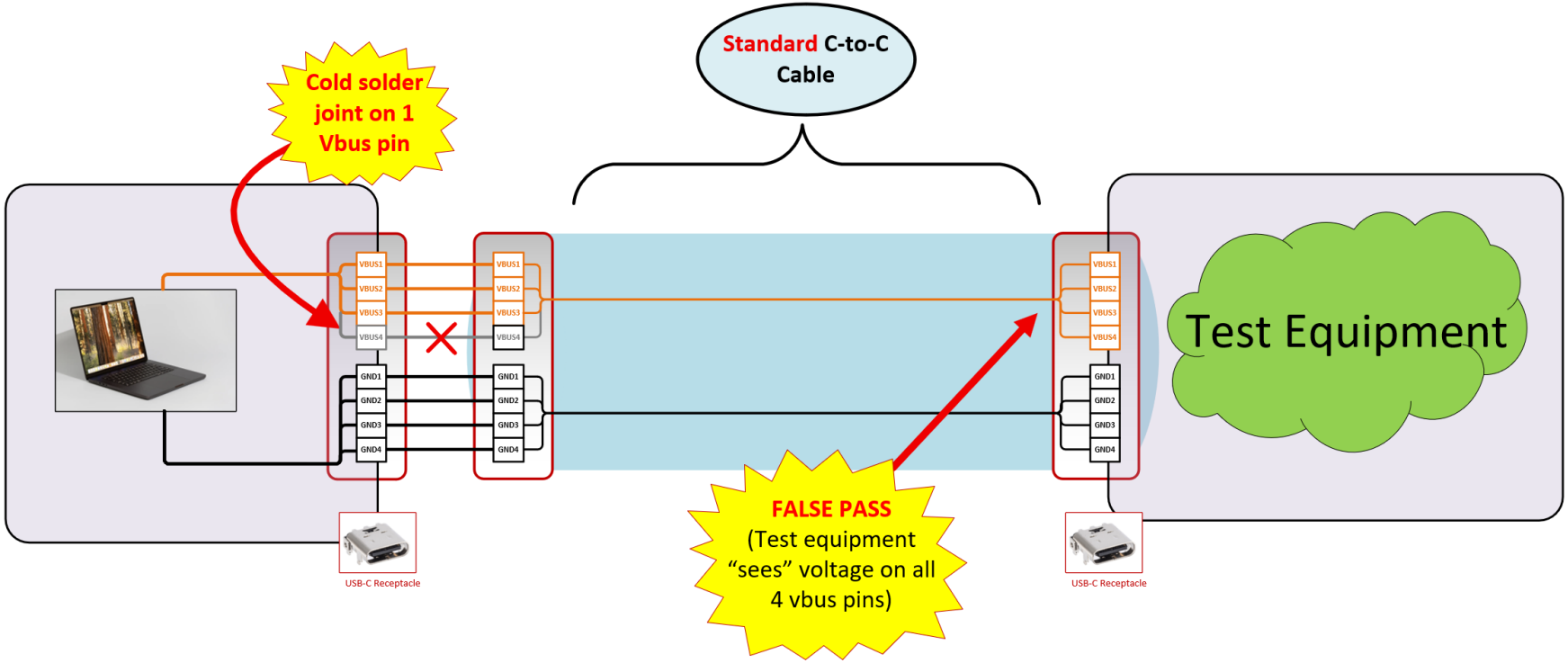
Factory Test Example: Defect on Vbus

- Question: What happens if one (and only one) of the VBUS pins is not making proper contact?

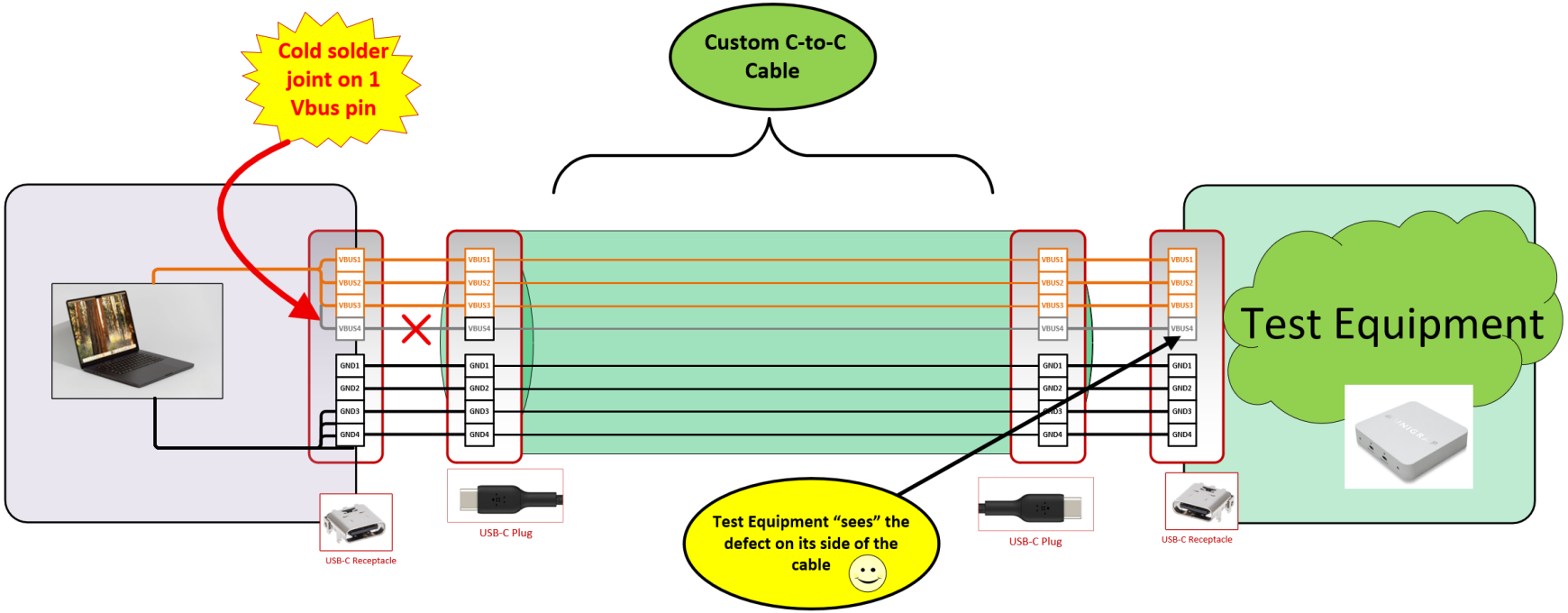
Figure 2-1 USB Type-C Receptacle Interface (Front View)



Factory Test Example: Defect on Vbus



Factory Test Example: Defect on Vbus



Factory Test Example: Defect on Vbus

Takeaway:

To detect a **single-pin defect** on ***Vbus*** or ***GND***, the test equipment must have **independent visibility** of all 8 of these pins (4 vbus and 4 gnd).

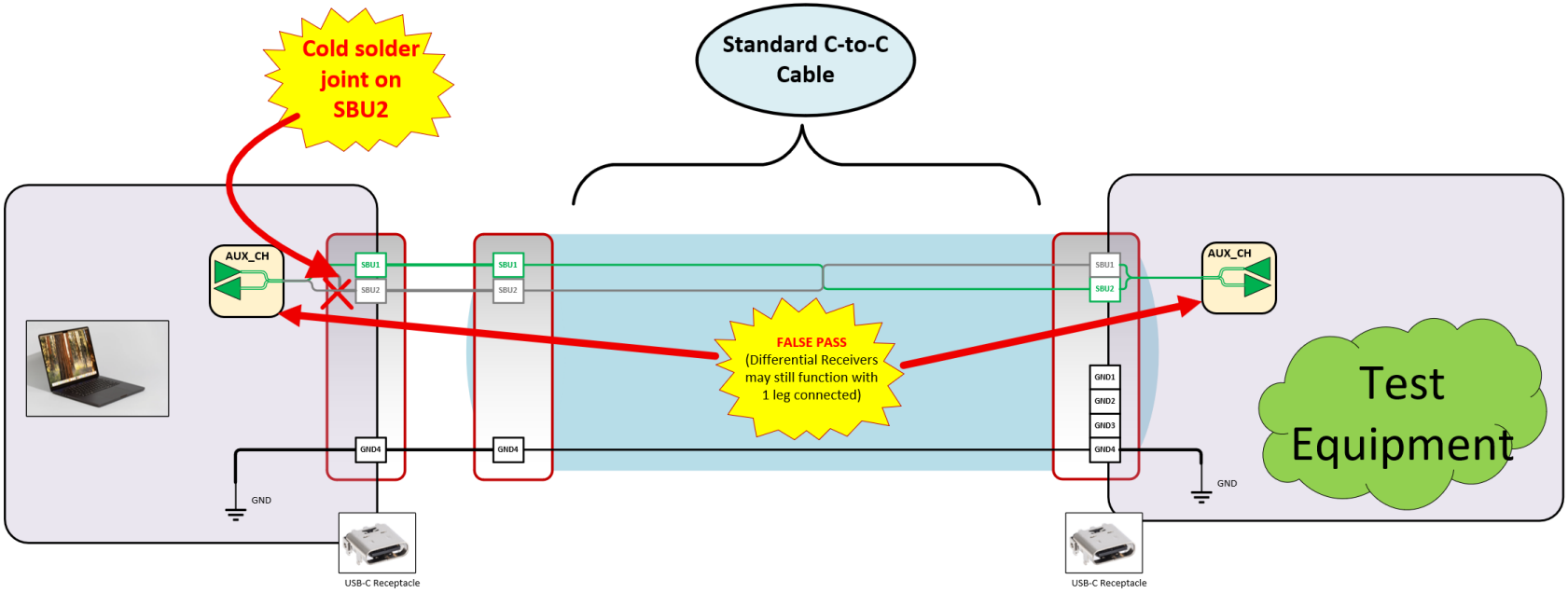
Factory Test Example: Defect on SBU

- Question: What happens if one (and only one) of the **SBU** pins is not making proper contact?

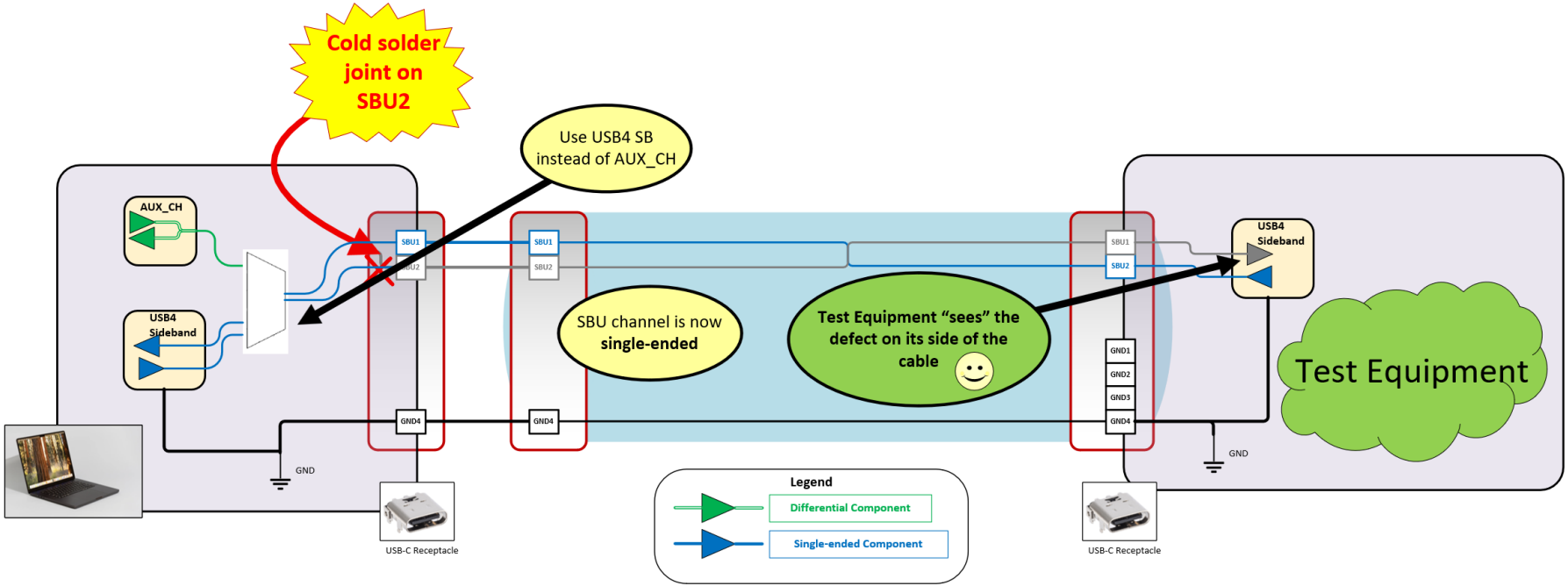
Figure 2-1 USB Type-C Receptacle Interface (Front View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Factory Test Example: Defect on SBU



Factory Test Example: Defect on SBU



Factory Test Example: Defect on SBU

Takeaway:

The most reliable way to detect **single-pin defects** on ***SBU*** is to configure these pins for a **single-ended application** (for example, USB4)

Factory Test

- Question: What about the other pins??

Figure 2-1 USB Type-C Receptacle Interface (Front View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Factory Testing: Unigraf UTC-274

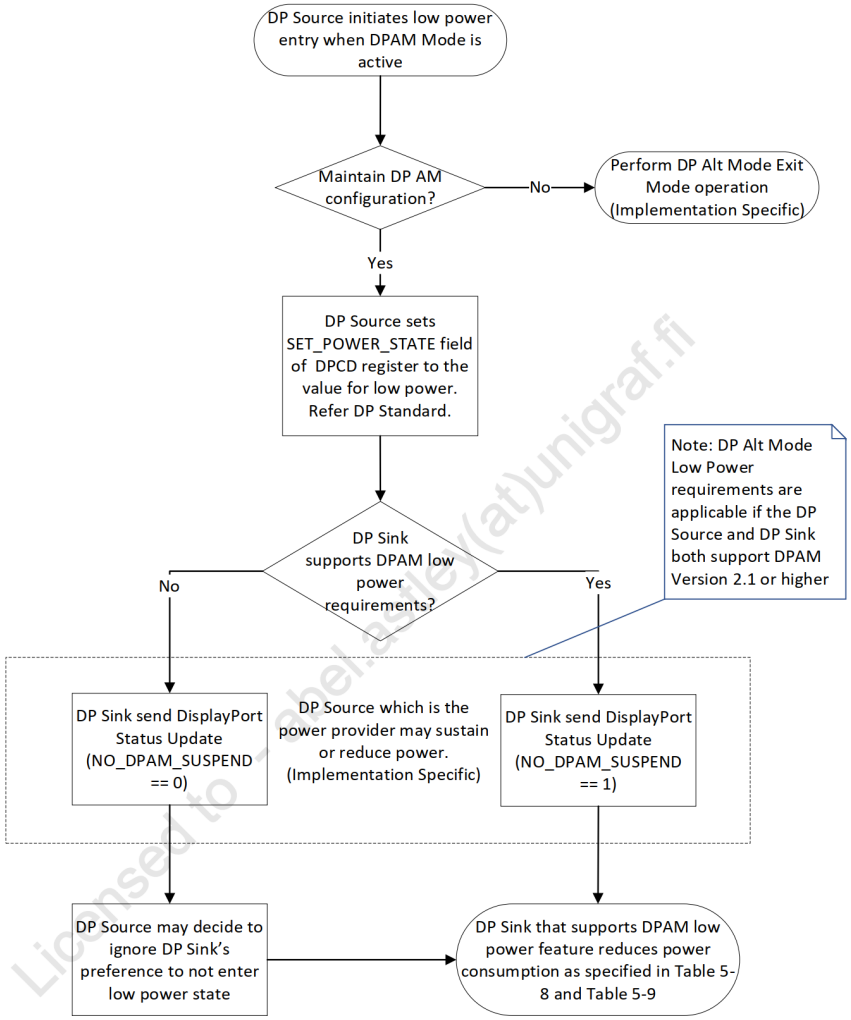
- ✓ **Purpose-built** for production environments
- ✓ Reliably detects **single-pin defects** on **all 24** USB-C pins
- ✓ Cost-effective for **large-scale deployments**
- ✓ Automatable



Recent Changes

Noteworthy updates to *USB PD* and *DisplayPort Alternate Mode* Specifications

DPAM Suspend

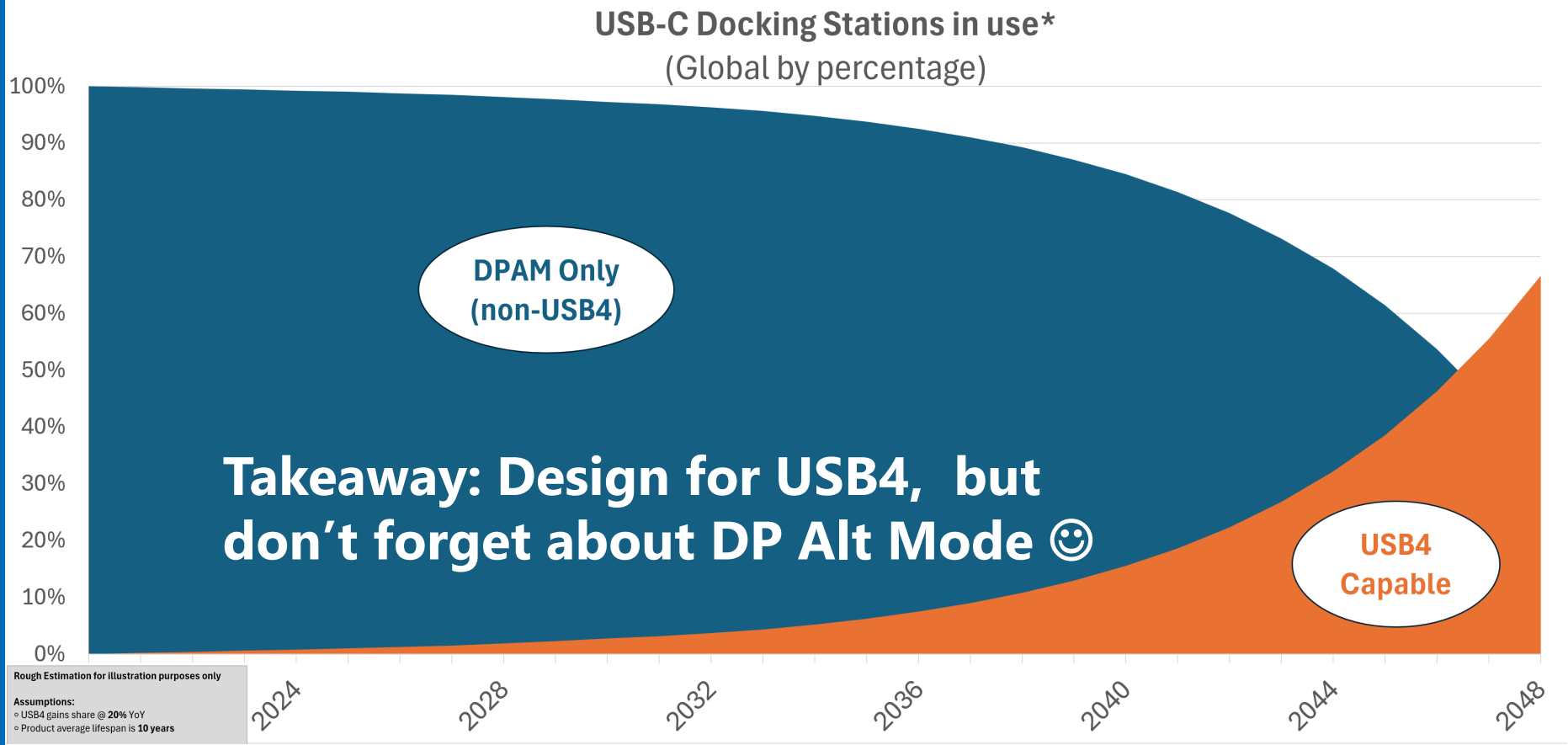


Licensed to ... abel.astley(at)unigraf.fi

Figure 6-1: High-level example DP Alt Mode low power flow with a bus powered UFP_U/DP Sink

USB4

VESA



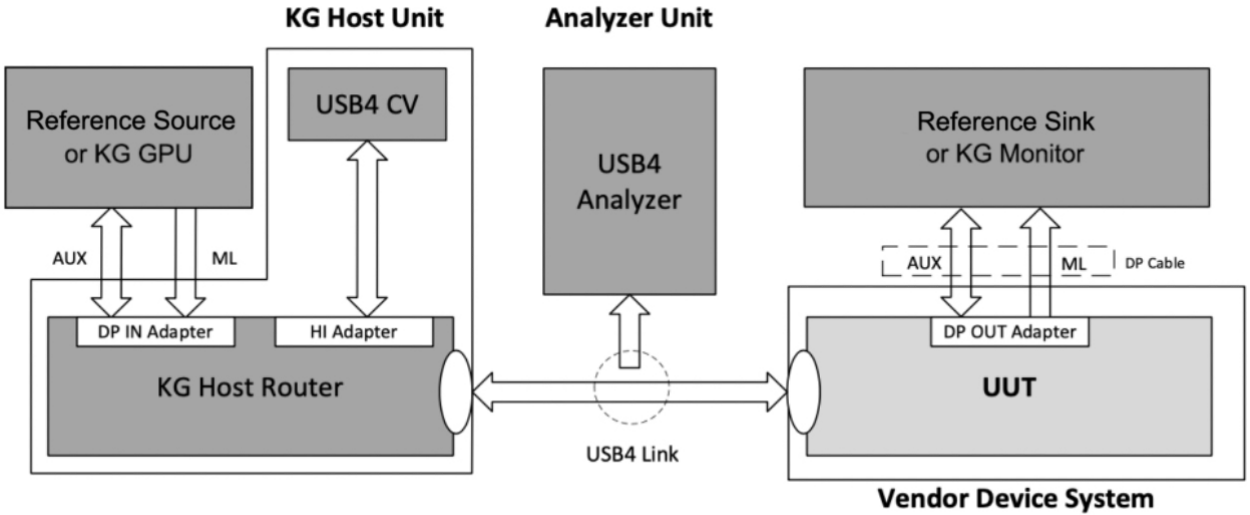
Takeaway: Design for USB4, but don't forget about DP Alt Mode ☺

Rough Estimation for illustration purposes only

Assumptions:
- USB4 gains share @ **20%** YoY
- Product average lifespan is **10 years**

USB4 Testing

- From *USB4 DP Tunneling CTS Rev 2.6*



UCD-500 Gen 3

16K DP 2.1b Generator & Analyzer

- DP 2.1b Sinks and Sources up to 8K@60Hz
  (16K@60Hz with DSC up to UHBR 20 Bit Rate)
- Supports DP and USB-C connectors
- GPIO interface for external control
- New fan cooler and chassis design
- Adaptive Sync, DSC, FEC and LTTPR support
- DP 2.1b and DP 1.4a Link Layer CTS Tool including DSC, LTTPR,
  DisplayID/EDID and Adaptive-Sync
- MST (up to 4 streams) with MST CTS Source and Branch DUT
  (full test set for Branch scheduled release in 4Q 2026)
- HDCP 2.3 Compliance Test Device for Transmitters, Receivers and Repeaters
- Color depth 6 to 16bpc
- Capture memory 16GB
- Now featuring Link Analyzer (monitor), *Panel Replay and eDP 1.5 test functions (eDP 2.0 scheduled release in 4Q 2026)

16K UHD

DP 2.1 LL CTS

HDCP 2.3 CTS











*Demo video on Youtube

Summary

Summary

- Factory testing mistakes are costly; don’t skimp on test engineering development or equipment

- For questions on USB-C product design or testing, don’t hesitate to reach out to us at www.unigraf.fi

QA

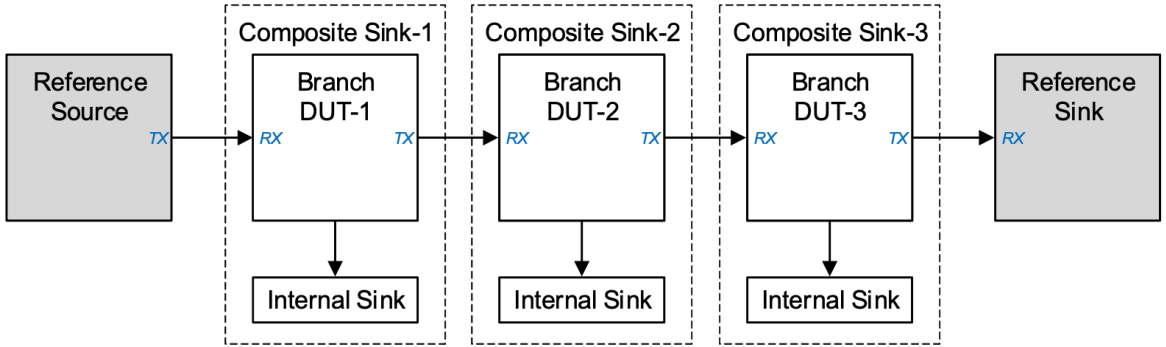
Compliance Testing

VESA PlugTest Events

- Provide significant value to VESA compliance program and member companies, particularly as new capabilities and products are deployed.
- Demonstrate and improve traditional interoperability
- Test Native DP and DP Alt Mode over USB Type-C™ products
  - UHBR rates, DSC, New MST Link Layer Tests, FEC, DisplayHDR and other new capabilities
  - Verify Test Equipment Correlation
- VESA hosted two successful PlugTests in 2025 (Taiwan and US)
- VESA hosts two PlugTests in 2026
  - Honolulu, Hawaii USA: **May 2026 (completed)**
  - Taipei, Taiwan: **October 19-23, 2026 (next week)**

Multi-Stream Transport (MST) Compliance Testing Enhancements

- After over a year of specification and test equipment test development VESA is preparing to release its biggest MST test update since DP 1.2. With the introduction of UHBR20 + DSC, users can now daisy chain multiple 4K/120Hz displays from a single output connector
- The unique DP capability of driving multiple daisy chained displays with a single output connection/cable is increasingly the most popular feature of DP for end users
- To further improve end user experience with MST configurations, VESA's latest DP Link Layer Compliance Test Specification adds dozens of new MST source/sink tests to verify products are implemented according to DP specifications



DP 2.1a LL CTS Composite Sink (Daisy-chainable Sink) Setup 3

DP54, DP80 and DP80LL Cable Specifications and Certification program

- Work on Enhanced DP cable and connector specifications and test requirements started in 2021 to ensure high performance connectors and cables would be available for products supporting UHBR rates
- DP54 and DP80 Certified cables provide added assurance of proper operation at the highest link rates (UHBR10, UHBR13.5 and UHBR20 Gbps).
- DP80LL active LRD cable CTS and certification added to provide UHBR20 Gbps rate support for longer cables (can support ~3 meter cables)
  - Linear Redrivers (LRD) are level boosting amplifiers that boost signal transmission over longer distances
- Over 150 Enhanced DP cables and connectors have been certified since launch of the Enhanced DP cable and connector certification programs

Product certifications* 2024/2025/2026

Products	2024	2025	2026
DP Sources	93	136	81
DP Sinks	491	428	362
DP Cables	70	57	34
DisplayHDR	556	582	528
ClearMR	53	71	68
AdaptiveSync	75	113	122

*Note: Numbers are base model certs not including family models. Updates to Compliance Management System (CMS) will include feature to count family models in the future.

DisplayPort Link Testing
Source CDF Tool

Overview

VESA Workshop

Oct 12 2026

What is a DisplayPort CDF

- **CDF** stands for Capability Declaration Form.
- A **CDF** is an official document or electronic form that a product manufacturer (OEM or brand) fills out and submits when seeking official DisplayPort Certification.
- **Purpose:** It serves as a detailed checklist recording all the exact capabilities, hardware features, and specifications supported by a DisplayPort transmitter (source, like a graphics card) or receiver (sink, like a monitor).
- **Authorized Test Centers** (ATCs) use the data entered into the CDF to configure automated testing equipment. The test equipment dynamically builds test parameters to verify that the device actually behaves according to the capabilities claimed in its CDF.

Source CDF Tool

The **Source CDF Tool** is an active Excel Spreadsheet but can be used without enabling Macros

Source CDF Tool

The **Source CDF Tool** is available to VESA members on the VESA Causeway Test Implementation Subgroup Page

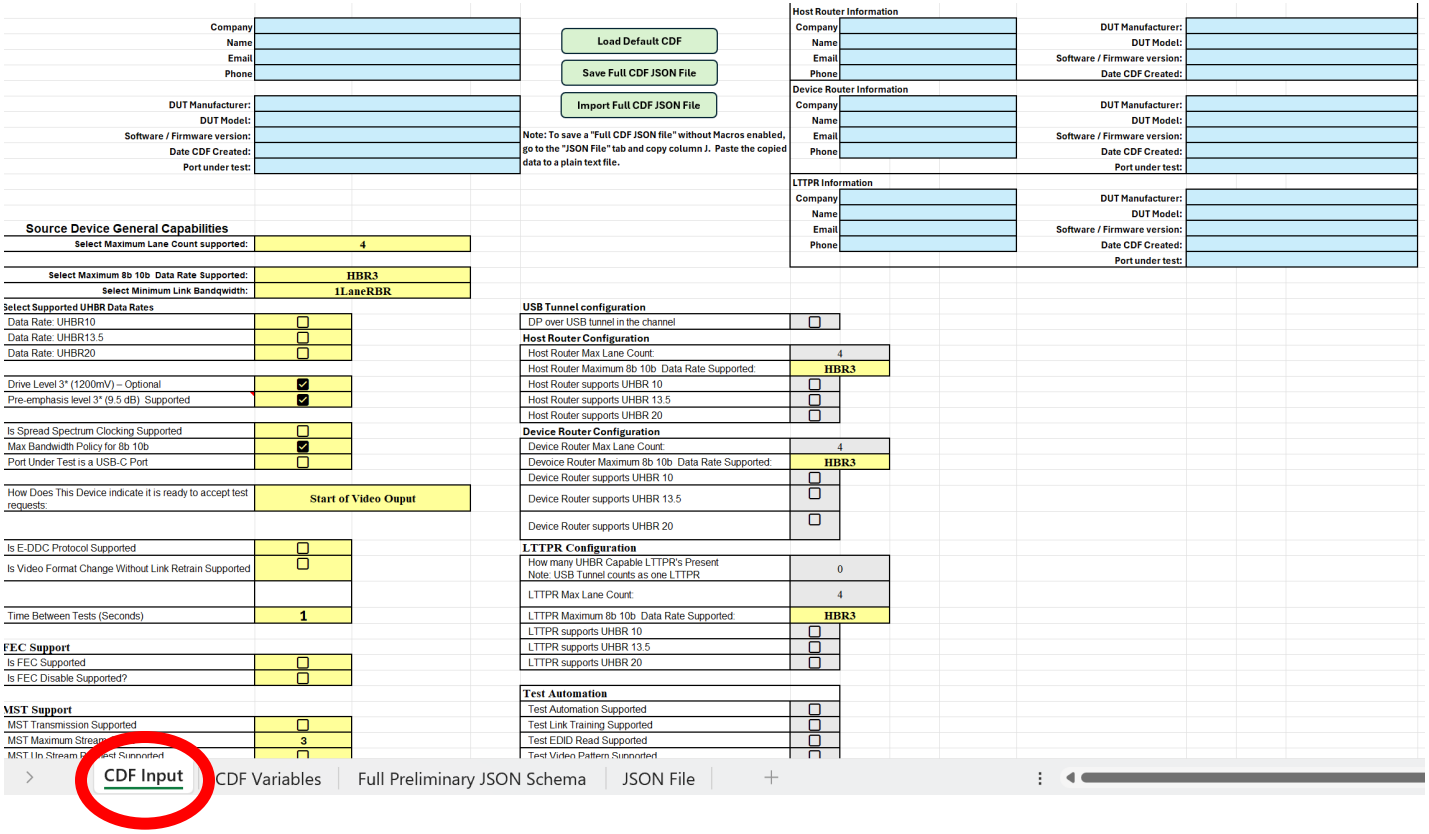
SourceCDFTool_Beta_xxxx_xx_2026.xlsm

Source CDF Tool

The **Source CDF Tool** creates a CDF file in json format that can be imported and used with the two approved Link Test Equipment:
UCD500 and **M42d / M42de**

Source CDF Tool

The Source CDF Tool takes user input in the first “CDF Input” tab



Company	
Name	
Email	
Phone	
DUT Manufacturer:	
DUT Model:	
Software / Firmware version:	
Date CDF Created:	
Port under test:	

Load Default CDF

Save Full CDF JSON File

Import Full CDF JSON File

Note: To save a "Full CDF JSON file" without Macros enabled, go to the "JSON File" tab and copy column J. Paste the copied data to a plain text file.

Host Router Information			
Company		DUT Manufacturer:	
Name		DUT Model:	
Email		Software / Firmware version:	
Phone		Date CDF Created:	
Device Router Information			
Company		DUT Manufacturer:	
Name		DUT Model:	
Email		Software / Firmware version:	
Phone		Date CDF Created:	
		Port under test:	
LTTPR Information			
Company		DUT Manufacturer:	
Name		DUT Model:	
Email		Software / Firmware version:	
Phone		Date CDF Created:	
		Port under test:	

Source Device General Capabilities

Select Maximum Lane Count supported:	4
Select Maximum 8b 10b Data Rate Supported:	HBR3
Select Minimum Link Bandqwidth:	1LaneRBR

Select Supported UHBR Data Rates	
Data Rate: UHBR10	☐
Data Rate: UHBR13.5	☐
Data Rate: UHBR20	☐
Drive Level 3* (1200mV) – Optional	☑
Pre-emphasis level 3* (9.5 dB) Supported	☑
Is Spread Spectrum Clocking Supported	☐
Max Bandwidth Policy for 8b 10b	☑
Port Under Test is a USB-C Port	☐
How Does This Device indicate it is ready to accept test requests:	Start of Video Ouput
Is E-DDC Protocol Supported	☐
Is Video Format Change Without Link Retrain Supported	☐
Time Between Tests (Seconds)	1

FEC Support

Is FEC Supported	☐
Is FEC Disable Supported?	☐

MST Support

MST Transmission Supported	☐
MST Maximum Stream	3
MST Up Stream Request Supported	☐

USB Tunnel configuration	
DP over USB tunnel in the channel	☐

Host Router Configuration	
Host Router Max Lane Count:	4
Host Router Maximum 8b 10b Data Rate Supported:	HBR3
Host Router supports UHBR 10	☐
Host Router supports UHBR 13.5	☐
Host Router supports UHBR 20	☐

Device Router Configuration	
Device Router Max Lane Count:	4
Devoice Router Maximum 8b 10b Data Rate Supported:	HBR3
Device Router supports UHBR 10	☐
Device Router supports UHBR 13.5	☐
Device Router supports UHBR 20	☐

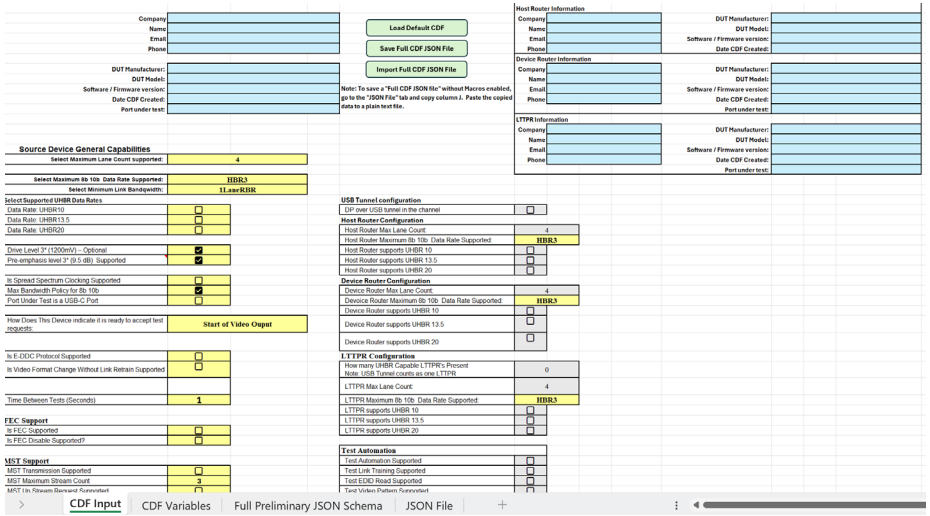
LTTPR Configuration	
How many UHBR Capable LTTPR's Present Note: USB Tunnel counts as one LTTPR	0
LTTPR Max Lane Count:	4
LTTPR Maximum 8b 10b Data Rate Supported:	HBR3
LTTPR supports UHBR 10	☐
LTTPR supports UHBR 13.5	☐
LTTPR supports UHBR 20	☐

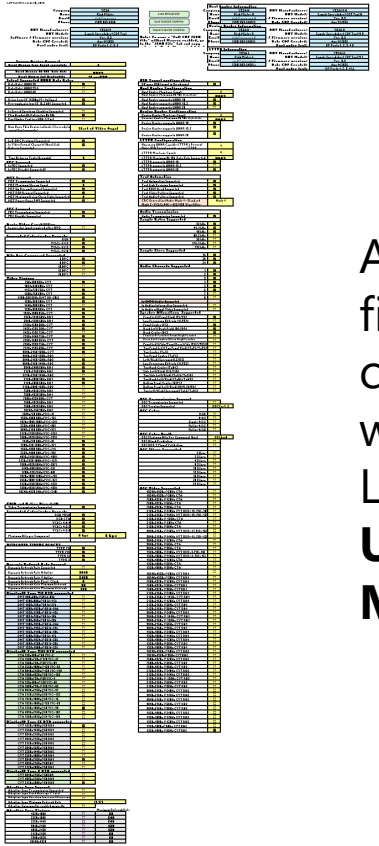
Test Automation	
Test Automation Supported	☐
Test Link Training Supported	☐
Test EDID Read Supported	☐
Test Video Pattern Supported	☐

CDF Input | CDF Variables | Full Preliminary JSON Schema | JSON File

Source CDF Tool

The Source CDF Tool allows full CDF User Input (up to 330+ input fields)





Allows input for every field required for compliance testing with the two approved Link test tools: **UCD500** and **M42d / M42de**

Source CDF Tool

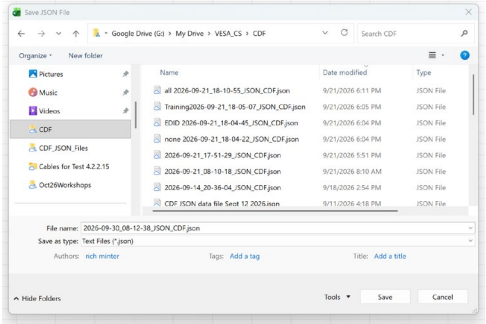
Company	
Name	
Email	
Phone	
DUT Manufacturer:	
DUT Model:	
Software / Firmware version:	
Date CDF Created:	
Port under test:	

Load Default CDF

Save Full CDF JSON File

Import Full CDF JSON File

Note: To save a "Full CDF JSON file" without Macros enabled, go to the "JSON File" tab and copy column J. Paste the copied data to a plain text file.



After completing the CDF input information, the CDF JSON file can be saved. A file save dialog will open to allow saving the CDF JSON file.

Note: If Macros are not enabled in your excel application, you may save the JSON file manually

Source CDF Tool

A comprehensive Source CDF Tool Tutorial has instructions to load CDF files into the Test Equipment

M42de: Instructions to load a CDF file see: Slide 16 - 22

UCD500: Instructions to load a CDF file see: Slide 23 - 27

The Source CDF Tool Tutorial is available on VESA Causeway Test Implementation Subgroup Documents Page:

Source CDF Tool Tutorial.ppsx

END

Summary

Summary

- VESA-based product shipments and certifications have transitioned from rapid growth to a steady state of high-volume output.
- DP 2.1 UHBR capable product development and certifications are in mass production and continue to grow
- VESA Enhanced cable and connector certification programs have been very successful with significant numbers of DP54, DP80 and now DP80LL cables certified
- MST continues to be a popular DP feature and with UHBR20 + DSC it can be used to drive multiple high resolutions displays at high refresh rates through a single connector
- Display Performance Standards adoption and certification have been extremely successful the last several years
- Development and adoption of new technologies continues to drive steady VESA membership growth

VESA

Questions?

Thank you to the contributors that made this event possible

- ***Thank you, speakers.*** For donating your time, energy and expertise
- ***Thank you, VESA organizing staff.*** The detailed work of arranging these events is tedious and tiring but critical.
- ***Thank you, attendees.*** You are why we are here. Let us know how we did in feedback and include any suggestions for additional topics or improvement for next year.

VESA

THANK YOU

DisplayPort.org
DisplayHDR.org
ClearMR.org
AdaptiveSync.org
VESA.org