# VESA 2026 Taipei Workshop

*October 16, 2026*

VESA

# Agenda

| Time | Topic | Speaker |
|---|---|---|
| 9:00am CT | Registration Opens | _ |
| 9:30am – 10:00am CT | Snacks & Refreshments | _ |
| 10:00am – 10:30am CT | VESA Overview and Standards Updates, Including DisplayPort v 2.1b | Jim Choate, Compliance Manager, VESA |
| 10:30am – 11:00am CT | DisplayPort Link Layer CTS v 2.1 MST Updates and Automotive Extension Services Updates | Alok Soni, Software Lead, Teledyne LeCroy |
| 11:00am – 11:30am CT | eDP and DP v 2.1 PHY CTS Overview and Updates | Abhijeet Shinde, Product Manager, Edge AI, Keysight |
| 11:30am – 12:00pm CT | VESA Display Panel Metrics Standards Overview | Cyan Chen, Global Business Lead, Display Technologies, Granite River Labs |
| 12:00pm – 1:00pm CT | Lunch | _ |
| 1:00pm – 1:30pm CT | LRD/Active Cable Testing and DP 2.1 Enhanced Connector Certification Challenges | Lexus Lee, Technical Program Manager, Allion Labs |
| 1:30pm – 2:15pm CT | Design Considerations for USB-C Products | Abel Astley, Head of USB Technology, Unigraf Oy |
| 2:15pm – 2:45pm CT | Break | _ |
| 2:45pm – 3:00pm CT | VESA Compliance Program | Jim Choate, Compliance Manager, VESA |
| 3:00pm – 3:10pm CT | Summary, Questions & Answers | Jim Choate, Compliance Manager, VESA |
| 3:10pm – 3:40pm CT | Demo Stations Overview | _ |

# VESA Overview and Standards Updates

**Jim Choate**
VESA Compliance Program Manager

# Agenda

- VESA Overview
- DisplayPort Overview
- VESA Technology Development Areas
- Summary

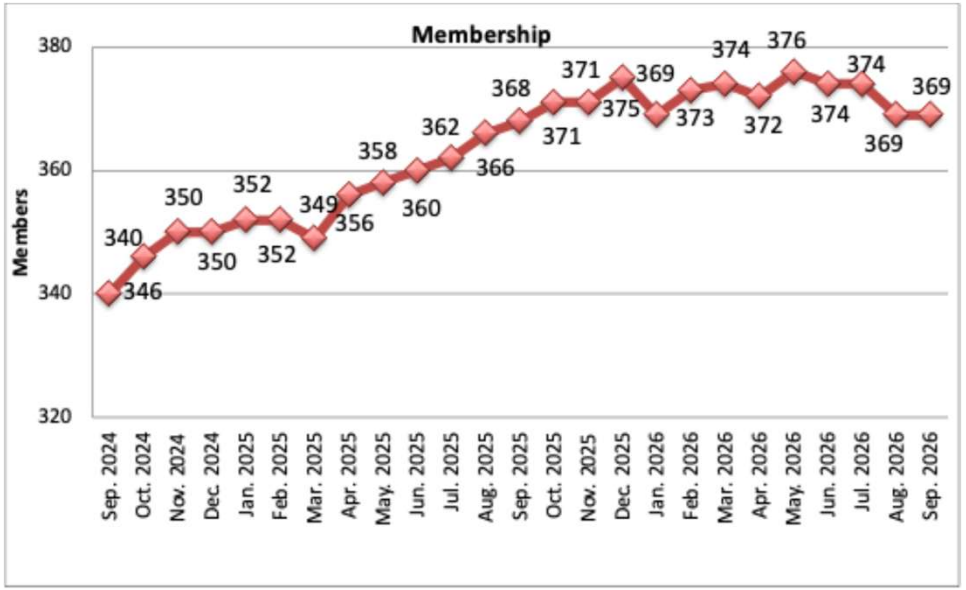
# VESA OVERVIEW

# VESA Vision

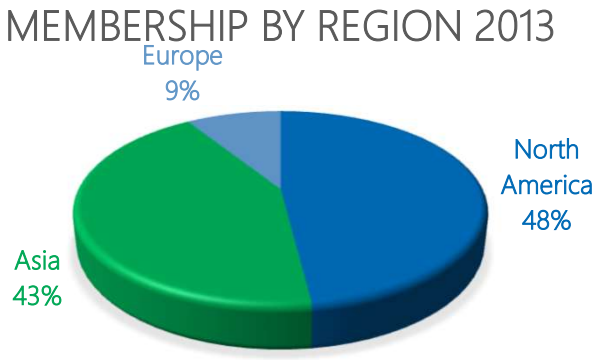
- VESA's vision is continual growth in technical standards development and evolution as an international trade association, with a worldwide membership driving standards initiatives, product implementations, and market implementation.

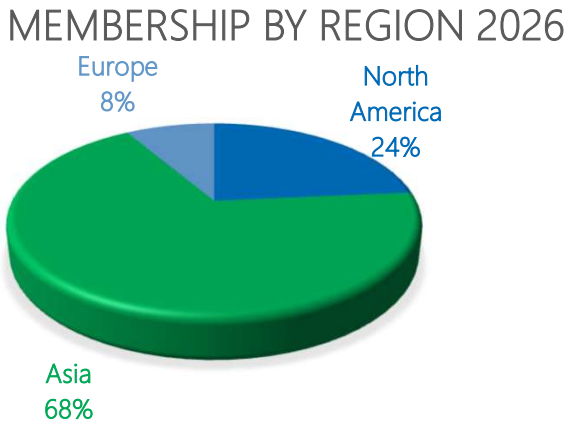
# About VESA

- A growing global industry alliance with 369 members. Continuous growth in membership.
- Mission to develop, promote and support ecosystem of vendors and ***certified*** interoperable products for the electronics industry.
- *Develops OPEN standards, contribution is open to all companies at all stages of development*



# VESA Membership Growth by %

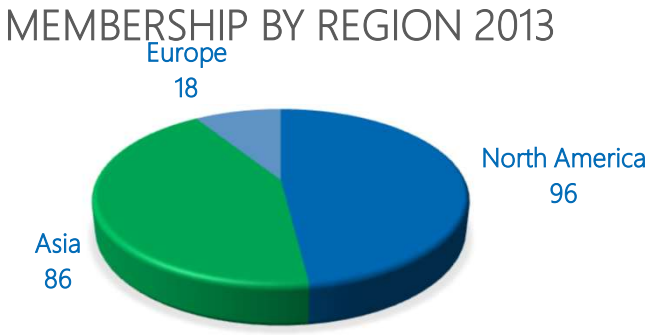


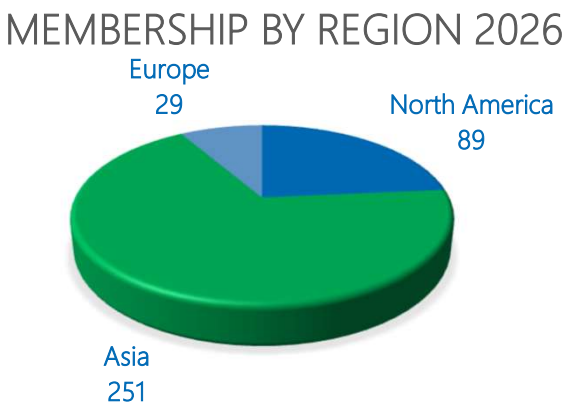




- **Total Ecosystem:** 200 total corporate members worldwide.
- **Western Core:** North American companies hold the largest single regional share.
- **Balanced Footprint:** Early-stage adoption driven primarily by foundational US chipmakers and device OEMs.

- **Total Ecosystem:** Expanded to 369 total corporate members.
- **Epicenter Shift:** Asian tech hubs now represent over two-thirds of the standards body.
- **Global Standard:** Widespread international integration driven by the ubiquity of DisplayPort, DPAM, eDP, Display Panel Metrics (DPM)) and automotive display profiles.

# VESA Membership Growth by Total Companies




- The Illusion of Decline: A percentage-only view falsely suggests North American membership shrank by half (48% down to 24%).
- The Reality of Stability: In absolute numbers, North American membership stayed completely robust and stable (89 vs 96 companies). Europe membership has grown 61% in this interval.
- The Growth Engine: The structural shift is entirely additive—fueled by 165 new Asian companies joining the ecosystem to support massive display infrastructure expansion.

# VESA Standards Enable Many Market Segments…



Monitors, PCs and laptops



Gaming consoles and headsets



Smartphones and tablets



Automotive

*NEW: VESA DP AE specification and DP AE CTS*




Multi-Stream Transport (MST)

# VESA Local Asian Support Capability

- VESA continues to provide local support to Asia to address growing regional membership needs
- **Kellen** is VESA's Representative in Asia
- This partnership provide members with a communication option in their native language. Kellen handles membership related activities including, new membership requests, renewals, event support and translation of VESA member messaging, etc.
- AsiaVESA@kellencompany.com or at +86 10 6580 0670

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# DisplayPort ™ Overview

# DisplayPort Market Penetration

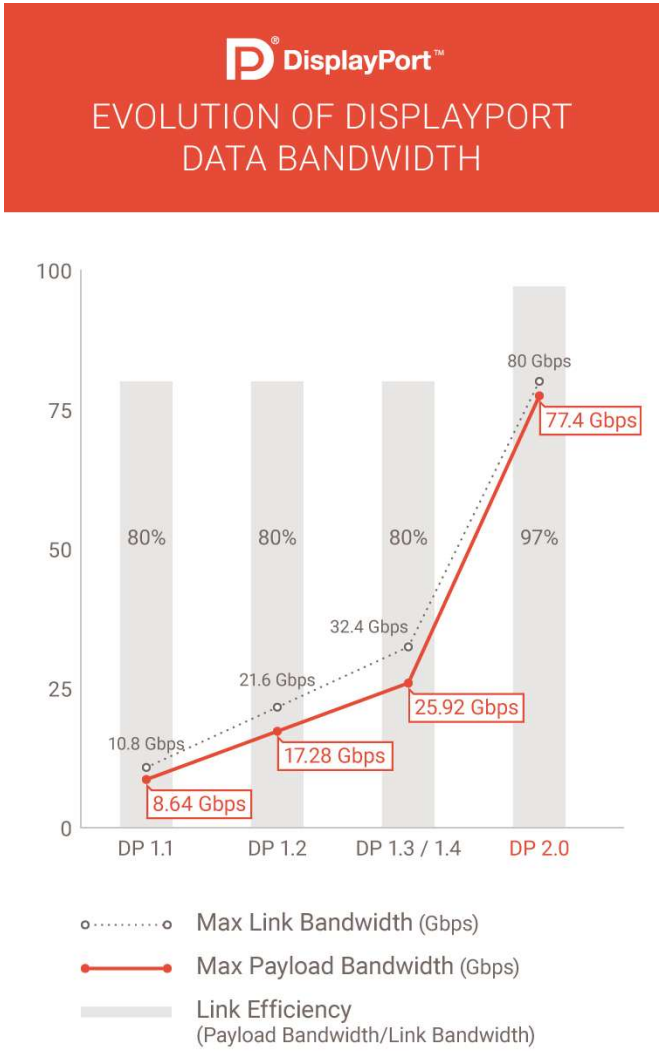
- DisplayPort adoption continues to grow in 2026
- DisplayPort and DisplayPort Alternate Mode over USB-C
  - The common monitor interface for personal computers
  - Supported on the USB-C interfaces
    - Mandated for USB4 and Thunderbolt
  - Automotive integration with DP AE specification
  - Mobile phones with USB-C
  - ***New:*** *AR/VR standard and CTS*
- Embedded DisplayPort (eDP)
  - >95% to near 100% penetration in notebook PCs, used in many high-end tablets and automotive

# DisplayPort 2.1b Summary

- DisplayPort v2.1b was released in December 2025
- Major features added in v2.0/v2.1/v2.1a/v2.1b:
  - Added 128b/132b DP channel coding (UHBR rates)
  - Increase in data bandwidth performance (almost 3X) with new link rates up to 20 Gbps/lane
  - Panel Replay, similar to PSR (Panel Self Refresh) used for eDP
  - DSC support mandated
  - Enhanced DP connectors and cables (DP40, DP54 and DP80)
  - DP PHY specification alignment with USB4 PHY specification
  - Updated DP to HDMI v2.1 or higher protocol converter (PCON)
  - Corrects errata
  - Replaces DP40 cables with DP54 to expand higher rate cable length
  - Expanded Tunneling capability
  - Updates for DP AE Services specification
  - DP80LL cable spec section (active cables for longer reach with lower loss)
  - LRD Active Cable Electrical Mandate section

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- DisplayPort 2.1b enables up to 3X increase in video bandwidth performance vs DP 1.4
- UHBR10, UHBR13.5 and UHBR20 provides up to 80Gbps link bandwidth for 4 lanes at 20Gbps.
- First standard to support 8K resolution (7680 x 4320) at 60 Hz refresh rate with full-color 4:4:4 resolution, including with 30 bits per pixel (bpp) for HDR-10 support
- Beyond 8K resolutions achieved with maximum link rate to up to 20 Gbps/lane and more efficient 128b/132b channel coding



# DisplayPort 2.1 Link Layer CTS Summary

- DP 2.1 LL CTS v1.1 released 12/2025
- Major updates:
  - Updates to align with other published VESA standards and terminology
  - Incorporated many approved and published SCRs
    - For example: FEC, Audio, DisplayID, min Hblank/Vblank, etc
  - Addition of new Source, Sink and Branch device MST tests (covered separately)
  - LTTPR emulation testing

# VESA Technology Development Areas

# VESA technology development

VESA members are collaborating on several key technology areas

- Embedded DisplayPort - v2.0 (published Sept 2024)
- DP Tunneling over USB4 – compliance testing has begun
- AR/VR Task Group
  - Focused on creating solutions roadmap to meet performance, power and implementation requirements for future AR/VR needs. Specification is released. Work on CTS underway
- DP Automotive Extension Task Group
  - Working with automotive industry to address needs for high-resolution performance in this market segment
  - Working on DP AE CTS and testing
- MST Compliance Test Updates
  - DP 2.1 LL CTS v1.1 released and new tests became normative 7/7/2029
- Display Performance Metrics Task Group
  - DisplayHDR, ClearMR, AdaptiveSync updates and proposals for future capabilities

# VESA Logos and Marketing Guidelines

# VESA Membership Allows Use of VESA Logos

- When your product passes certification company can use VESA logo to show customers proof of quality

*Cable Logos include:*

*DP Product Logos include:*

*Display Logos include:*



# VESA DisplayPort MST CTS 改進

**Alok Soni/Neal Kendall**
Teledyne LeCroy
*2026年10月16日 – 台北，台灣*

# MST Source CTS Updates Since CTS Rev 1.1

## Agenda

- Overview of CTS updates since Rev 1.1
- MST Source CTS updates
- MST Branch CTS updates
- Composite Sink CTS updates
- New Sink and Source tests
- Summary
- Q/A and feedback

# MST 來源 CTS 自 CTS 1.1 版以來的更新

## 議程.

- 自 Rev 1.1 以來的 CTS 更新概述
- MST 來源 CTS 更新
- MST 分支 CTS 更新
- 複合匯 CTS 更新
- 新的匯與源頭測試
- 摘要
- 問答與回饋

# MST Source CTS updates since CTS Rev 1.1

# MST 來源 CTS 自 CTS Rev 1.1 以來的更新

## MST CTS Coverage Summary

| Area | Rev 1.1 Tests | New Tests | Updated Tests |
|---|---|---|---|
| Source | 21 | 0 | 4 |
| Branch | 54 | 2 | 15 |
| Composite Sink | 48 | 1 | 14 |

## MST CTS 覆蓋摘要

| 面積 | Rev 1.1 測試 | 新測試 | 更新測試 |
|---|---|---|---|
| 資料來源 | 21 | 0 | 4 |
| 分支 | 54 | 2 | 15 |
| 複合合成匯 | 48 | 1 | 14 |

## CTS Updates - MST Source Device

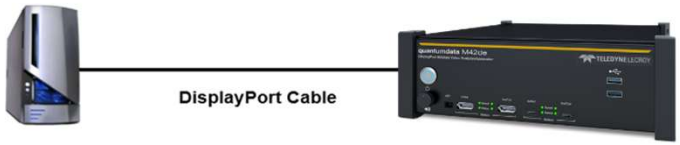
- MST Source Tests in Rev 1.1 CTS (21 Tests):
  - 4.10.1.1 to 4.10.1.21.
- MST Source Tests updates since Rev 1.1 CTS via approved SCRs.
  - 4.10.1.4
  - 4.10.1.8
  - 4.10.1.12
  - 4.10.1.21

## MST 來源 CTS 自 CTS Rev 1.1 以來的更新

- MST 來源測試於 1.1 版 CTS（共 21 次測試）：
  - 4.10.1.1 to 4.10.1.21.
- 自 1.1 版以來，MST 來源測試透過核准的 SCR 更新 CTS.
  - 4.10.1.4
  - 4.10.1.8
  - 4.10.1.12
  - 4.10.1.21

# CTS Updates - MST Source Device

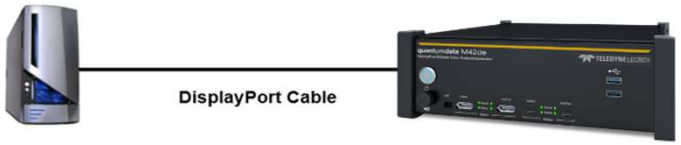
- How to run MST Source CTS:
  - Connect TE to Source DUT.




  - From Test Equipment software fill out CDF entry.
    - **Note**: Test Equipment automatically retrieves CDF entries from the VESA CDF JSON file.
  - Select MST Source Tests and then run them.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

# CTS 更新 - MST 來源裝置

- 如何運行 MST Source CTS:
  - 將 TE 連接到來源 DUT.




  - 從測試設備軟體填寫 CDF 條目.
    - **注意:測試設備會自動從 VESA CDF JSON 檔案中取得 CDF 條目**.
  - 選擇 MST 來源測試，然後執行它們。
  - 依照圖形使用者介面提示設定/驗證。
  - 測試執行完成後，產生 HTML 報告.

# CTS 更新 - MST 來源裝置

## MST 來源 CTS CDF 輸入細節

| S.No | 能力 | CDF登記 | 預設值 |
|---|---|---|---|
| 1 | 支援 MST 傳輸嗎？<br>選項：是，否 | MST_TRANS_SUPPORTED | 是的 |
| 2 | 最多支援的同時串流次數？<br>選項：1、2、3、4 | MST_MAX_STREAM_COUNT | 4 |
| 3 | Source DUT 會處理 Up 請求嗎？<br>選項：是，否 | MST_UP_REQUEST_SUPPORTED | 是的 |
| 4 | Source DUT 會處理 RSN Up 的請求嗎？<br>選項：是，否 | MST_RSN_REQUEST_SUPPORTED | 不 |
| 5 | 最多支援多少 Daisy 鏈條水槽數量？<br>選項：1、2、3、4 | MST_MAX_DAISY_CHAIN_SINK_SUPPORTED | 4 |
| 6 | Source DUT 會處理 Power Up Down Phy 的請求嗎？<br>選項：是，否 | MST_POWER_UP_DOWN_PHY_SUPPORTED | 是的 |

# CTS Updates - MST Branch Device

- MST Branch Device Tests in Rev 1.1 CTS (54 tests)
  - Branch Setup 1: 6.10.1.1 to 6.10.1.12 (12 tests)
  - Branch Setup 2: 6.10.2.1 to 6.10.2.10 (10 tests)
  - Branch Setup 3: 6.10.3.1 to 6.10.3.14 (14 tests)
  - Branch Setup4: 6.10.4.1 to 6.10.4.14 (14 tests)
  - Branch Setup 5: 6.10.5.1 to 6.10.5.4 （ 4 tests)
- MST Branch Device Tests updates since Rev 1.1 CTS via approved SCRs.
  - Branch Setup 1: 6.10.1.[1,5,6,7,8,9,10,11,12] (9 tests)
  - Branch Setup 2: 6.10.2.[3,6,7] (3 tests)
  - Branch Setup 3: 6.10.3.[3] (1 test)
  - Branch Setup 4: 6.10.4.[2,3] (2 tests)
- MST Branch Device Tests addition since Rev 1.1 CTS via approved SCRs
  - Branch Setup 2: 6.10.2.11: Verify the DFP port allocate payload allocation and de-allocation sequence
  - Branch Setup 3: 6.10.3.15: Verify the DFP port allocate payload allocation and de-allocation sequence.

# CTS 更新 - MST 分支裝置

- MST 分支裝置測試於 1.1 CTS 版本（54 次測試）.
  - 分支設置 1：6.10.1.1 至 6.10.1.12（12 次測試）
  - 分支設定 2：6.10.2.1 到 6.10.2.10（10 次測試）
  - 分支設定 3：6.10.3.1 至 6.10.3.14（14 次測試）
  - 分支設置4：6.10.4.1 到 6.10.4.14（14 次測試）
  - 分支設定 5：6.10.5.1 到 6.10.5.4（4 次測試）.
- MST 分支裝置測試自 1.1 版以來透過核准的 SCR 更新 CTS.
  - 分支設置1：6.10.1。[1,5,6,7,8,9,10,11,12]（9次測試）
  - 分支設置 2：6.10.2。[3,6,7]（3 次測試）
  - 分支設定 3：6.10.3。[3]（1 次測試）
  - 分支設置 4：6.10.4。[2,3]（2 次測試）.
- 自 1.1 版起，透過核准的 SCR 新增 MST 分支裝置測試.
  - 分支建立 2：6.10.2.11：驗證 DFP 埠口配置有效載荷分配與取消分配序列
  - 分支建立 3：6.10.3.15：驗證 DFP 埠口配置有效載荷分配與取消分配序列.

# CTS Updates - MST Branch Device

- How to run MST Branch CTS
  - Connect Test Equipment to Branch DUT in Setup 1.
  - From Test Equipment software fill out CDF entry.
  - Select MST Branch Setup 1 and then run.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.




# CTS 更新 - MST 分支裝置

- 如何運行 MST 分支 CTS.
  - 在設置 1 中將測試設備連接到分支 DUT。
  - 從測試設備軟體填寫 CDF 條目。
  - 選擇 MST 分支設定 1 然後執行。
  - 依照圖形使用者介面提示設定/驗證。
  - 測試執行完成後，產生 HTML 報告。

# CTS Updates - MST Branch Device

- How to run MST Branch CTS
  - Connect Test Equipment to Branch DUT in Setup 2.
  - From Test Equipment software fill out CDF entry.
  - Select MST Branch Setup 2 and then run.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

# CTS 更新 - MST 分支裝置

- 如何運行 MST 分支 CTS.
  - 在設定2中將測試設備連接到分支DUT。
  - 從測試設備軟體填寫 CDF 條目。
  - 選擇 MST 分支設定 2，然後執行。
  - 依照圖形使用者介面提示設定/驗證。
  - 測試執行完成後，產生 HTML 報告.



# CTS Updates - MST Branch Device

- How to run MST Branch CTS
  - Connect Test Equipment to Branch DUT in Setup 3.
  - From Test Equipment software fill out CDF entry.
  - Select MST Branch Setup 3 and then run.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

# CTS 更新 - MST 分支裝置

- 如何運行 MST 分支 CTS.
  - 在設定 3 中將測試設備連接到分支 DUT。
  - 從測試設備軟體填寫 CDF 條目。
  - 選擇 MST 分支設定 3 然後執行。
  - 依照圖形使用者介面提示設定/驗證。
  - 測試執行完成後，產生 HTML 報告。



# CTS Updates - MST Branch Device

- How to run MST Branch CTS
  - Connect Test Equipment to Branch DUT in Setup 4.
  - From Test Equipment software fill out CDF entry.
  - Select MST Branch Setup 2 and then run.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

# CTS 更新 - MST 分支裝置

- 如何運行 MST 分支 CTS.
  - 在設置4中將測試設備連接到分支DUT。
  - 從測試設備軟體填寫 CDF 條目。
  - 選擇 MST 分支設定 2，然後執行。
  - 依照圖形使用者介面提示設定/驗證。
  - 測試執行完成後，產生 HTML 報告。



# CTS Updates - MST Branch Device

- How to run MST Branch CTS
  - Connect Test Equipment to Branch DUT in Setup 5.
  - From Test Equipment software fill out CDF entry.
  - Select MST Branch Setup 5 and then run.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

# CTS 更新 - MST 分支裝置

- 如何運行 MST 分支 CTS.
  - 在設置 5 中將測試設備連接到分支 DUT。
  - 從測試設備軟體填寫 CDF 條目。
  - 選擇 MST 分支設定 5 然後執行。
  - 依照圖形使用者介面提示設定/驗證。
  - 測試執行完成後，產生 HTML 報告.



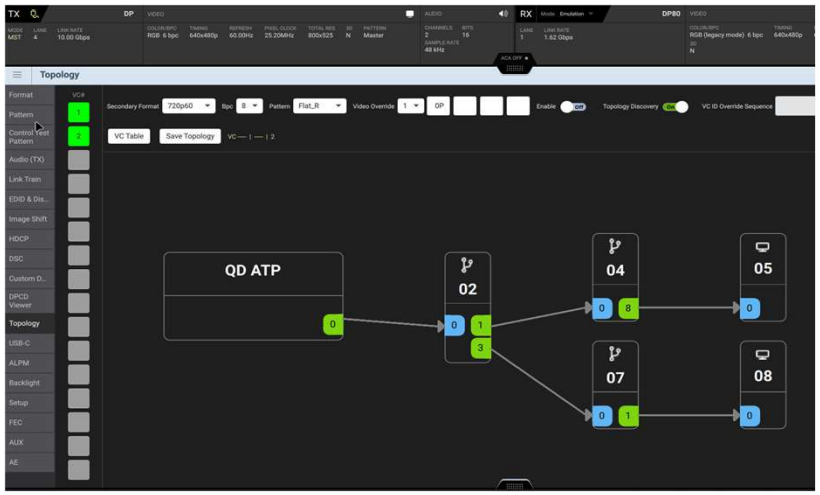
# CTS 更新 - MST 分支裝置

## MST 分支 CTS CDF 輸入細節

| S.No | 能力 | CDF登記 | 預設值 |
|---|---|---|---|
| 1 | 有多少個 DFP DP/USB-C 埠？<br>選項：1 至 4 | BRANCH_DUT_NO_OF_DFP_DPPORT | - |
| 2 | 連接至 TE 發射埠的 MST 裝置上行埠號<br>選項：0 到 16 | BRANCH_DUT_UFP_PORT_NUM_CONNECTED_TO_TE | - |
| 3 | MST 裝置下行埠號回 TE Rx 埠<br>選項：0 到 16 | BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_TE | - |
| 4 | MST 裝置下行埠號回 Sink1<br>選項：0 到 16 | BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK1 | - |
| 5 | MST 裝置下游埠號連接回 Sink2<br>選項：0 到 16 | BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK2 | - |
| 6 | MST 裝置下游埠號連接回 Sink3<br>選項：0 到 16 | BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK3 | - |
| 7 | MST 裝置下行埠號連接回 Sink4<br>選項：0 到 16 | BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK4 | - |
| 8 | Branch DUT 支援 CSN DFP 廣播嗎？<br>選項：真、假 | BRANCH_DUT_CSN_DFP_BROADCAST | 錯誤 |

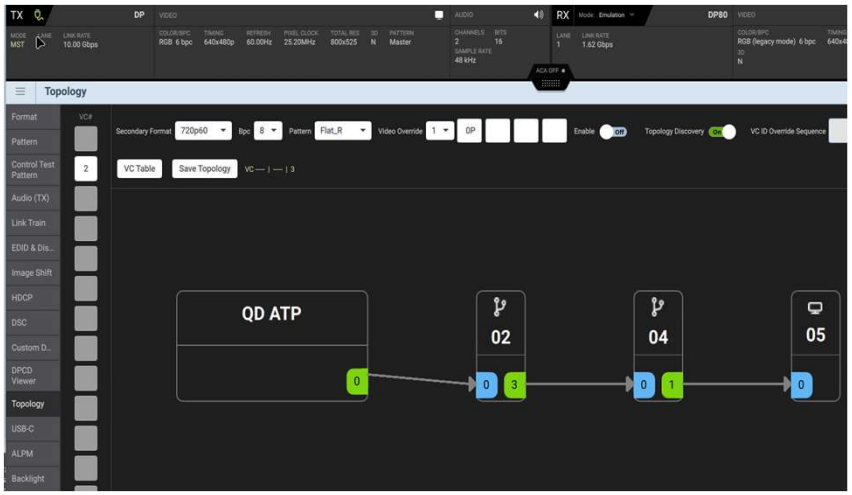
# CTS Updates - MST Branch Device

- How to get port number value for CDF.
  - Connect Test Equipment to Branch DUT in Setup 2.
  - See Test Equipment Generator topology for ports (below left).
  - Disconnect one DFP port and see Test Equipment generator topology (below right).
  - The disconnected DFP port number is 1.




# CTS 更新 - MST 分支裝置

- 如何取得 CDF 的埠號值.
  - 在設定2中將測試設備連接到分支DUT。
  - 請參見測試設備發電機拓撲以了解埠口。
  - 斷開一個 DFP 埠，查看測試設備產生器的拓撲。
  - 斷線的DFP埠號為1.

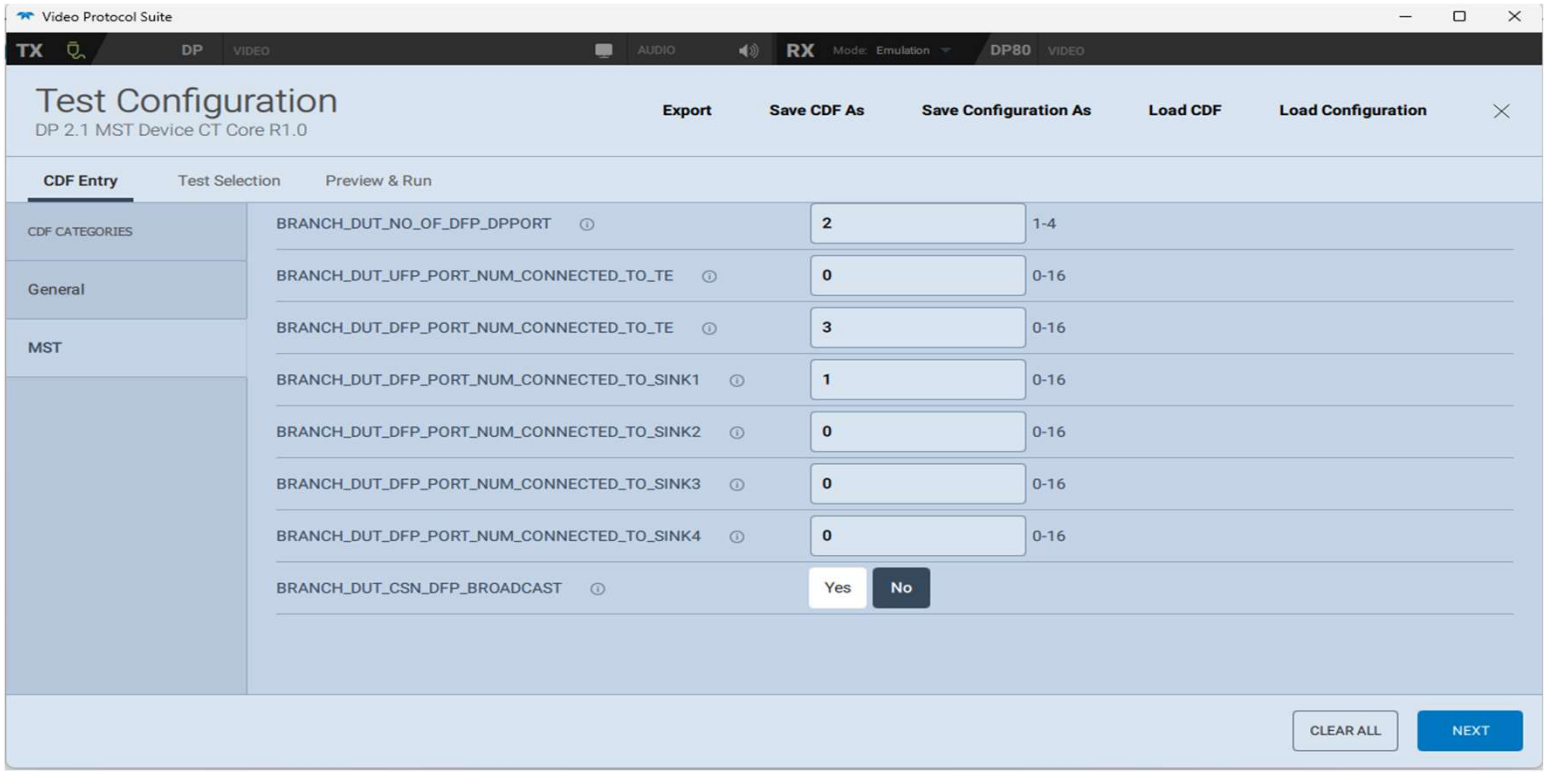


# CTS Updates - MST Branch Device

# CTS 更新 - MST 分支裝置

## MST Branch CTS CDF Sample for Setup 2:

## MST 分支 CTS CDF 設置 2 範例：



# CTS Updates – Composite Sink Device

- MST Composite Sink Device Tests in Rev 1.1 CTS (48 tests)
  - CS Setup 1: 6.10.6.1 to 6.10.6.21 (21 tests)
  - CS Setup 2: 6.10.7.1 to 6.10.7.19 (19 tests)
  - CS Setup 3: 6.10.8.1 to 6.10.8.5 ( 5 tests)
  - CS Setup 4: 6.10.9.1 to 6.10.9.3 ( 3 tests)
- MST Composite Sink Device Test updates since Rev 1.1 CTS via approved SCRs.
  - CS Setup 1: 6.10.6.[2,4,6,7,8,11,12] (7 tests)
  - CS Setup 2: 6.10.7.[1,3,5,6,7,10] (6 tests)
  - CS Setup 3: 6.10.8.[1] (1 test)
- MST Composite Sink Device Test additions since Rev 1.1 CTS via approved SCRs
  - CS Setup 1: 6.10.6.22: Verify the DFP port allocate payload allocation and de-allocation sequence

# CTS 更新 – 複合水槽裝置

- MST 複合匯槽裝置測試於 1.1 CTS 版本（48 次測試）.
  - CS Setup 1: 6.10.6.1 to 6.10.6.21 (21 tests)
  - CS Setup 2: 6.10.7.1 to 6.10.7.19 (19 tests)
  - CS Setup 3: 6.10.8.1 to 6.10.8.5 ( 5 tests)
  - CS Setup 4: 6.10.9.1 to 6.10.9.3 ( 3 tests)
- 自 1.1 版 CTS 以來，MST 複合匯設備測試透過核准的 SCR 更新.
  - CS Setup 1: 6.10.6.[2,4,6,7,8,11,12] (7 tests)
  - CS Setup 2: 6.10.7.[1,3,5,6,7,10] (6 tests)
  - CS Setup 3: 6.10.8.[1] (1 test)
- 自 1.1 CTS 版本以來，MST 複合匯裝置測試透過核准的 SCR 新增.
  - CS Setup 1: 6.10.6.22: 驗證 DFP 埠口配置有效載荷分配與取消分配序列

# CTS Updates - Composite Sink Device

- How to run MST Composite Sink Device CTS Setup 1
  - Connect Test Equipment to Composite Sink DUT in Setup 1.
  - From Test Equipment software fill out CDF entry.
  - Select MST Composite Sink Setup 1 Tests and then run them.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.




# CTS 更新 - 複合合成匯流裝置

- 如何執行 MST 複合匯線裝置 CTS 設定 1.
  - 在設置1中將測試設備連接到複合水槽DUT。
  - 從測試設備軟體填寫 CDF 條目。
  - 選擇 MST 複合匯水槽設定 1 測試，然後執行它們。
  - 依照圖形使用者介面提示設定/驗證。
  - 測試執行完成後，產生 HTML 報告。

# CTS Updates - Composite Sink Device

- How to run MST Composite Sink Device CTS Setup 2
  - Connect Test Equipment to Composite Sink DUT in Setup 2.
  - From Test Equipment software fill out CDF entry.
  - Select MST Composite Sink Setup 2 Tests and then run them.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

# CTS 更新 - 複合合成匯流裝置

- 如何執行 MST 複合匯線裝置 CTS 設定 2.
  - 在設置2中將測試設備連接到複合材料水槽的DUT。
  - 從測試設備軟體填寫 CDF 條目。
  - 選擇 MST 複合水槽設置 2 測試，然後執行它們。
  - 依照圖形使用者介面提示設定/驗證。
  - 測試執行完成後，產生 HTML 報告。



# CTS Updates - Composite Sink Device

- How to run MST Composite Sink Device CTS Setup 3
  - Connect Test Equipment to Composite Sink DUT in Setup 3.
  - From Test Equipment software fill out CDF entry.
  - Select MST Composite Sink Setup 3 Tests and then run them.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

# CTS 更新 - 複合合成匯流裝置

- 如何執行 MST 複合匯線裝置 CTS 設定 3.
  - 在設置3中將測試設備連接到複合水槽被測器。
  - 從測試設備軟體填寫 CDF 條目。
  - 選擇 MST 複合匯線設定 3 測試，然後執行它們。
  - 依照圖形使用者介面提示設定/驗證。
  - 測試執行完成後，產生 HTML 報告.



# CTS Updates - Composite Sink Device

- How to run MST Composite Sink Device CTS Setup 4
  - Connect Test Equipment to Composite Sink DUT in Setup 4.
  - From Test Equipment software fill out CDF entry.
  - Select MST Composite Sink Setup 4 Tests and then run them.
  - Follow graphical user interface prompt for setup/validation.
  - After test execution completes, generate the HTML report.

# CTS 更新 - 複合合成匯流裝置

- 如何執行 MST 複合匯線裝置 CTS 設定 4.
  - 在設置4中將測試設備連接到複合水槽DUT。
  - 從測試設備軟體填寫 CDF 條目。
  - 選擇 MST 複合水槽設置 4 測試，然後執行它們。
  - 依照圖形使用者介面提示設定/驗證。
  - 測試執行完成後，產生 HTML 報告.



# VESA複合匯線裝置 CTS 更新

## MST 複合匯 CTS CDF 輸入細節

| S.No | 能力 | CDF登記 | 預設值 |
|---|---|---|---|
| 1 | 有多少個 DFP DP/USB-C 埠？<br>選項：1 至 4 | BRANCH_DUT_NO_OF_DFP_DPPORT | - |
| 2 | 連接至 TE 發射埠的 MST 裝置上行埠號<br>選項：0 到 16 | BRANCH_DUT_UFP_PORT_NUM_CONNECTED_TO_TE | - |
| 3 | MST 裝置下行埠號回 TE Rx 埠<br>選項：0 到 16 | BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_TE | - |
| 4 | MST 裝置下行埠號回 Sink1<br>選項：0 到 16 | BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK1 | - |
| 5 | MST 裝置下游埠號連接回 Sink2<br>選項：0 到 16 | BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK2 | - |
| 6 | MST 裝置下游埠號連接回 Sink3<br>選項：0 到 16 | BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK3 | - |
| 7 | MST 裝置下行埠號連接回 Sink4<br>選項：0 到 16 | BRANCH_DUT_DFP_PORT_NUM_CONNECTED_TO_SINK4 | - |
| 8 | Branch DUT 支援 CSN DFP 廣播嗎？<br>選項：真、假 否 | BRANCH_DUT_CSN_DFP_BROADCAST | 錯誤 |

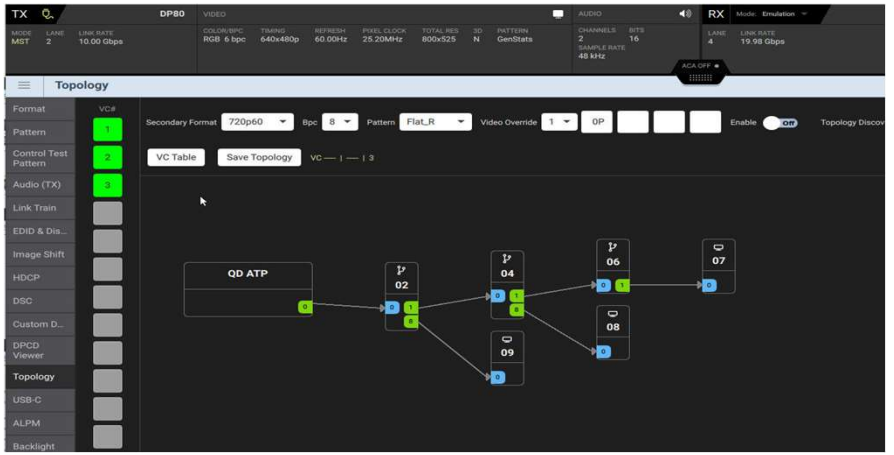
# CTS Updates – Composite Sink Device

- How to get port number value for CDF.
  - Connect Test Equipment to Composite Sink DUT in Setup 2.
  - See Test Equipment Generator topology:
  - The Composite Sink has 2 DFP Ports, 1 internal and 1 external.
  - Test Equip Sink connected by DFP Port 1
  - Sink 1 connected on Test Equip DFP Port 0
  - Sink 2 connected on Sink1 DFP Port 1.




# CTS 更新 – 複合水槽裝置

- 如何取得 CDF 的埠號值.
  - 在設置2中將測試設備連接到複合材料水槽的 DUT。
  - 參見測試設備產生器拓撲:
  - 複合水槽有兩個 DFP 埠，一個內部，一個外部。
  - 測試裝備匯流器由DFP埠1連接
  - Sink 1已連接於測試裝備 DFP 埠 0
  - Sink 2 連接在 Sink1 DFP 埠 1 上.

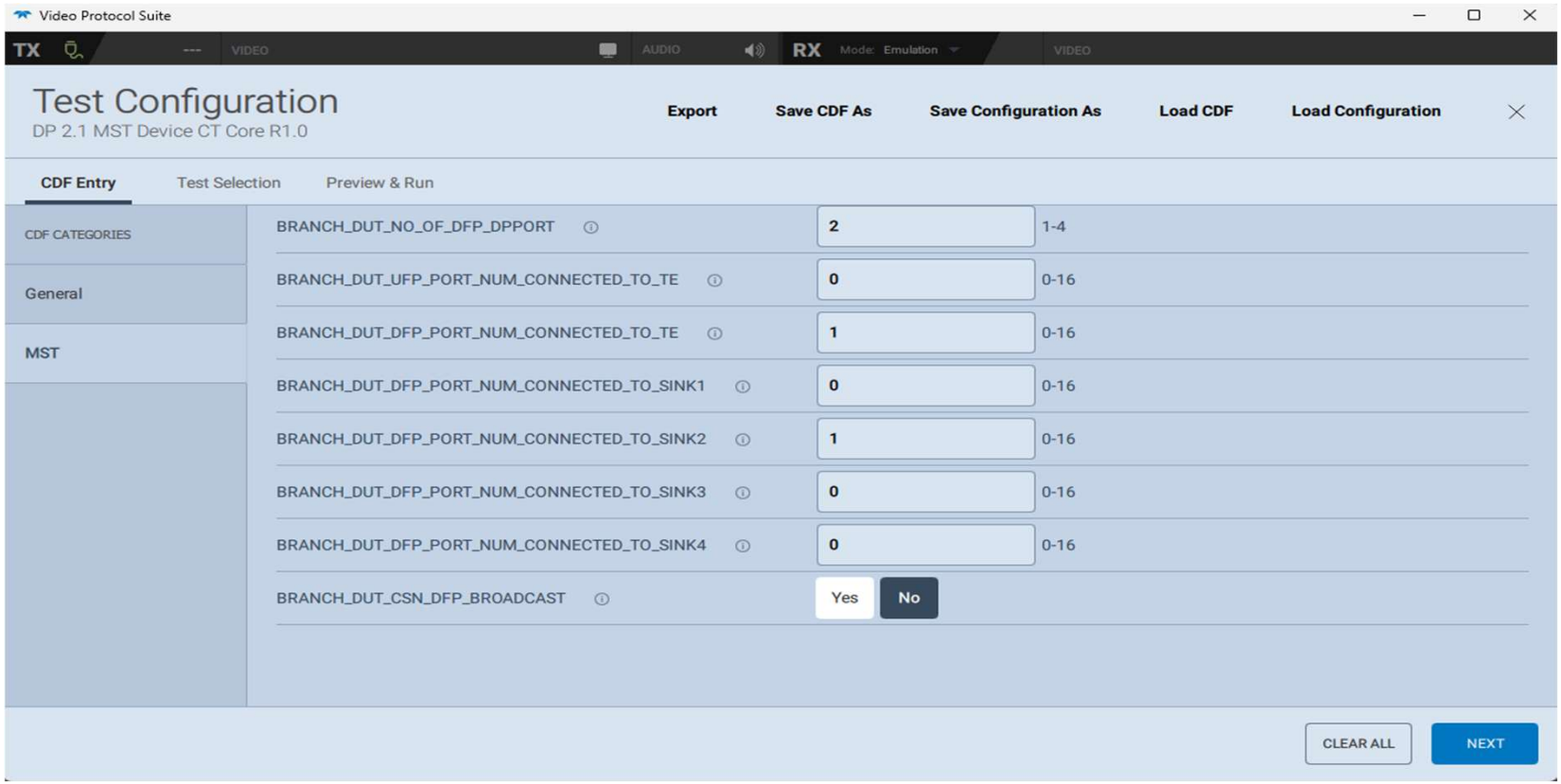


# CTS Updates – Composite Sink Device

## MST Composite Sink CTS CDF Sample for Setup 2:

# CTS 更新 – 複合水槽裝置

## MST 複合匯 CTS CDF 設置 2 範例：



# Recent New Test Additions

- New Source Tests
  - 4.3.1.25 : Successful link training when Sink is in BIOS mode with random LTTPR .
  - 4.4.1.7 : Verify Source DUT video transmission timing is within MAX_UNCOMPRESSED_PIXEL_RATE capability
  - 4.4.1.8 : Validation for VSC-SDP when transmitting YCbCr4:20 and ITU-R BT.2020 formats

# 近期新增測試項目

- 新源測試.
  - 4.3.1.25：當 Sink 進入 BIOS 模式並隨機 LTTPR 時，成功進行連結訓練。
  - 4.4.1.7 ：確認來源被測器視訊傳輸時間是否在 MAX_UNCOMPRESSED_PIXEL_RATE能力範圍內
  - 4.4.1.8 ：在傳輸 YCbCr4：20 及 ITU-R BT.2020 格式時，VSC-SDP 的驗證

# Recent New Test Additions

## New Sink Tests

- 5.7.1.7 EDID – Mandatory Blocks for HDR Displays
- 5.7.19.7 Native DisplayID – Mandatory Blocks for HDR Displays
- 5.7.20.4 Native DisplayID – Product Identification Data Block Product Name String ASCII Validation
- 5.7.20.5 EDID – Product Identification Data Block Revision (Byte 1)
- 5.7.20.6 EDID – Product Identification Data Block Number of Payload Bytes in Block (Byte 2)
- 5.7.20.7 EDID – Product Identification Data Block Week of Manufacture/Model Tag and Year of Manufacture/Model Year (Bytes 12 and 13)
- 5.7.20.8 EDID – Product Identification Data Block Product Name String ASCII Validation
- 5.7.21.6 Native DisplayID – Display Parameters Data Block Horizontal and Vertical Image Size Verification
- 5.7.21.7 EDID – Display Parameters Data Block Revision (Byte 1)
- 5.7.21.8 EDID – Display Parameters Data Block Number of Payload Bytes in Block (Byte 2)
- 5.7.21.9 EDID – Display Parameters Data Block Feature Support Flags Field (Byte 0Bh)
- 5.7.21.10 EDID – Display Parameters Data Block Native Luminance-related Fields (Bytes 18h to 1Dh)
- 5.7.21.11 EDID – Display Parameters Data Block Depth and Display Device Technology Fields (Byte 1Eh).

# 近期新增測試項目

## 新匯測試.

- 5.7.1.7 EDID – HDR 顯示的強制區塊
- 5.7.19.7 原生 DisplayID – HDR 顯示的強制區塊
- 5.7.20.4 原生 DisplayID – 產品識別資料區塊 產品名稱字串 ASCII 驗證
- 5.7.20.5 EDID – 產品識別資料區塊修訂版（位元組 1）
- 5.7.20.6 EDID – 產品識別資料區塊有效載荷位元組數（位元組2）
- 5.7.20.7 EDID – 產品識別資料區塊 製造週/型號標籤與製造年份/型號年（位元組 12 與 13）
- 5.7.20.8 EDID – 產品識別資料區塊 產品名稱字串 ASCII 驗證
- 5.7.21.6 原生 DisplayID – 顯示參數資料區塊水平與垂直影像大小驗證
- 5.7.21.7 EDID – 顯示參數資料區塊修訂（位元組 1）
- 5.7.21.8 EDID – 顯示參數 資料區塊 有效載荷位元組數（區塊2）
- 5.7.21.9 EDID – 顯示參數資料區塊功能支援旗標欄位（位元組 0Bh）
- 5.7.21.10 EDID – 顯示參數 資料區塊 原生亮度相關欄位（位元組 18h 至 1Dh）
- 5.7.21.11 EDID – 顯示參數、資料區塊深度與顯示裝置技術欄位（位元組 1Eh）。

# Recent New Test Additions

## New Sink Tests Continued…

- 5.7.21.12 – EDID – Display Parameters Data Block Horizontal and Vertical Image Size Verification
- 5.7.22.8 – EDID – Display Interface Features Data Block Revision (Byte 1)
- 5.7.22.9 – EDID – Display Interface Features Data Block Number of Payload Bytes in Block (Byte 2)
- 5.7.22.10 – EDID – Display Interface Features Data Block Supported Interface Color Depth-related Fields
- 5.7.22.11 – EDID – Display Interface Features Data Block Minimum Pixel Rate at Which YCbCr 4:2:0 Encoding Is Supported (Byte 7)
- 5.7.22.12 – EDID – Display Interface Features Data Block Supported Interface Audio Capability and Feature Flags (Byte 8)
- 5.7.22.13 – EDID – Display Interface Features Data Block Supported Interface Color Space and EOTF-related Fields
- 5.7.22.14 – EDID – Display Interface Features Data Block Additional Supported Interface Color Space and EOTF-related Fields (Bytes 0Bh to 12h)
- 5.4.1.9 : Verify Sink DUT displays the video timing based on MAX_UNCOMPRESSED_PIXEL_RATE capability
- 5.6.3.8: Verify Sink DUT correctly reconstructs image when HActive % Slice_Count != 0.

# 近期新增測試項目

## 新一輪沉沒測試持續進行…

- 5.7.21.12 – EDID – 顯示參數資料區塊水平與垂直影像大小驗證
- 5.7.22.8 – EDID – 顯示介面功能資料區塊修訂版(位元組 1)
- 5.7.22.9 – EDID – 顯示介面功能資料區塊, 有效載荷位元組數(位元組 2)
- 5.7.22.10 – EDID – 顯示介面功能 資料區塊支援介面 顏色深度相關欄位
- 5.7.22.11 – EDID – 顯示介面功能 支援 YCbCr 4:2:0 編碼的最小像素率資料區塊(位元組 7)
- 5.7.22.12 – EDID – 顯示介面特性、資料區塊、支援介面、音訊能力與功能標誌(位元組 8)
- 5.7.22.13 – EDID – 顯示介面功能、資料區塊支援介面、色彩空間及 EOTF 相關欄位
- 5.7.22.14 – EDID – 顯示介面功能、資料區塊、額外支援介面、色彩空間及 EOTF 相關欄位(位元組 0Bh 至 12h)
- 5.4.1.9 :驗證匯入被測器顯示視訊時序, 依據 MAX_UNCOMPRESSED_PIXEL_RATE能力
- 5.6.3.8:當 HActive % Slice_Count ！= 0 時, 驗證匯 DUT 正確重建影像。

# Summary

- **Key Takeaways**
  - CTS coverage significantly expanded since Rev 1.1
  - New Source, Branch, and Composite Sink validations added
  - Test Equipment software supports automated CDF population via VESA JSON file
  - Simplified CTS execution workflow
  - New tests improve EDID, NDID, HDR and MST interoperability coverage

# 摘要

- **重點摘要.**
  - 自 Rev 1.1 以來，CTS 的覆蓋範圍大幅擴展
  - 新增了原始碼、分支與複合匯驗證功能
  - 測試設備軟體支援透過 VESA JSON 檔案自動建立 CDF
  - 簡化的 CTS 執行工作流程
  - 新測試提升了EDID、NDID、HDR及MST互通性覆蓋範圍

# 問答與回饋

**Alok Soni/Neal Kendall – 謝謝你**

Teledyne LeCroy

*2026年10月16日 – 台北，台灣*

# VESA DisplayPort汽车扩展（DP AE）测试您的功能安全实现

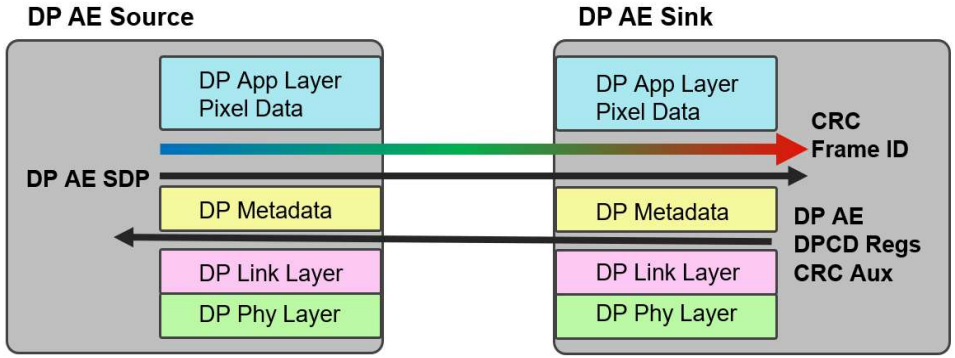
**Neal Kendall/Alok Soni**
Teledyne LeCroy
*2026年10月16日 - 台北，台灣*

# DisplayPort 汽車擴展——介紹

## VESA DisplayPort 汽車擴展版與 DisplayPort 有什麼不同？

- 傳統DisplayPort側重於鏈路可靠性：
  - 連結訓練、連結對齊、時鐘恢復。
  - 前向糾錯(FEC)。
  - 顯示流壓縮(DSC)。
  - 傳輸視頻和音頻。
  - 多流傳輸(MST)。
- DisplayPort 不驗證以下內容：
  - 整個圖像流程都是正確的。
  - 生成了正確的圖像。
  - 沒有任何幀丟失。
  - 這些照片準時送達。
  - 注意：DisplayPort 汽車擴展拓撲假設為靜態；發現、初始化和配置得到簡化。

- DisplayPort的汽車擴展插件：
  - AE使用DisplayPort 2.1a和/或eDP 2.0規範。
  - DP AE引入了新的DP AE DPCD 暫存器，用於能力、狀態和配置。
  - DP AE對視頻和數據使用CRC檢查。
  - DP AE檢查接收到的DisplayPort流的幀序列和幀時序。
  - DP AE增加了一個次級資料包(DP AE SDP)。



# DisplayPort 汽車擴充——設定檔

## 功能安全與保安配置文件

**功能安全要素——配置文件1和2**

| | |
|---|---|
| 未压缩像素上的CRC | 压缩像素上的CRC |
| 重建后的DSC像素上的CRC | CRC在次级数据包（SDP）上 |
| CRC关注区域 | CRC关于主流属性（MSA） |
| 帧丢弃、重复和超时监控 | 状态报告 |

- 汽車延伸功能.
  - 功能安全（配置檔1和2）——防止意外故障。
  - 安全性（設定檔3和4）——防止惡意入侵和修改。

**安全要素——配置文件3和4**

| | |
|---|---|
| MAC映射在未壓縮像素/壓縮位元組和MSA | DP AE二級資料包（SDP）上的MAC |
| 數據平面安全（輔助通道認證） | AE次級資料包（SDP）的全面完整性安全 |

# DisplayPort 汽車擴展——功能安全

## 將DisplayPort從視頻傳輸介面擴展為汽車顯示器的端到端監控系統

### 為什麼選擇DP AE功能安全？

汽車顯示屏越來越多地呈現安全關鍵信息.

- 傳統DisplayPort驗證鏈路傳輸，但不驗證端到端圖像正確性.
- DisplayPort AE增加了監控機制:
  - 形象完整性。
  - 框架連貫性。
  - 時機準確性。
  - 渲染正確性.
- DisplayPort AE實現了快速故障檢測和系統級安全響應.
- DisplayPort AE可擴展，從儀表板到多顯示器駕駛艙架構.

DisplayPort**汽車擴展功能安全**



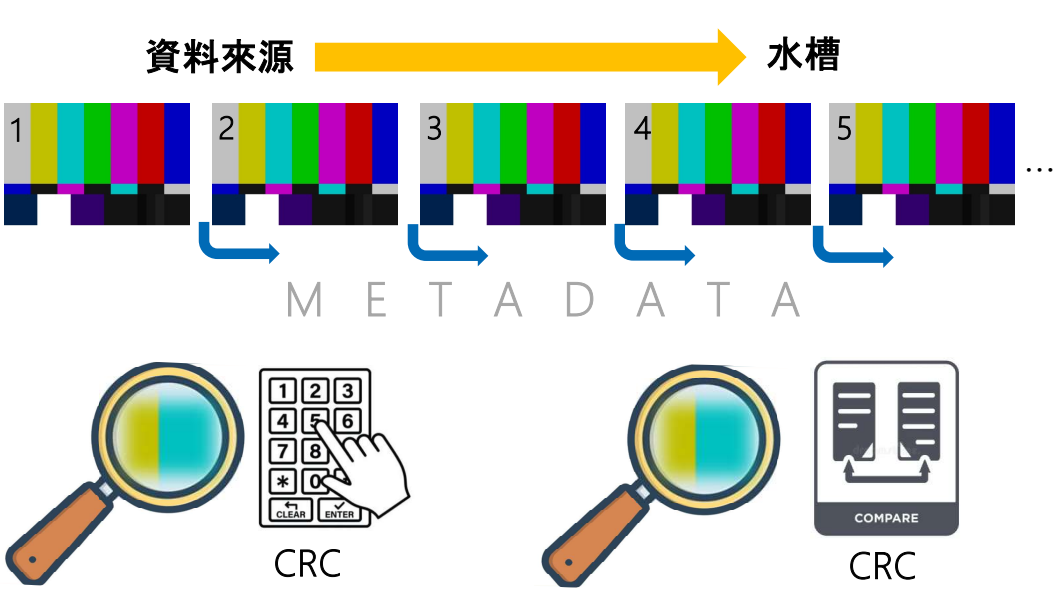
# DisplayPort AE – 功能安全 – 圖像完整性

## 圖像完整性監測——圖像數據是否正確到達？

目標：驗證顯示的圖像是否與源生成的圖像一致.

- 機制:
  - CRC PIXELS(未壓縮或壓縮的”重建像素“).

    **註:壓縮技術使SerDes成本更低，降低電纜複雜度和重量，降低功耗.**
  - CRC 壓縮位元組.
  - CRC主流屬性(MSA).
  - CRC二級數據包(SDP)).
  - CRC汽車推廣SDP.
  - CRC輔助信道消息.
  - CRC興趣區域(ROI).
- 探測:
  - 像素損壞(壓縮/未壓縮)。
  - 鏈路傳輸與元資料錯誤.



# VESA DisplayPort AE – 功能安全 - 關注領域

## 帶有關注區域(ROI)的幀視頻關鍵監控

目標：指定顯示中哪些區域最為關鍵.

- 目的:
  - 將功能安全監控重點放在顯示中安全關鍵區域。
  - 能夠針對最重要的視覺資訊進行有針對性保護.
- 關注區域（ROI）能力:
  - 針對每個投資回報率(ROI)計算的CRC。
  - 每個顯示屏最高可獲得16的投資回報率。
  - ROI可以動態啟用、禁用或重新配置。
  - 投資回報率可能在展示中重疊。
  - 初始化時，ROI 座標通過輔助通道傳輸到 sack.



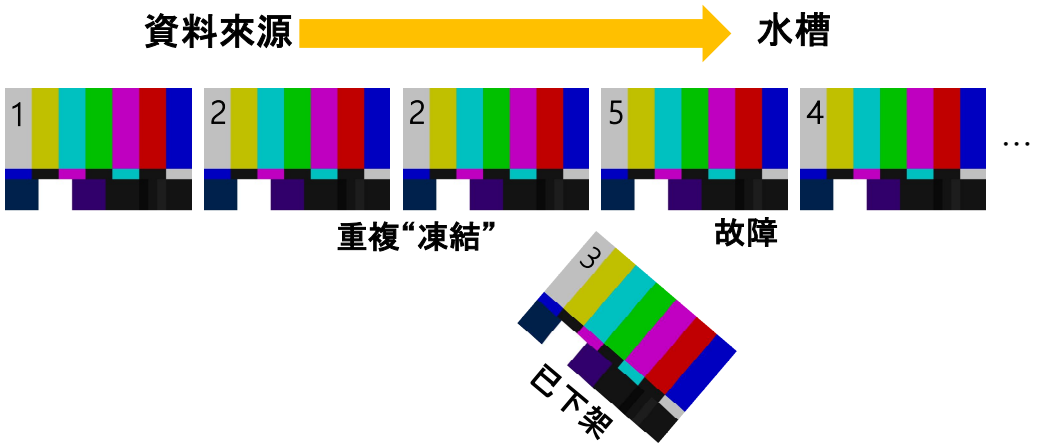



# VESA DisplayPort AE – 功能安全 – 幀連續性

## 幀連續性監測檢查，我們收到了每一幀嗎？

目標：確認所有視頻幀的到達順序正確.

- 機制:
  - FRAME ID計數器，每幀遞增.
- 探測:
  - 幀數缺失(掉落)。
  - 重複幀。
  - 亂序幀.

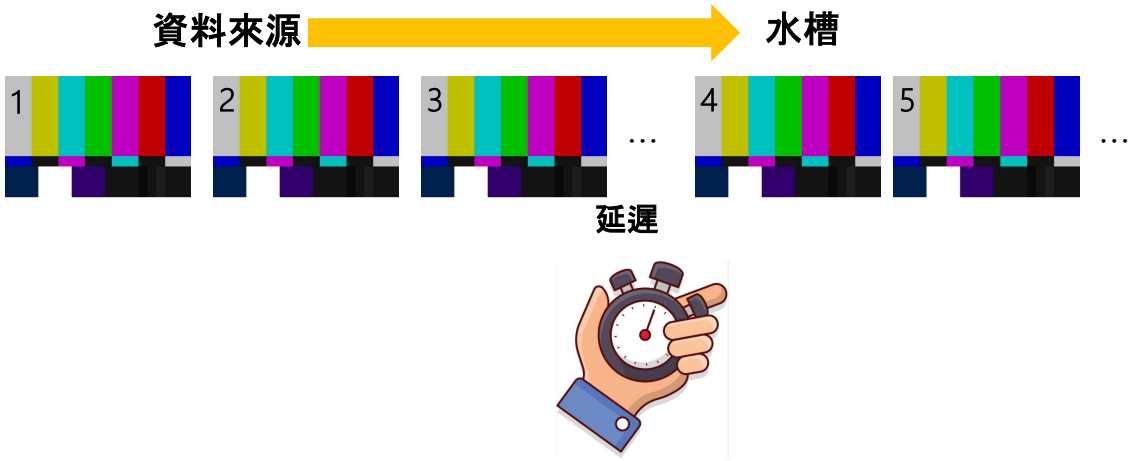


# VESA DisplayPort AE – 功能安全 – 時序正確性

## 時間準確性檢查，視頻幀和元數據是否按時到達？

目標：確認資訊按預期到達.

- 機制:
  - 超時監控。
  - 幀ID進程
  - AE SDP 中繼資料監控.
- 探測:
  - 延迟帧数。
  - 管道停滞。
  - 过度延迟.



# VESA DisplayPort AE – 功能安全 – 故障檢測/隔離

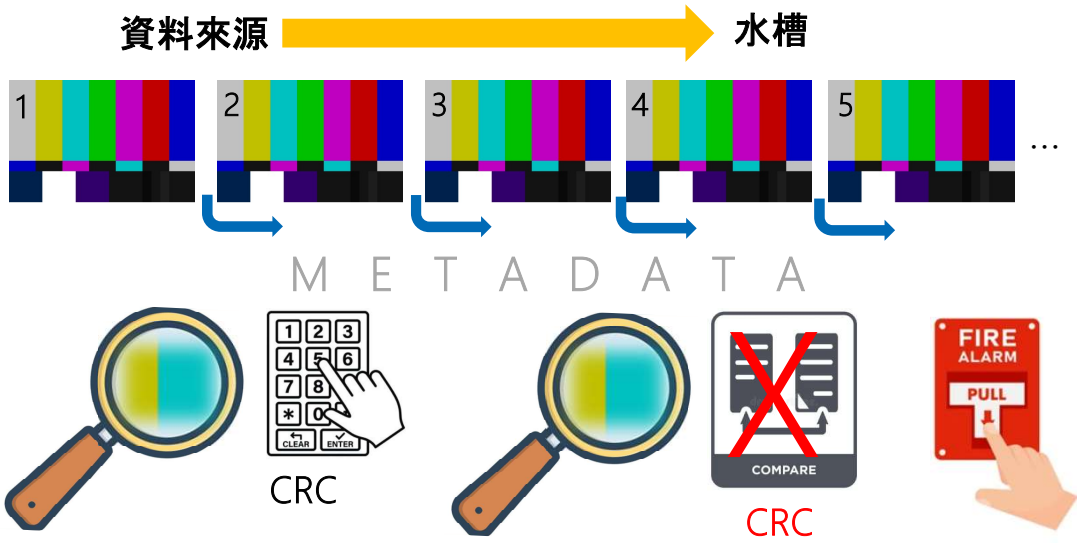
## 快速故障檢測與升級——使車輛能夠適當回應

目標：檢測到錯誤時提醒司機和系統.

- 軟錯誤:
  - CRC不匹配。
  - 幀數不匹配。
  - 暫停事件。
- 硬錯誤:
  - 持續性故障.
  - 錯誤閾值已超過.

**注意:投資回報率(ROI)有自己的CRC.**

- 故障檢測啟用:
  - 司機警報。
  - 故障保護操作。
  - 系統冗餘激活與診斷日誌.

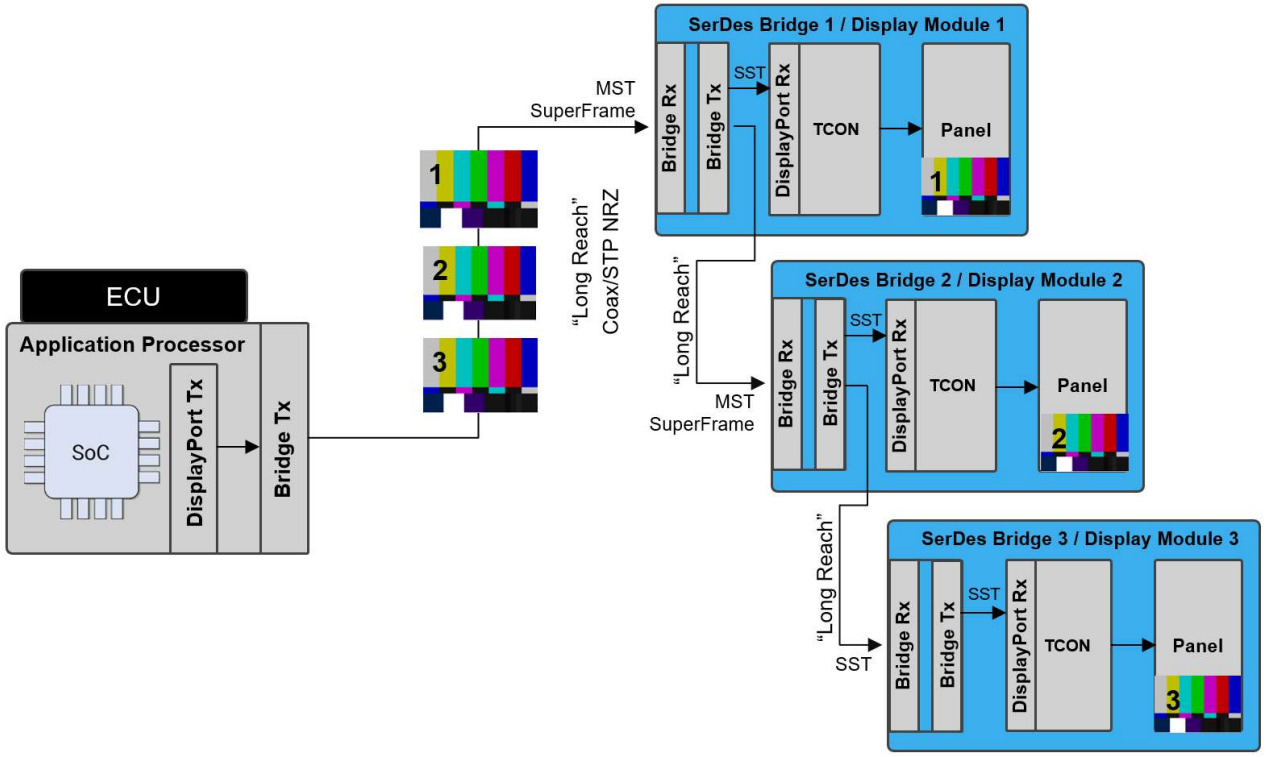


# VESA DisplayPort AE – 拓扑与架构

## DisplayPort 汽車擴展拓撲

DP AE 測試初始化.

- 多流傳輸（MST）——在單一實體通道上傳輸多個虛擬通道，用於多個顯示。
- MST運行在「長距離」傳輸媒介上，如OpenGMSL、FPD Link、A-Phy。

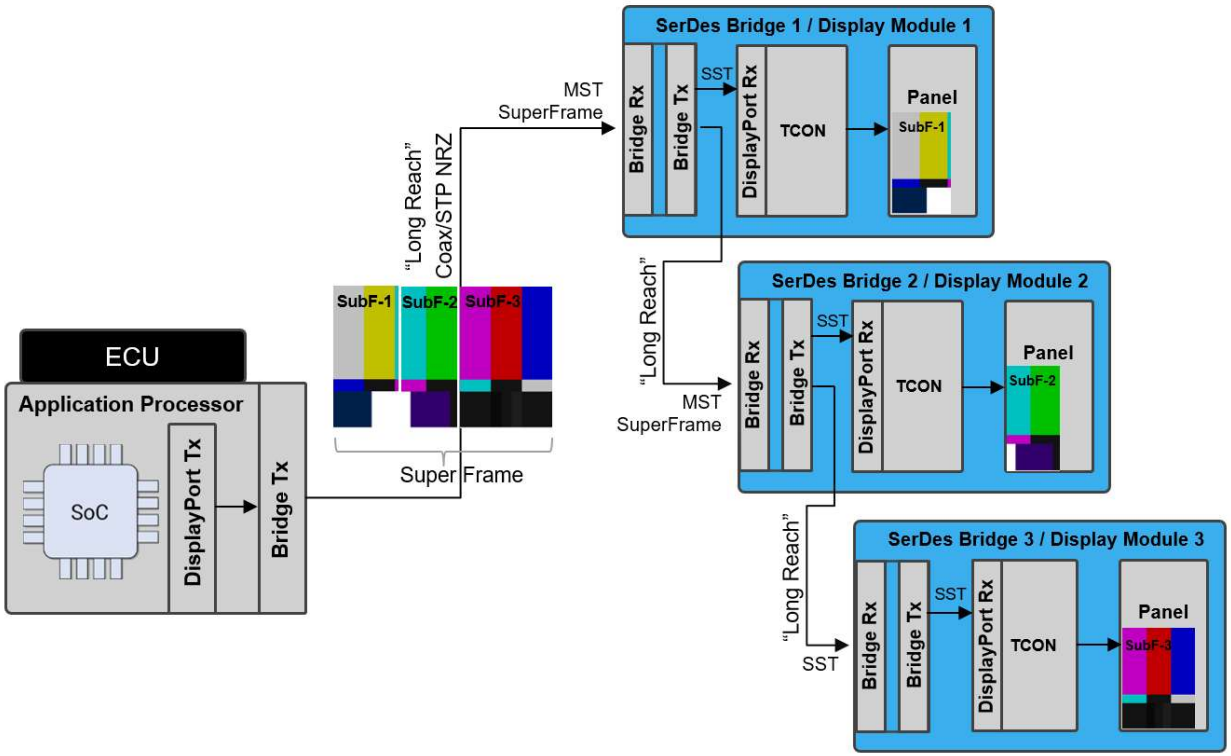


# DisplayPort AE – 拓扑与架构

## DisplayPort 汽車擴展拓撲

DP AE 測試初始化.

- 超幀和子幀——單幀視頻幀擴展至多顯示器。
- 超幀運行於「長距離」傳輸媒介，如OpenGMSL、FPD Link、A-Phy。



VESA

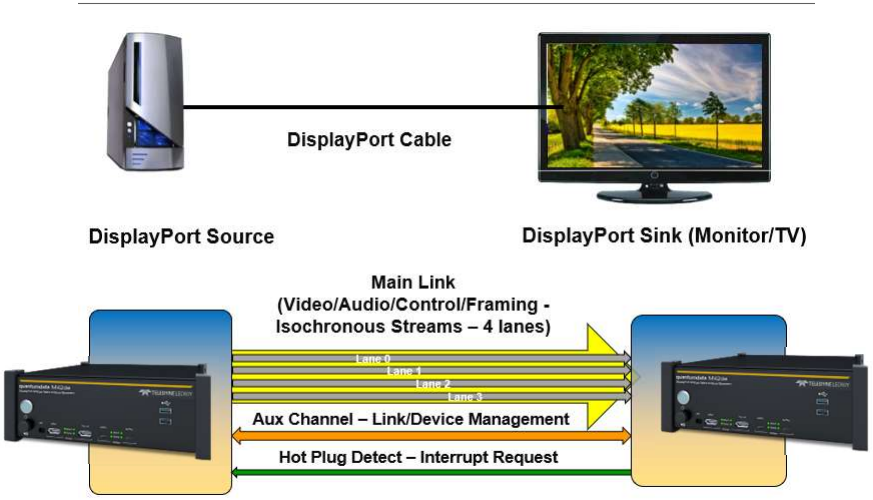
# 测试您的DisplayPort汽车扩展功能安全实现

# VESA DisplayPort AE——功能安全測試

## 如何測試您的DisplayPort汽車擴充實現

DP AE 源/匯測試.

- 設備仿真:
  - 模擬DP AE源以測試顯示和拓撲結構.
  - 模擬DP AE顯示器以測試源並展示拓撲結構.
- 視頻生成配置:
  - 配置MST或SuperFrame的拓撲.
  - 配置興趣區域(ROI).
- 視頻與協議分析:
  - 即時接收流的視圖。
  - 視頻和元數據的捕捉、後期分析。
  - 合規測試以支援 VESA DisplayPort 汽車標誌項目.







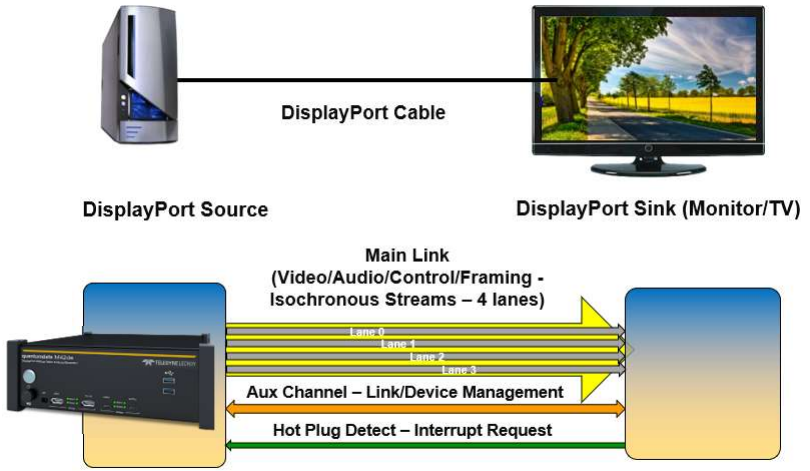
**M42DE 80G 視訊分析儀/發生器**

# VESA DisplayPort AE——功能安全测試

## 如何测試您的DisplayPort汽車擴充實現

設定DP AE視訊產生器.

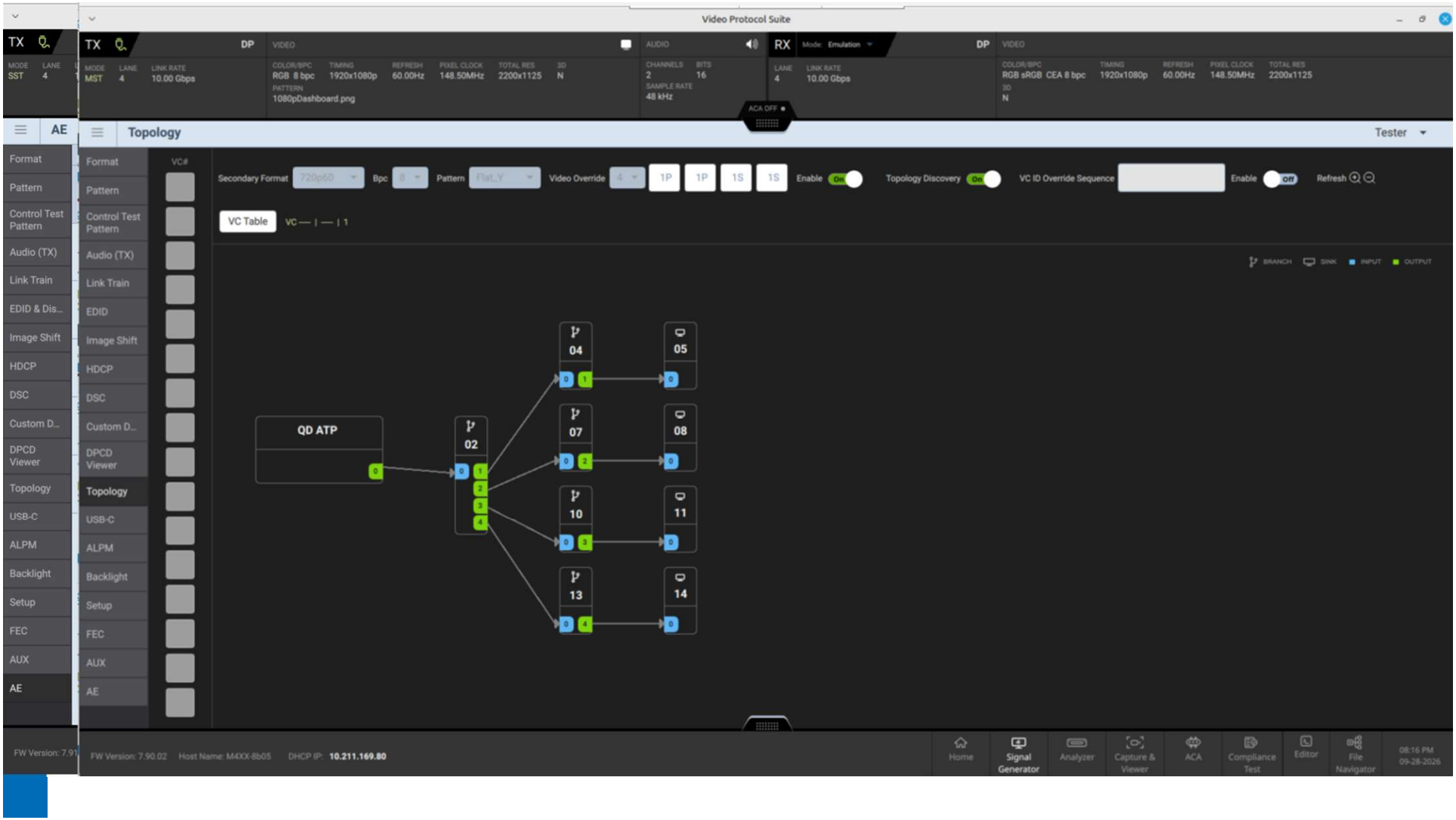
- **配置拓扑、流数、配置文件和投资回报率.**
- 次要分支的选择.
- 配置关注区域.
- 错误阈值配置.
- 查看汇 DPCD DP AE 寄存器.
- 注入错误.
- 查看汽车延伸现状.







**M42DE 80G 视频分析仪/发生器**

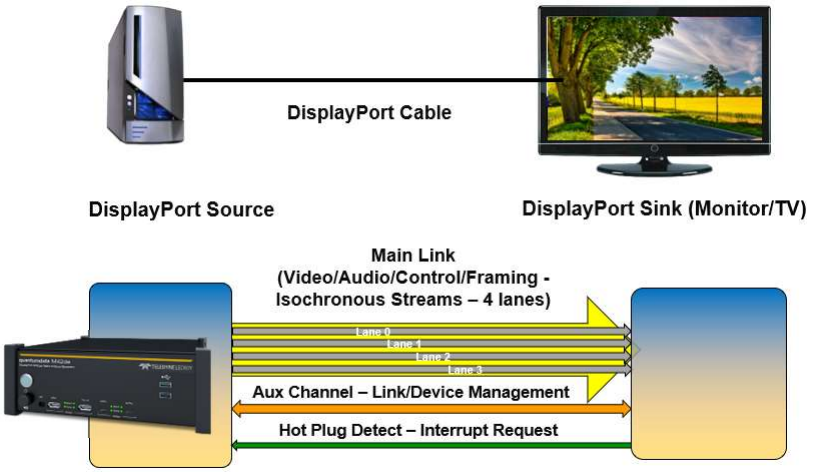

Video Protocol Suite
TX
DP
MODE MST
LANE 4
LINK RATE 10.00 Gbps
VIDEO
COLOR/BPC RGB 8 bpc
TIMING 1920x1080p
REFRESH 60.00Hz
PIXEL CLOCK 148.50MHz
TOTAL RES 2200x1125
3D N
PATTERN 1080pDashboard.png
AUDIO
CHANNELS 2
BITS 16
SAMPLE RATE 48 kHz
RX
Mode: Emulation
DP
LANE 4
LINK RATE 10.00 Gbps
VIDEO
COLOR/BPC RGB sRGB CEA 8 bpc
TIMING 1920x1080p
REFRESH 60.00Hz
PIXEL CLOCK 148.50MHz
TOTAL RES 2200x1125
3D N
ACA OFF
AE
Topology
Tester
Format
Pattern
Control Test Pattern
Audio (TX)
Link Train
EDID
Image Shift
HDCP
DSC
Custom D...
DPCD Viewer
Topology
USB-C
ALPM
Backlight
Setup
FEC
AUX
AE
VC#
Secondary Format
720p60
Bpc
8
Pattern
Flat_Y
Video Override
4
1P
1P
1S
1S
Enable
On
Topology Discovery
On
VC ID Override Sequence
Enable
Off
Refresh
VC Table
VC — | — | 1
BRANCH
SINK
INPUT
OUTPUT
QD ATP
02
04
05
07
08
10
11
13
14
FW Version: 7.91
FW Version: 7.90.02
Host Name: M4XX-8b05
DHCP IP: 10.211.169.80
Home
Signal Generator
Analyzer
Capture & Viewer
ACA
Compliance Test
Editor
File Navigator
08:16 PM
09-28-2026

# VESA DisplayPort AE——功能安全測試

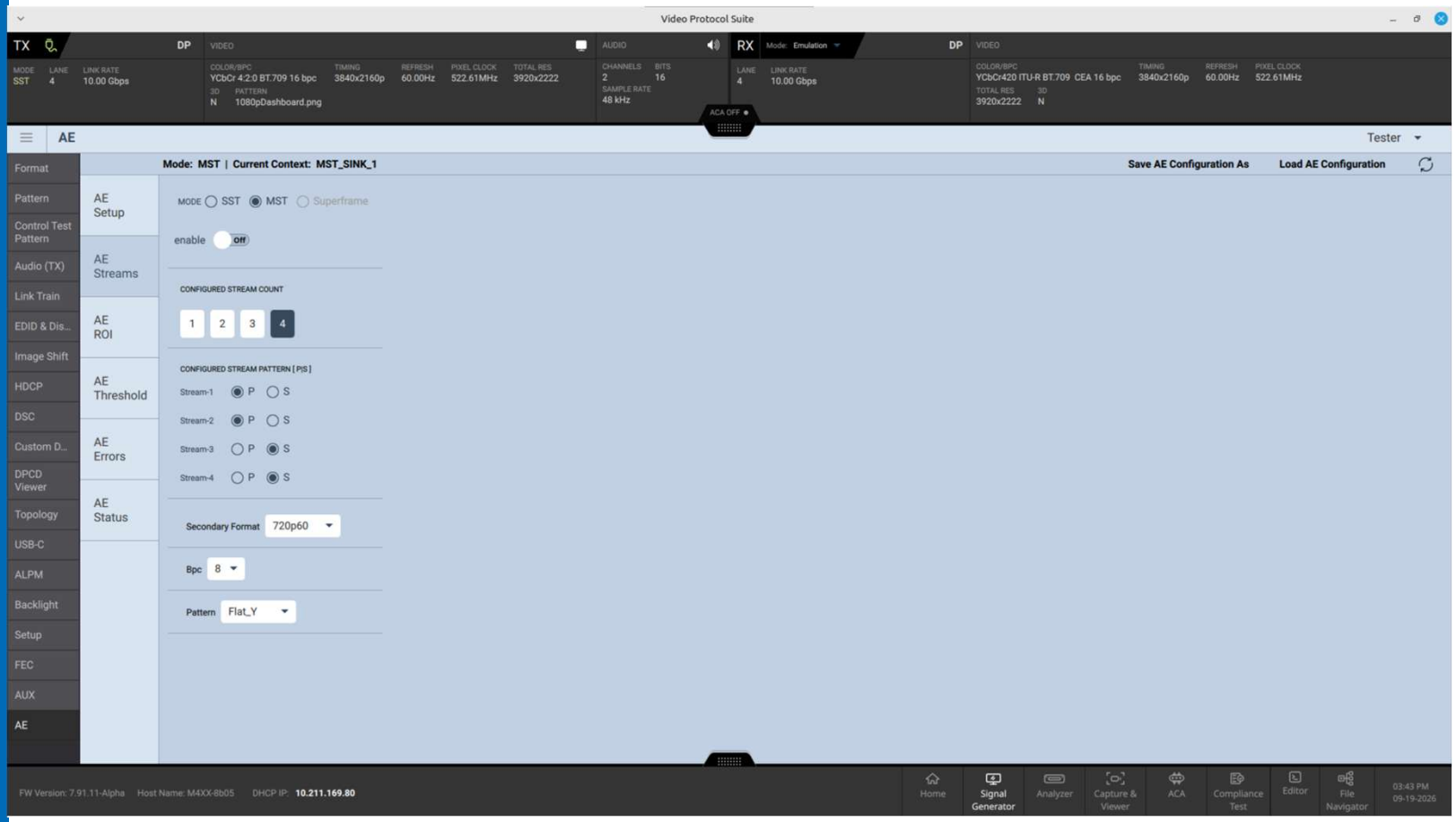
## 如何測試您的DisplayPort汽車擴充實現

設定DP AE視訊產生器.

- 配置拓撲、流數、配置文件和投資回報率。
- 選擇次要課程。
- 配置感興趣區域。
- 配置錯誤閾值。
- 查看Sink DPCD DP AE暫存器。
- 注入錯誤。
- 查看汽車延伸現狀.



# VESA DisplayPort AE – Testing Functional Safety

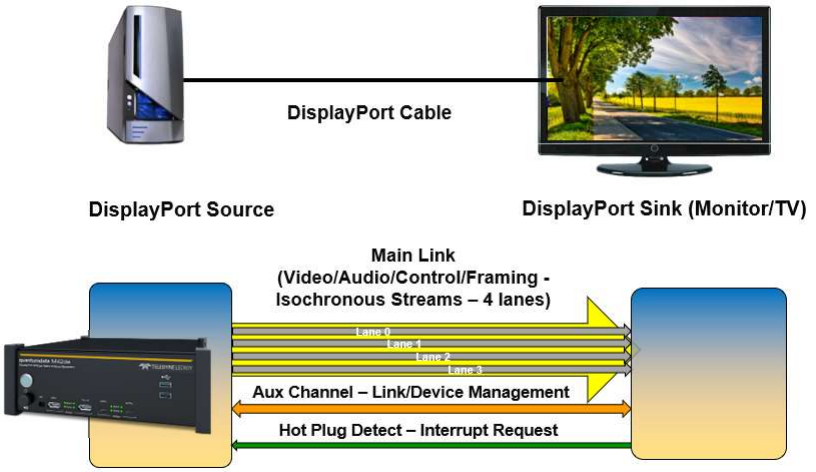


# VESA DisplayPort AE——功能安全測試

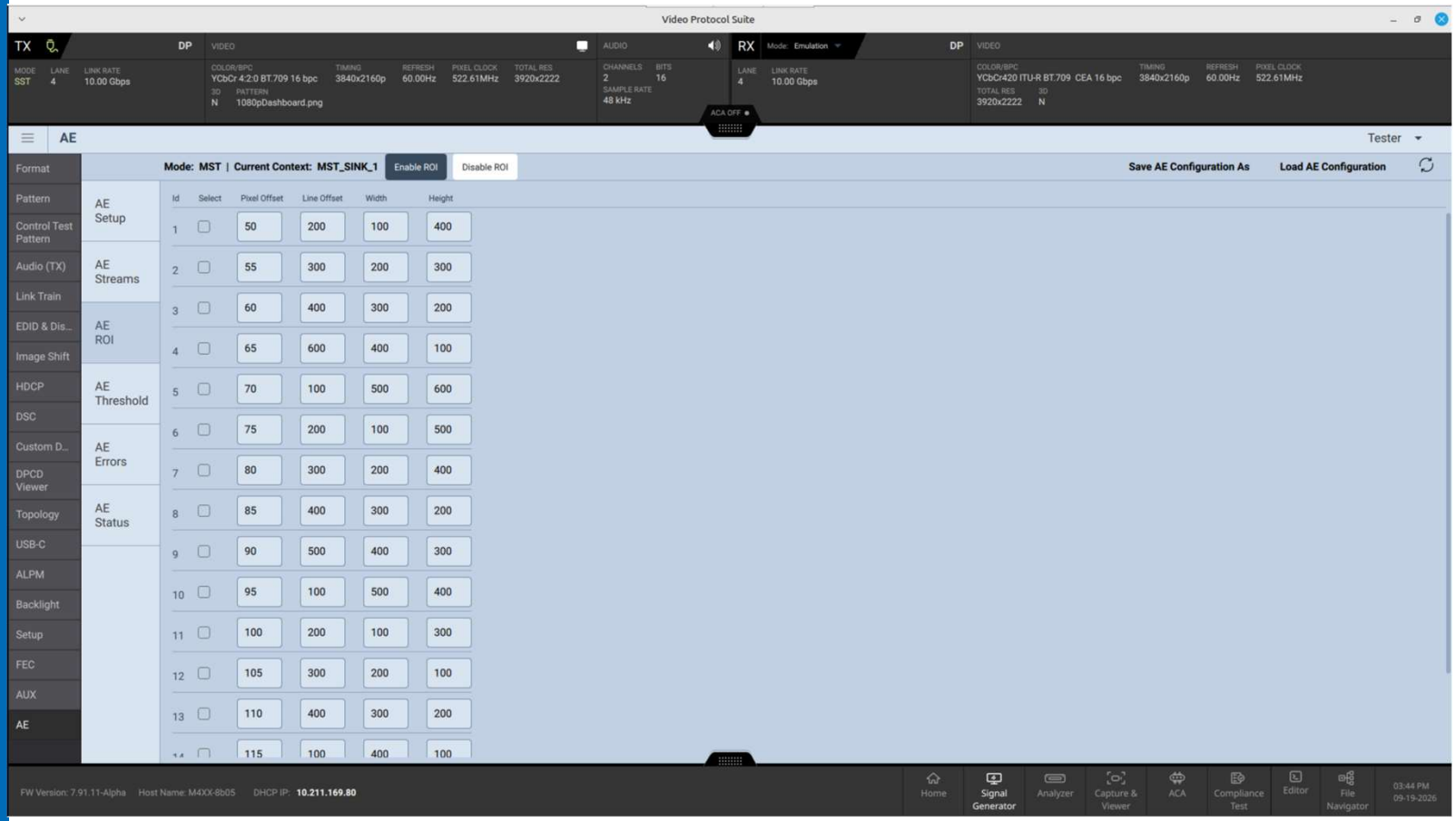
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# VESA DisplayPort AE – Testing Functional Safety

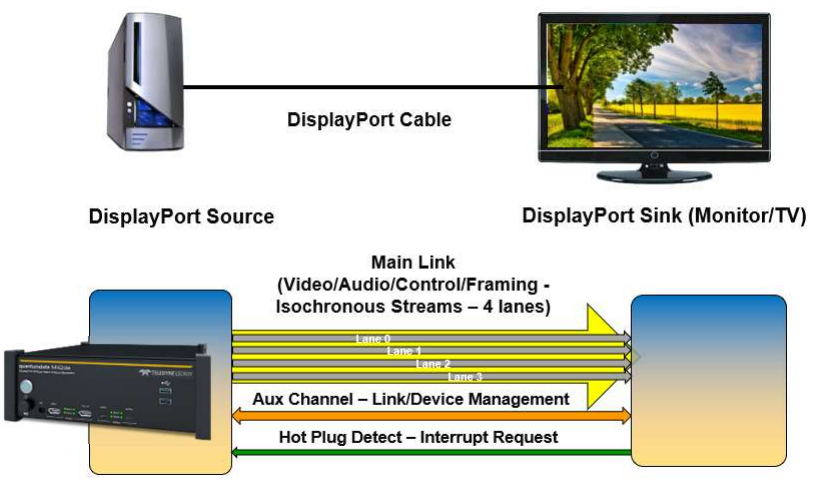


# VESA DisplayPort AE——功能安全測試

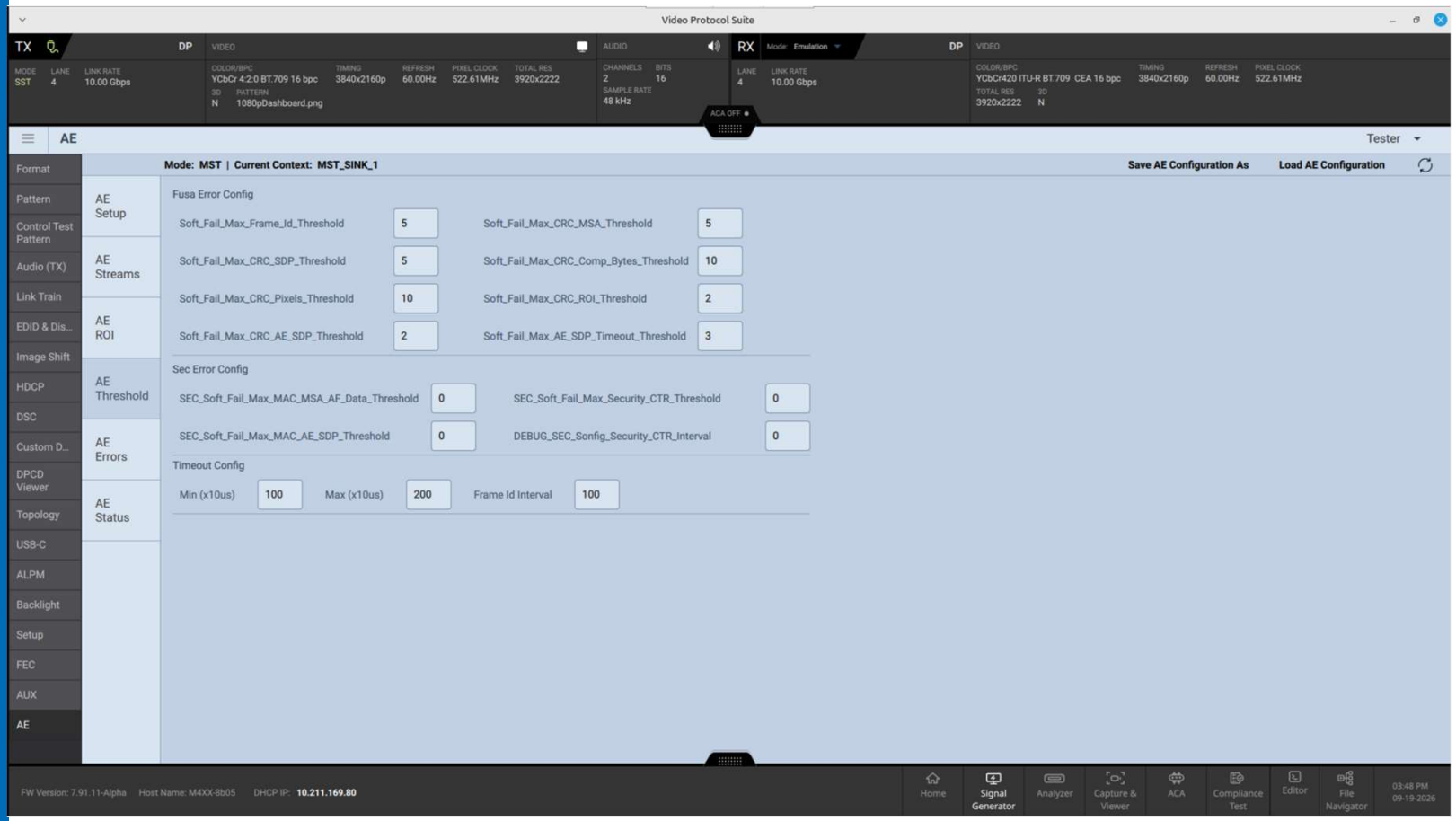
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- 配置錯誤閾值。
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# VESA DisplayPort AE – Testing Functional Safety

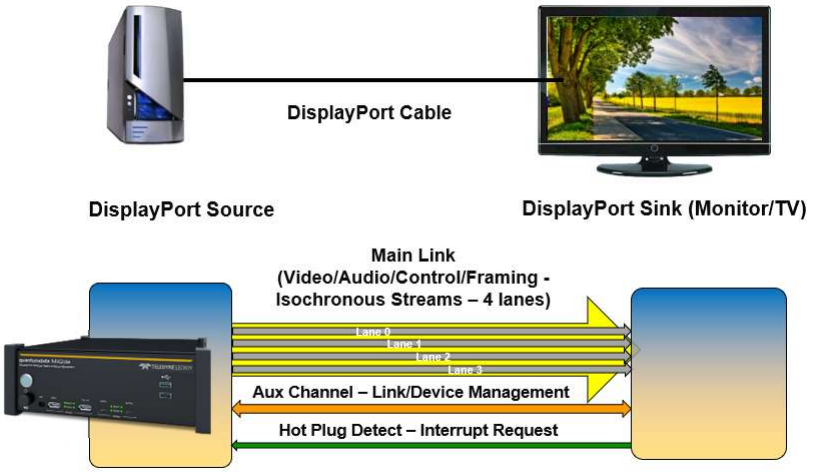


# VESA DisplayPort AE——功能安全測試

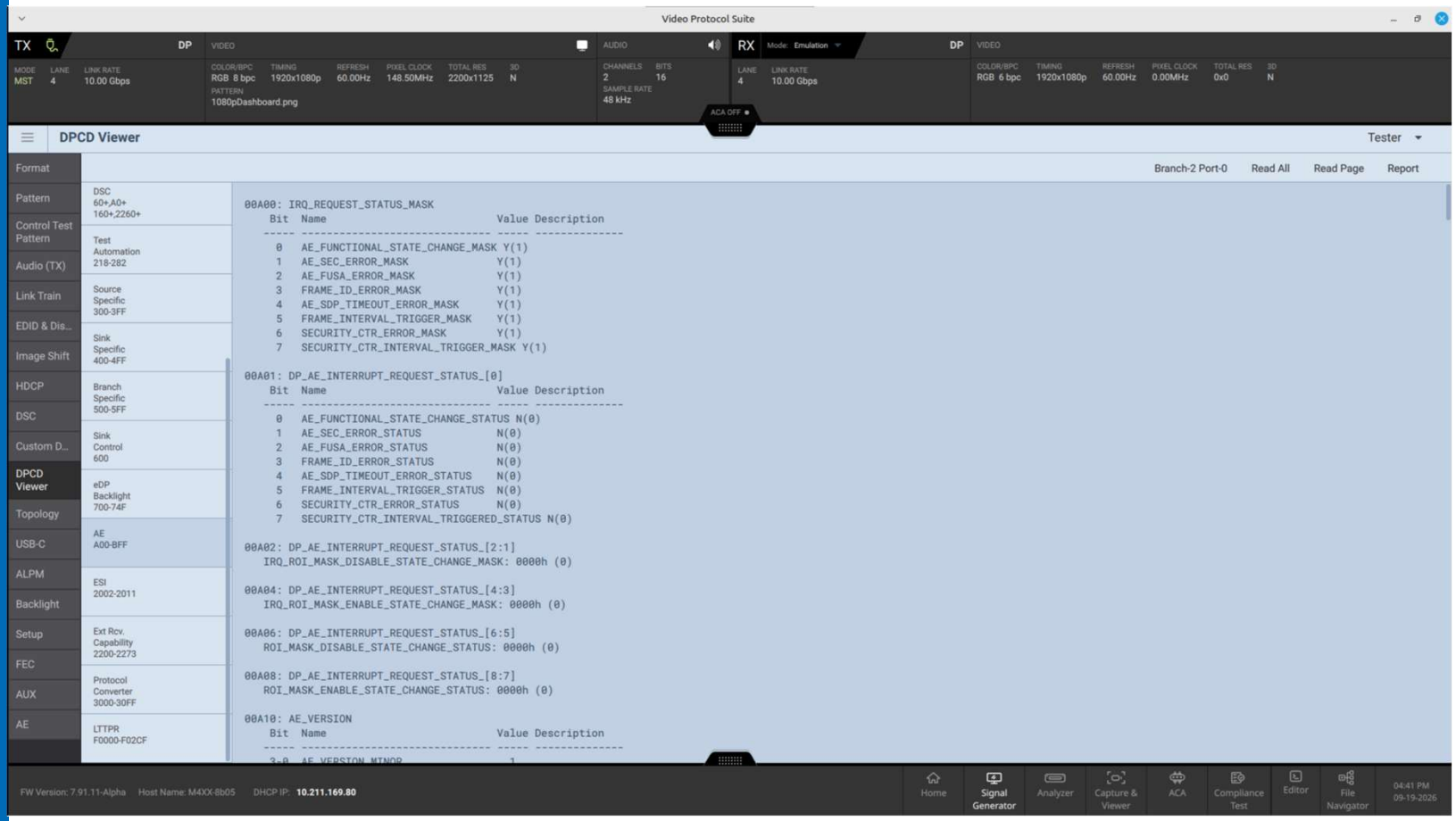
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- 選擇次要課程。
- 配置感興趣區域。
- 配置錯誤閾值 。
- **查看Sink DPCD DP AE暫存器。**
- 注入錯誤。
- 查看汽車延伸現狀.



# VESA DisplayPort AE – Testing Functional Safety

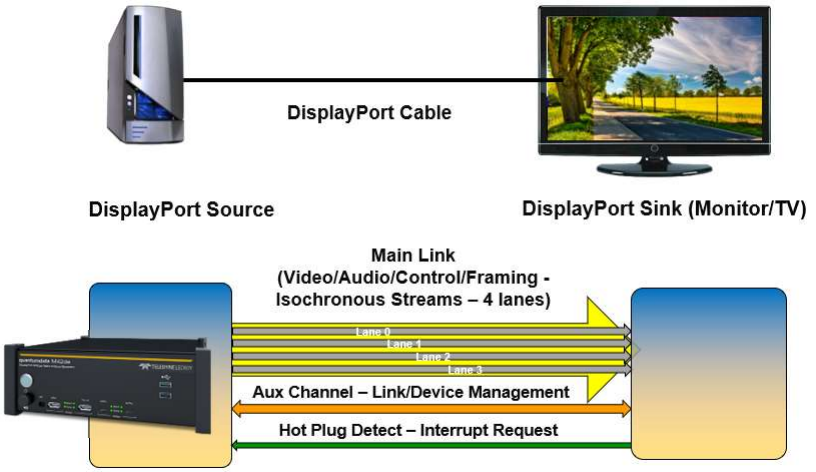


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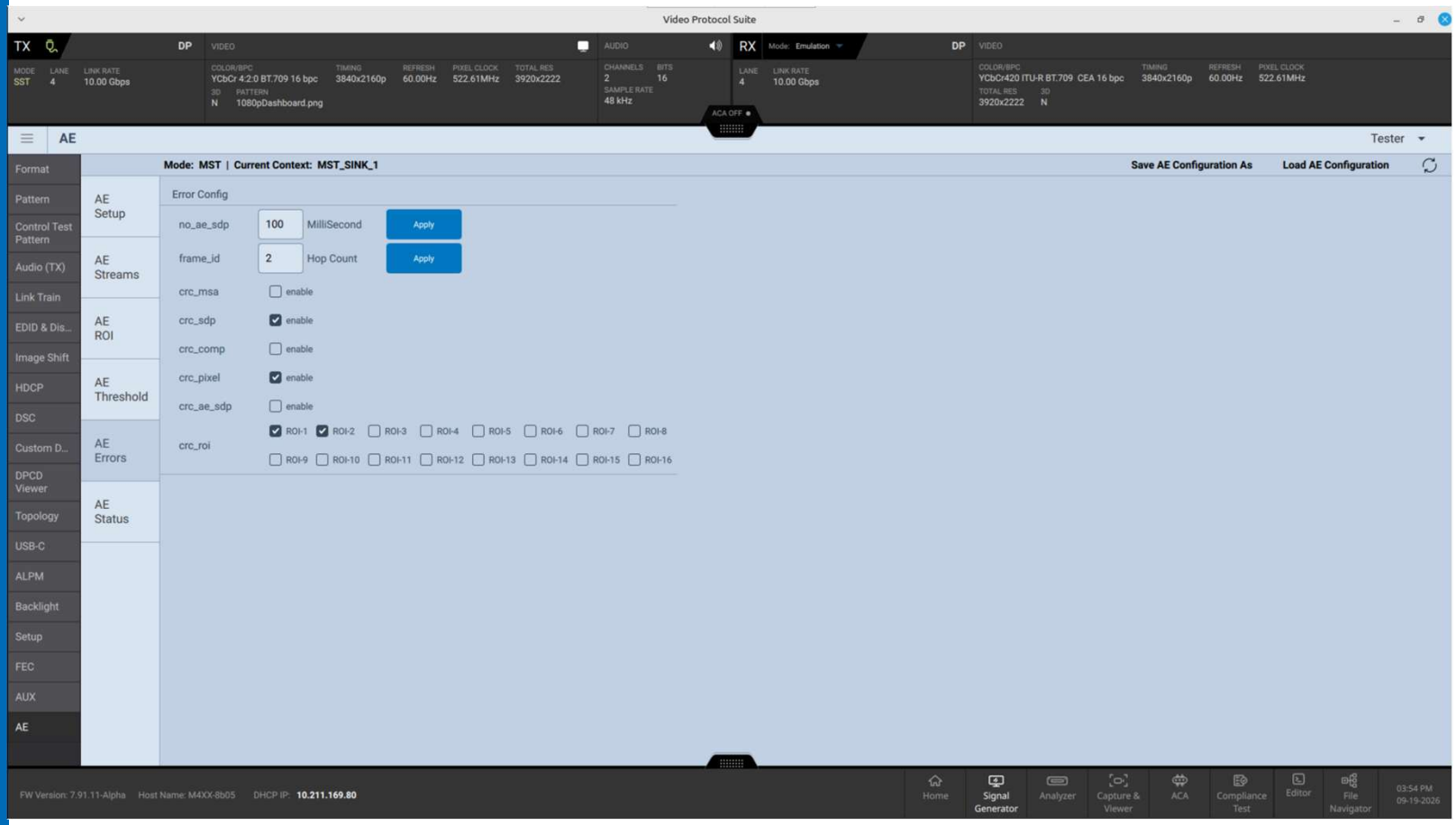
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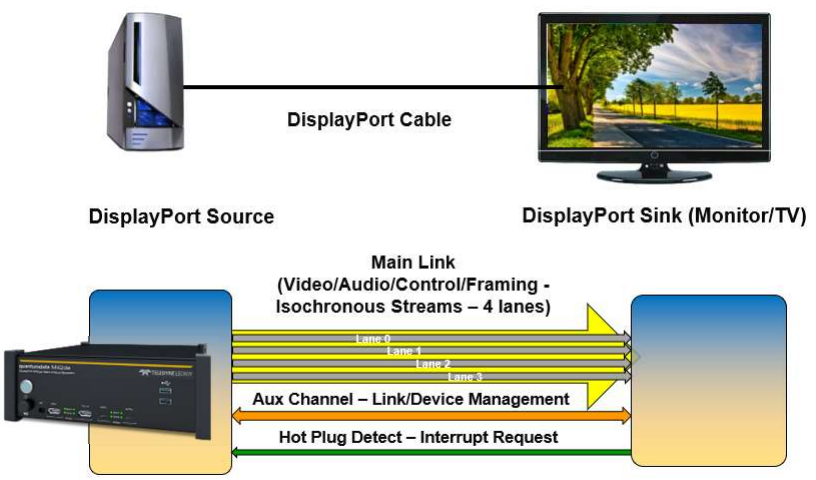


# VESA DisplayPort AE——功能安全測試

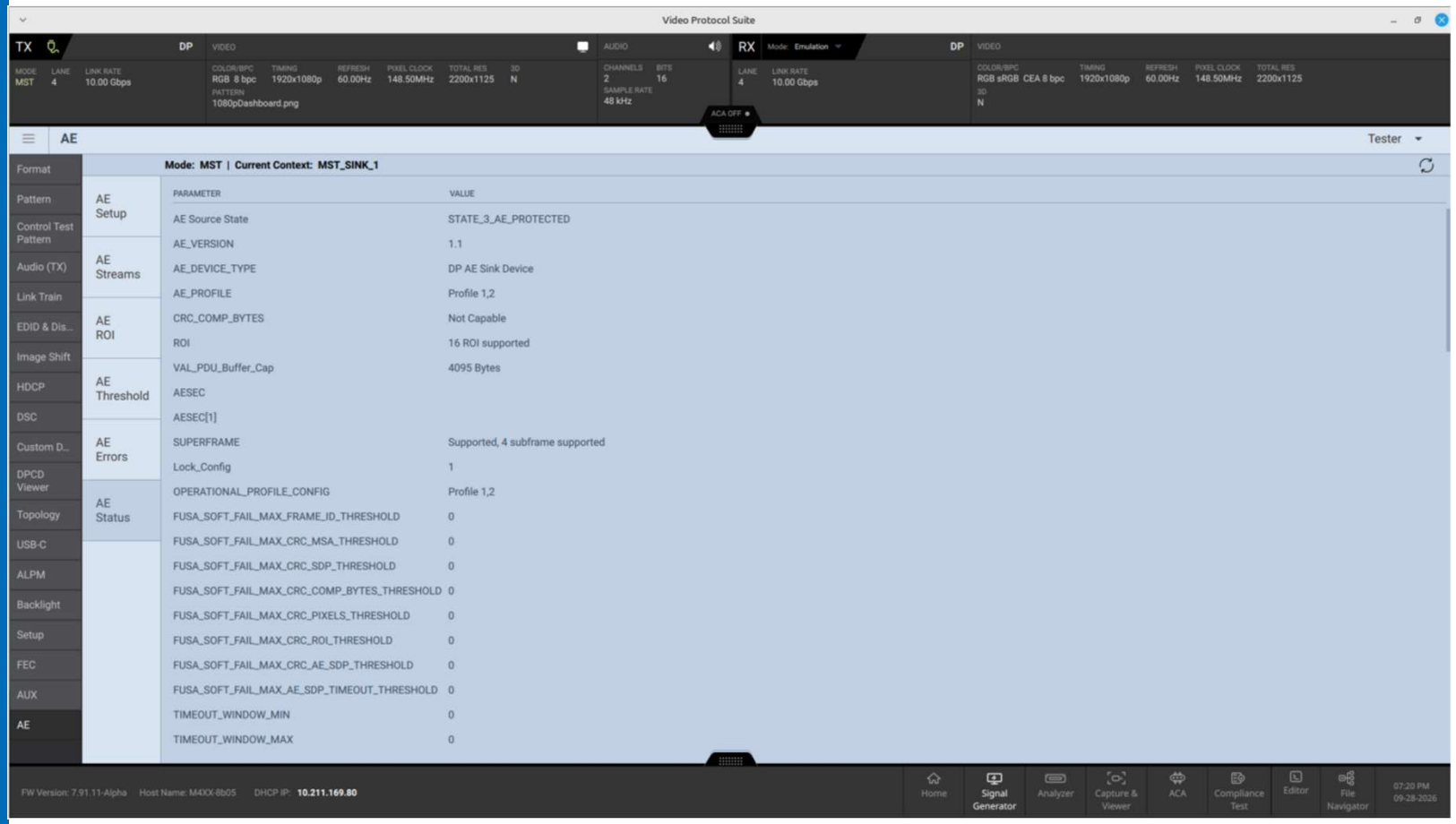
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# VESA DisplayPort AE – Testing Functional Safety



# VESA DisplayPort AE——功能安全測試

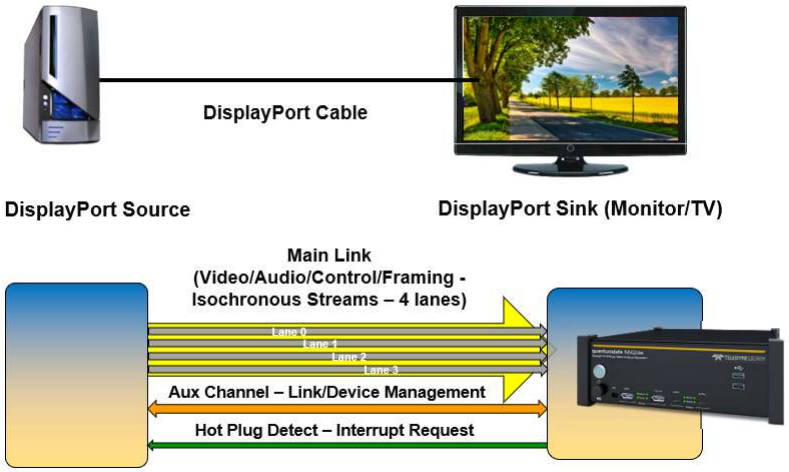
## 如何測試您的DisplayPort汽車擴充實現

設定DP AE視訊/協定分析儀.

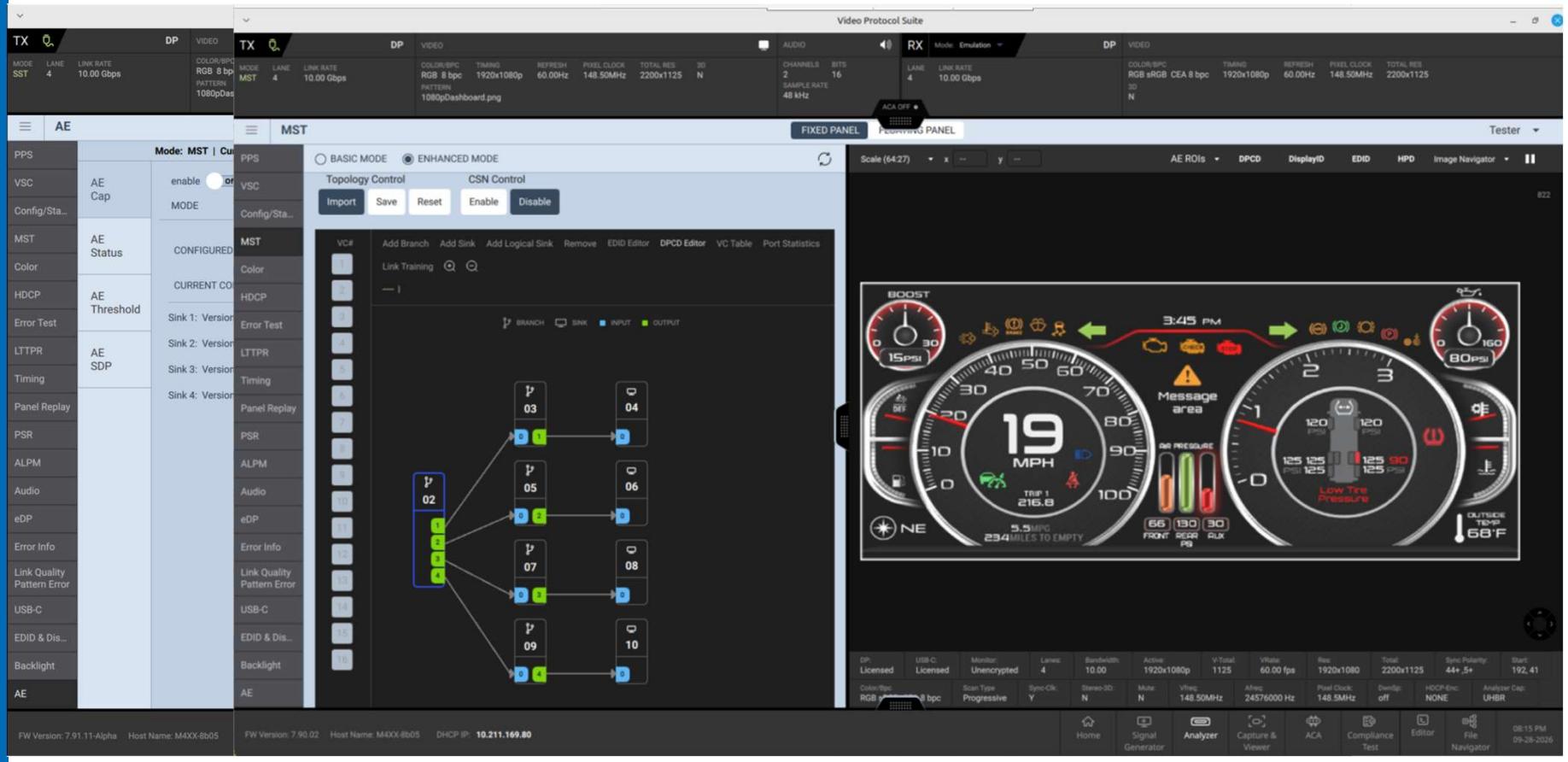
- **配置拓撲、配置文件、流數和版本數.**

分析輸入的DP AE流.

- 觀看狀態。
- 查看輔助通道和邊帶交易。
- 即時查看DP AE次級資料包（SDP）。
- 擷取和分析接收的DP AE流.



# VESA DisplayPort AE – Testing Functional Safety



# VESA DisplayPort AE——功能安全測試

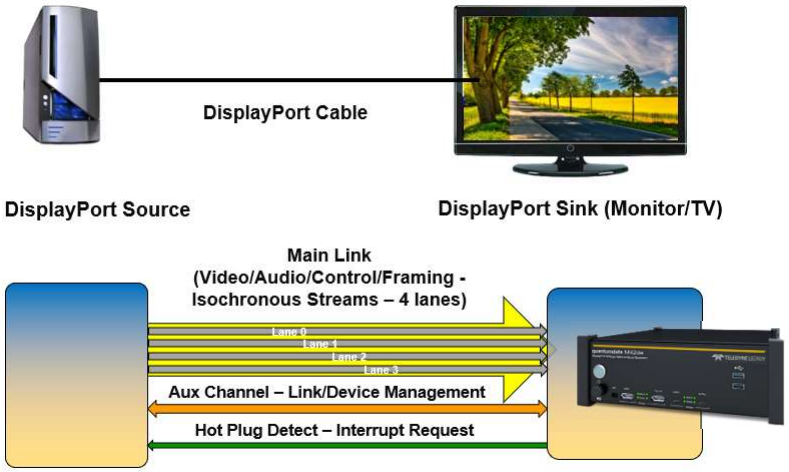
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設定DP AE視訊/協定分析儀.

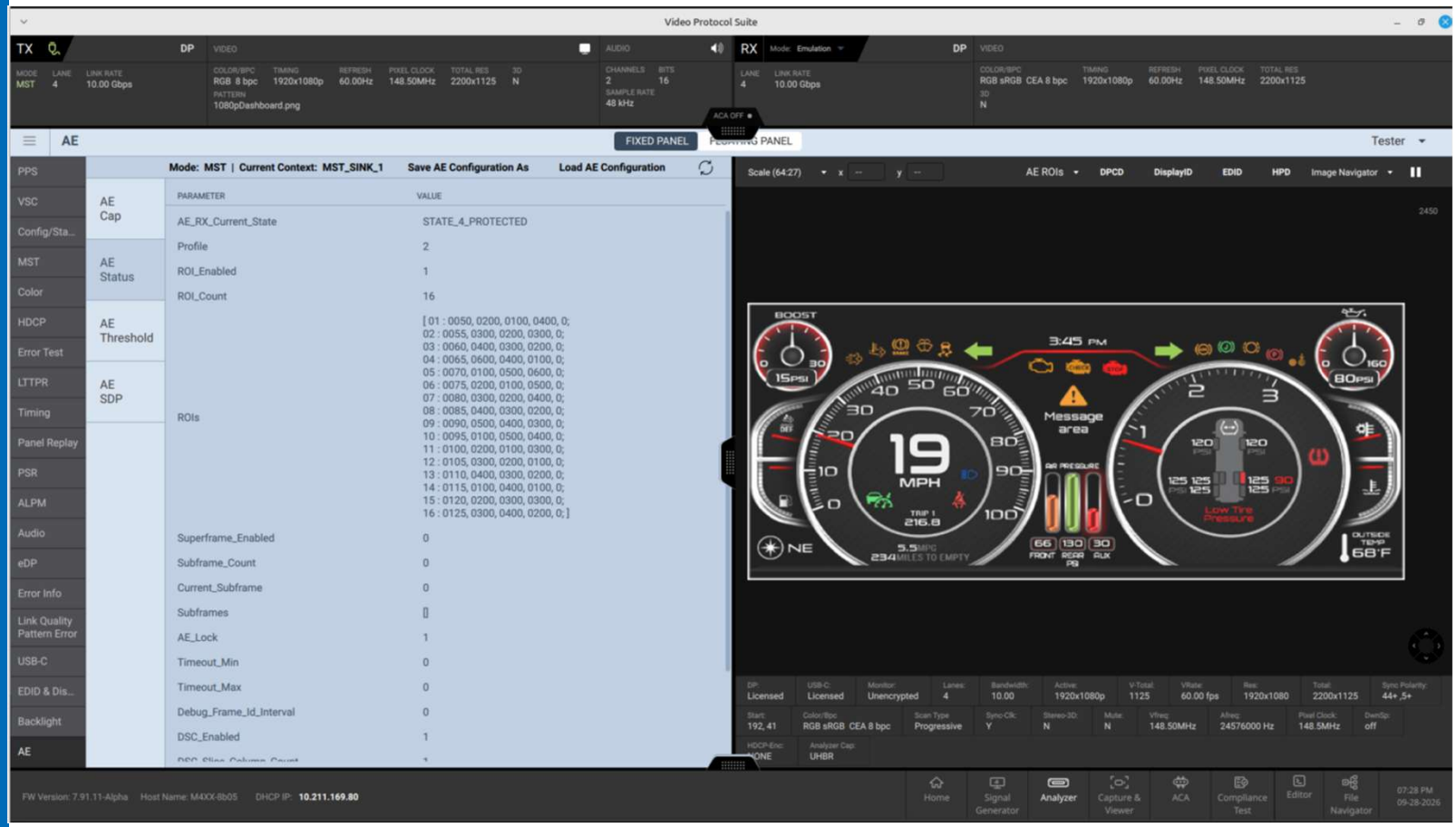
- 配置拓撲、配置文件、流數和版本數.

分析輸入的DP AE流.

- **觀看狀態。**
- 查看輔助通道和邊帶交易。
- 即時查看DP AE次級資料包（SDP）。
- 擷取和分析接收的DP AE流.



# VESA DisplayPort AE – Testing Functional Safety



# VESA DisplayPort AE——功能安全測試

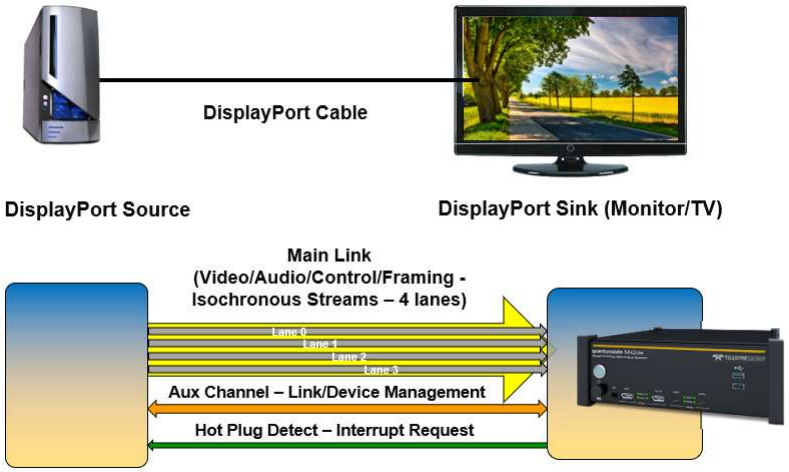
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設定DP AE視訊/協定分析儀.

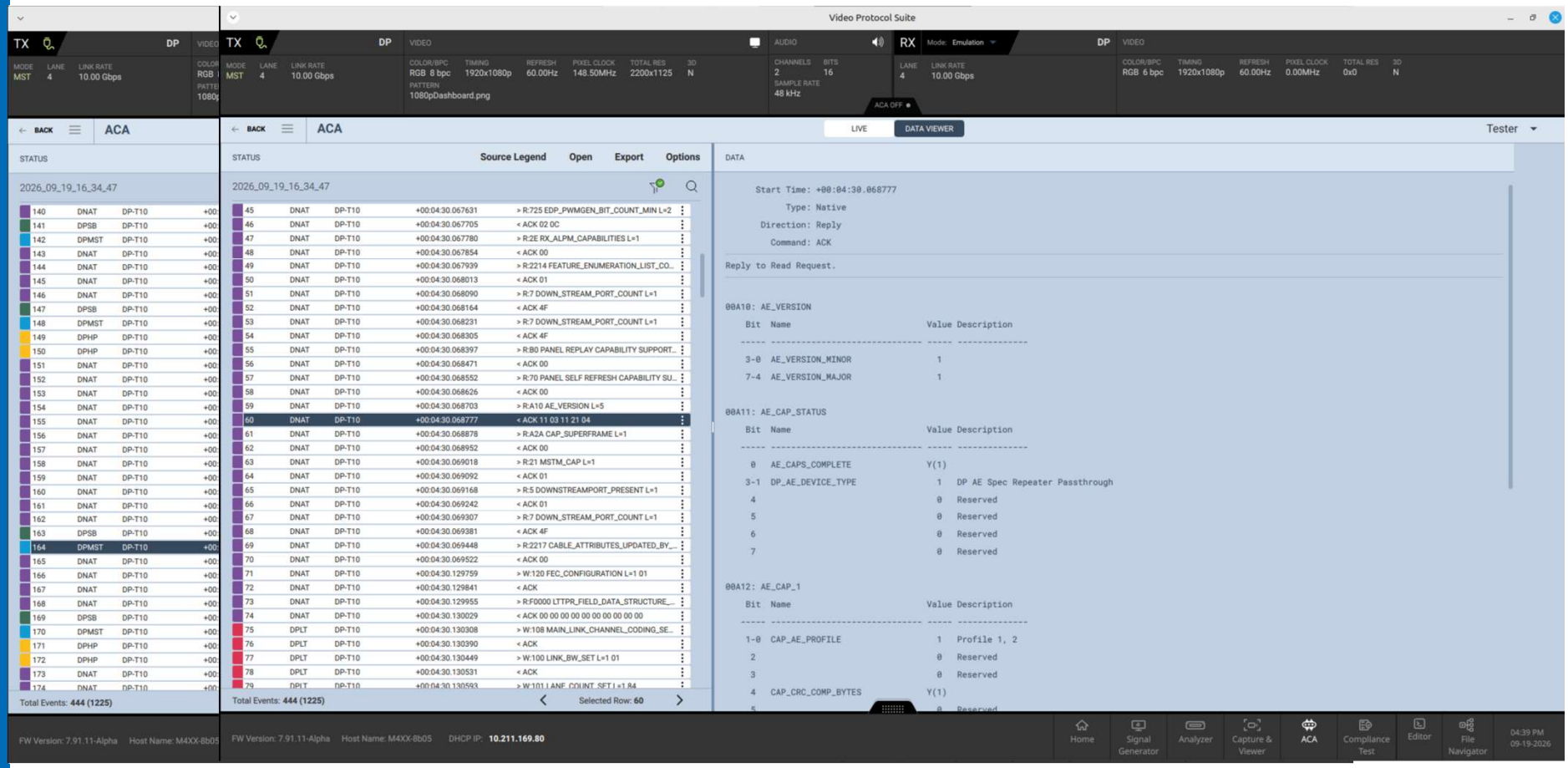
- 配置拓撲、配置文件、流數和版本數.

分析輸入的DP AE流.

- 觀看狀態。
- 查看輔助通道和邊帶交易。
- 即時查看DP AE次級資料包（SDP）。
- 擷取和分析接收的DP AE流.



# VESA DisplayPort AE – Testing Functional Safety



# VESA DisplayPort AE——功能安全測試

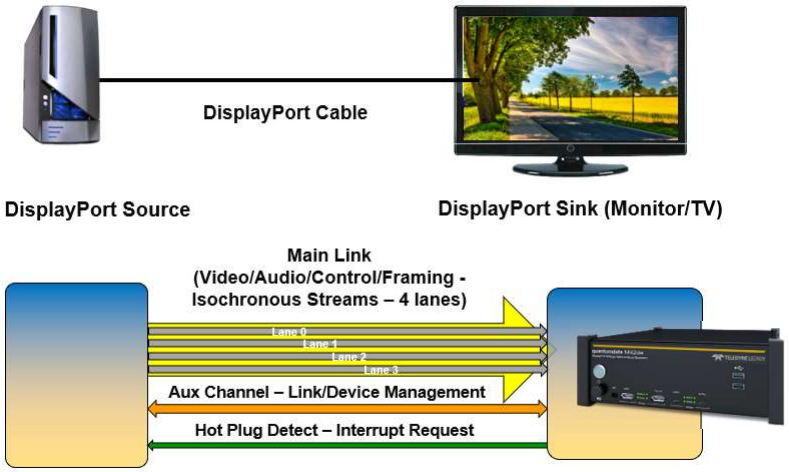
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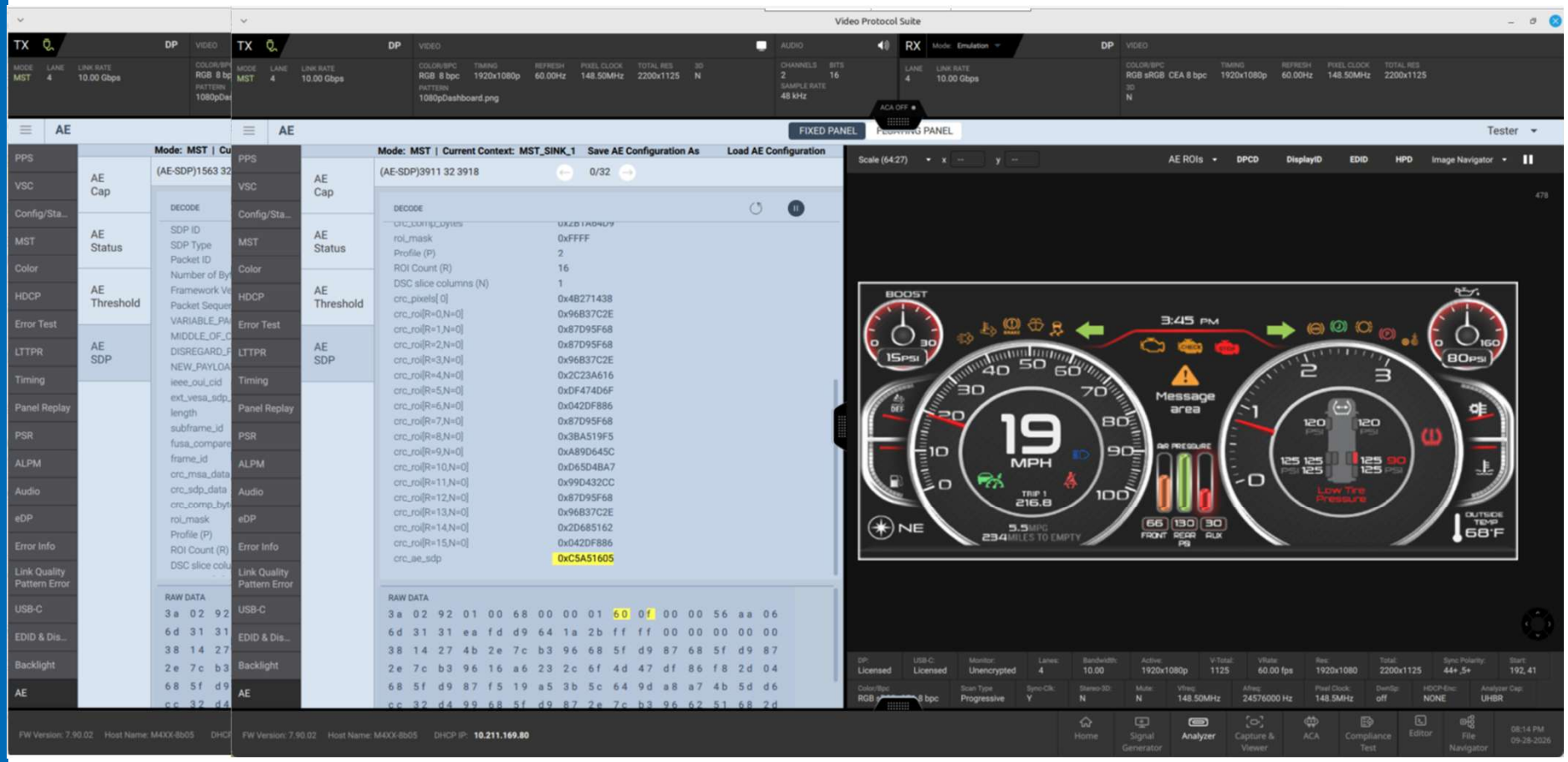
- 配置拓撲、配置文件、流數和版本數.

分析輸入的DP AE流.

- 觀看狀態。
- 查看輔助通道和邊帶交易。
- **即時查看DP AE次級資料包（SDP）。**
- 擷取和分析接收的DP AE流.



# VESA DisplayPort AE – Testing Functional Safety



# VESA DisplayPort AE——功能安全測試

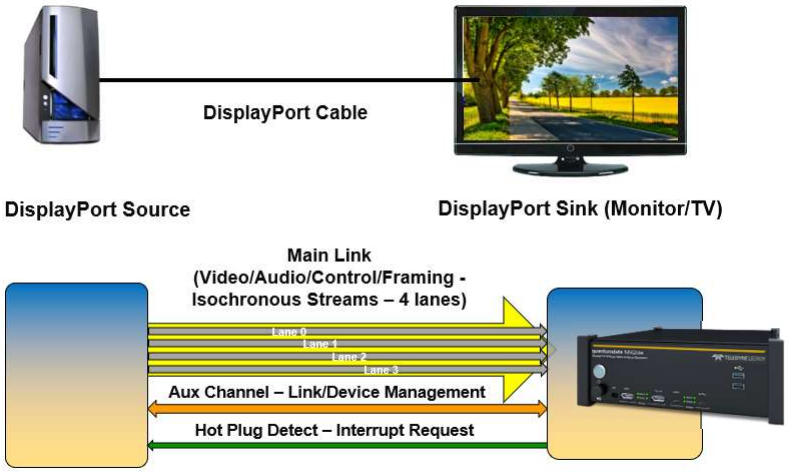
## 如何測試您的DisplayPort汽車擴充實現

設定DP AE視訊/協定分析儀.

- 配置拓撲、配置文件、流數和版本數.

分析輸入的DP AE流.

- 觀看狀態。
- 查看輔助通道和邊帶交易。
- 即時查看DP AE次級資料包（SDP）。
- **捕捉和分析進入的DP客戶獲取數據流及查看投資回報率.**



# VESA DisplayPort AE – Testing Functional Safety



# VESA DisplayPort汽车扩展（DP AE）测试您的功能安全实现

**Neal Kendall/Alok Soni**
Teledyne LeCroy
*2026年10月16日 - 台北，台灣*

VESA

# DisplayPort Electrical Testing Overview

**Abhijeet Shinde**
Keysight Technologies
*October 16, 2026*

# Agenda

- DP2.1 Electrical Compliance Test Requirements
- DP2.1 PHY Updates
- DP2.1 Transmitter Test
- DP2.1 Receiver Test
- eDP PHY Electrical Conformance Testing

# DP2.1a Electrical Compliance Test Requirement

# DisplayPort Interface

## Main Link

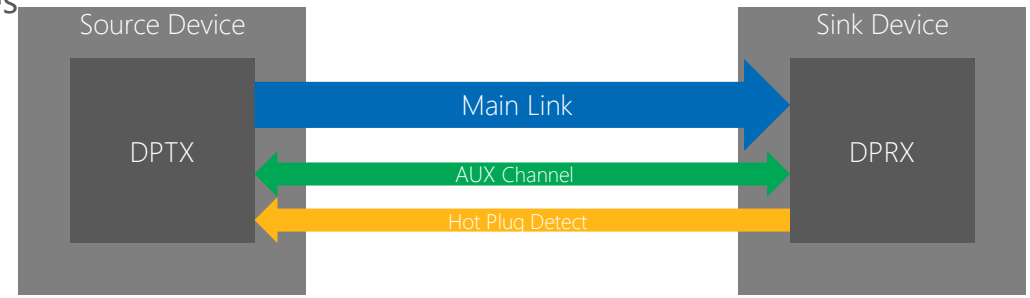
- Display data transfer
- 4 unidirectional high-speed lanes
- Multiple bitrates supported

## AUX Channel

- Link management
- Test mode control
- 1 bidirectional low-speed lane

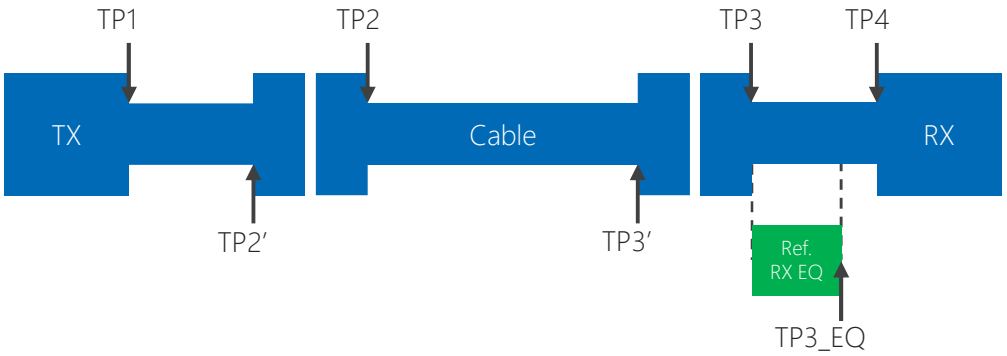
## Hot Plug Detect

- Source detects presence of sink
- Sink notifies of status changes via IRQ



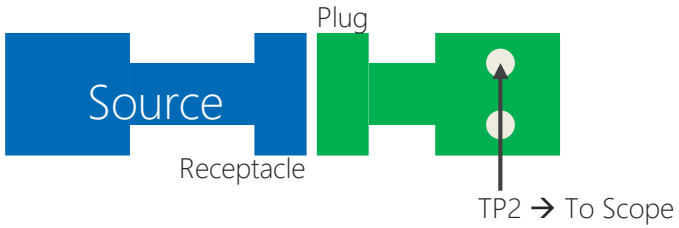
# Test Points

| Test Point | Definition |
|---|---|
| TP1 | Source transmitter pins. |
| TP2 | Test interface of a TPA, next to mated connection to a DP source. |
| TP2’ | RX JTOL signal injection point for DUTs with plug. |
| TP2_CTLE | RX JTOL calibration and test point for DUTs with plug. |
| TP3 | Test interface of a TPA, next to mated connection to a DP sink. |
| TP3’ | Signal injection point to a DP sink. |
| TP3_EQ | TP3 using a defined DP cable model with equalization applied.’ |
| TP3_CTLE | TP3 using a defined HBR3 cable model with CTLE applied. |
| TP3_DFE | TP3 using a defined HBR3 cable model with CTLE and DFE applied. |
| TP4 | Sink receiver pins. |

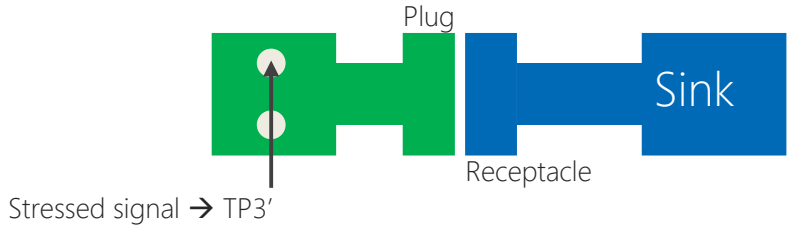


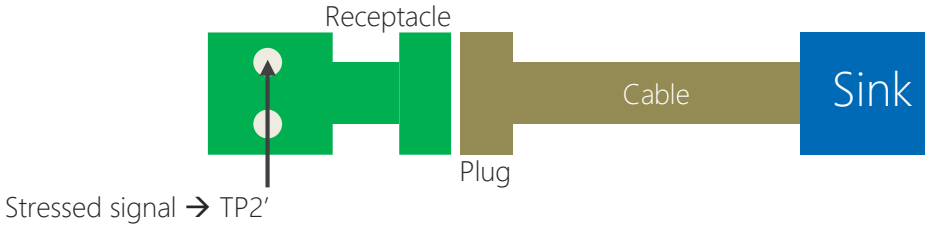
# Test Point Access Examples

## DPTX Testing




## DPRX Testing



# How to test the PHY layer?

**Source**

- Configure the source to output test patterns with certain drive settings → **AUX controller**
- Embed worst-case channels, apply equalization on the oscilloscope
- Run measurements

**Sink**

- Generate the stress signal with a pattern generator
- Guide the sink through Link Training → **AUX controller**
- Read built-in error counter → **AUX controller**

# DP2.1 PHY Updates

# Electrical Updates from DP2.1 to DP2.1a to DP2.1b

- There are minimal changes in 8b/10b electrical compliance testing.
- A new DP54 cable has been introduced in DP2.1a for UHBR13.5.
- The UHBR13.5 Source Enhanced FSDP testing will utilize the new DP54 cable model.
- A new DP80LL cable has been introduced in DP2.1b for UHBR20.
- The UHBR20 Source with 9dB loss budget will utilize the DP80LL cable.
- Changes in test limits primarily affect Source Testing.

- UHBR10
  - DPTX TP2
    - Total Jitter =380 mUI
    - Data-Dependent Jitter =160 mUI
    - Eye Width = 600 mUI
    - Eye Height = 242 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 185 mV
  - DPTX TP3_EQ
    - Total Jitter =450 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 115 mV
  - DPRX TP3_EQ
    - Total Jitter =485 mUI
    - Data-Dependent Jitter =240 mUI
    - Eye Width = 540 mUI
    - Eye Height = 112 mV
- UHBR20
  - DPTX TP2
    - Total Jitter =435 mUI
    - Data-Dependent Jitter =200 mUI
    - Eye Width = 540 mUI
    - Eye Height = 240 mV
  - DPTX TP3_EQ
    - Total Jitter =455 mUI
    - Data-Dependent Jitter =210 mUI
    - Eye Width = 560 mUI
    - Eye Height = 100 mV
  - DPRX TP3_EQ
    - Data-Dependent Jitter =255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV




- UHBR10
  - DPTX TP2
    - Total Jitter =440 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 550 mUI
    - Eye Height = 162 mV
- UHBR13.5
  - DPTX TP2
    - Eye Height = 200 mV
  - DPTX TP3_EQ
    - Total Jitter =515 mUI
    - Data-Dependent Jitter =245 mUI
    - Eye Width = 520 mUI
    - Eye Height = 80 mV
  - DPRX TP3_EQ
    - Total Jitter =530 mUI
    - Data-Dependent Jitter =260 mUI
    - Eye Width = 520 mUI
    - Eye Height = 73 mV
- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI

- UHBR20
  - DPTX TP2 EnhDP
    - Total Jitter =495 mUI
    - Data-Dependent Jitter =220 mUI
    - Eye Width = 530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ EnhDP
    - Total Jitter =510 mUI
    - Data-Dependent Jitter =242 mUI
    - Eye Width = 550 mUI
    - Eye Height = 84 mV
  - DPRX TP3_EQ EnhDP
    - Data-Dependent Jitter =265 mUI
    - Eye Width = 510 mUI
    - Eye Height = 80 mV

DPTX TP2 USB-C
- Total Jitter =480 mUI

DPTX TP3EQ USB-C
- Total Jitter = 500 mUI




- UHBR20
  - DPTX TP2 EnhDP DP80
    - Total Jitter = 480 mUI
    - Data-Dependent Jitter = 200 mUI
    - Eye Width =540 mUI
    - Eye Height = 240 mV
  - DPTX TP2 EnhDP DP80LL
    - Total Jitter = 495 mUI
    - Data-Dependent Jitter = 220 mUI
    - Eye Width =530 mUI
    - Eye Height = 170 mV
  - DPTX TP3_EQ for all connector Type
    - Total Jitter = 500 mUI
    - Data-Dependent Jitter = 210 mUI
    - Eye Width =560 mUI
    - Eye Height = 100 mV
  - DPRX TP3EQ for all connector type
    - Data-Dependent Jitter = 255 mUI
    - Eye Width = 520 mUI
    - Eye Height = 96 mV

# DP2.1 PHY CTS v1.01 Changes

- Clarification on 8b/10b SSC Modulation Deviation Limit
- Test fixture insertion loss update
- FFE Preset 15 measurement update
- LTTPR Frequency Variation test update
- Eye Height and Mask requirement update for UHBR Rates
- BERT Preset Calibration
- UHBR Return Loss Test added as Normative
- 8b/10b Sink Test : RBR & HBR TP2 is now Informative

# DP2.1 Transmitter Test

# Electrical Transmitter Tests

| Item | Name | Normative/ Informative |
|---|---|---|
| 3.1 | Eye Diagram Test | Normative |
| 3.2 | HBR/RBR Non-PE Level Verification Test | Normative |
| 3.3 | HBR/RBR PE Level Verification and Maximum Differential Peak-to-Peak Voltage Test | Normative |
| 3.4 | HBR3/HBR2 PE Level and Equalization Verification Test | Normative |
| 3.5 | HBR3/HBR2 $V_{TX_DIFFp\text{-}p_MAX}$ Test | Normative |
| 3.6 | Inter-pair Skew Test | Informative |
| 3.7 | Intra-pair Skew Test | Informative |
| 3.8 | AC Common Mode Noise Test | Informative |
| 3.9 | Non-ISI Jitter Measurement Test | Normative |
| 3.10 | HBR3 TX Differential RL Test | Informative |
| 3.11 | TJ/RJ/DJ Measurement Tests | Normative |
| 3.12 | Main-Link Frequency Compliance Test | Normative |
| 3.13 | Spread-spectrum Modulation Frequency Test | Normative |
| 3.14 | Spread-spectrum Modulation Deviation Test | Normative |
| 3.15 | dF/dT Spread-spectrum Deviation High-frequency Variation Test | Informative |
| xx | Embedded Re-timer Frequency Variation Test | Normative |

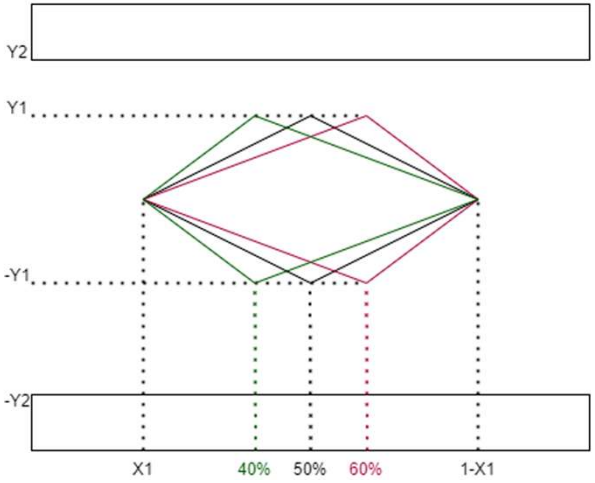
8b/10b

| Item | Name | Normative/ Informative |
|---|---|---|
| 4.2 | Preset and CTLE-DFE Declaration | Normative |
| 4.3 | UHBR Source Transmitter Equalization | Normative |
| 4.4 | UHBR Bit Rate | Normative |
| 4.4 | UHBR Unit Interval | Informative |
| 4.5 | UHBR SSC Down Spread Range, Rate, Phase Deviation, and Slew Rate | Normative |
| 4.6 | UHBR Embedded Re-timer Frequency Variation | Informative |
| 4.7 | UHBR TP2 Eye at 1E-6 BER | Normative |
| 4.8 | UHBR TP2 Jitter at 1E-9 BER | Normative |
| 4.9 | UHBR AC Common Mode Nosie Test | Informative |
| 4.10 | UHBR TP3_EQ Eye at 1E-6 | Normative |
| 4.11 | UHBR TP3_CTLE Jitter at 1E-9 | Informative |
| 4.12 | UHBR Transmitter Return Loss | Informative |

128b/132b

# UHBR Eye Mask Update

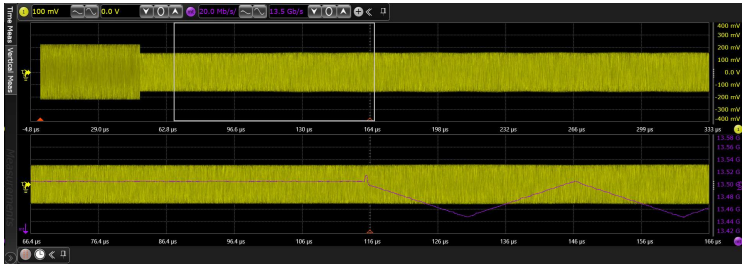
- If original eye mask fails, then modified mask will be used to re-test.
- Modify mask must comply the Y1 and X1 as per the DP 2.1 PHY CTS

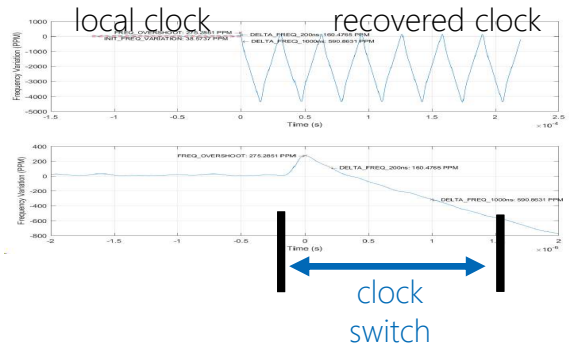





# LTTPR Frequency Variation Test

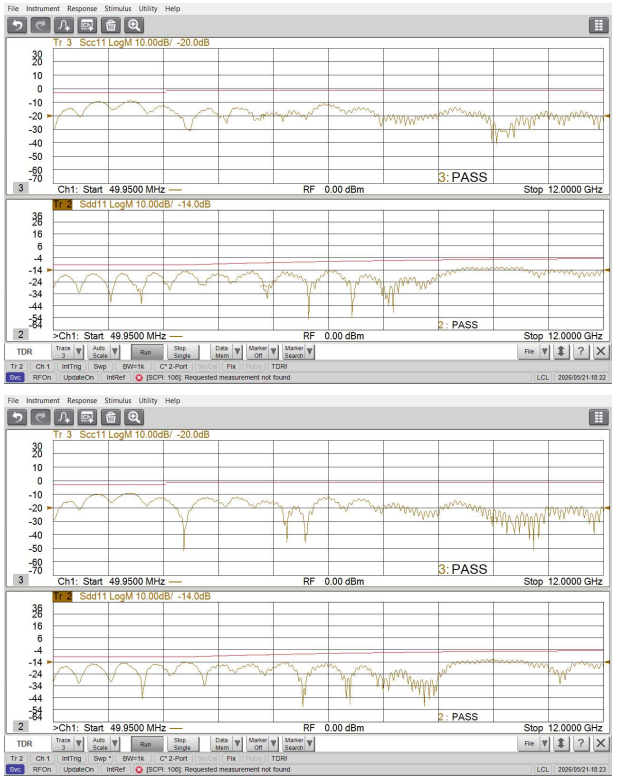
- LTTPRs are needed as total channel loss increases with the PHY rate
  - Longer channel
  - More complex link training
- LTTPR Re-timer Clock Switch Test Mode
  - DPCD 0x0010B – 0x0010Eh [7] =1
- Test Challenges
  - Entering Clock Switch test mode
  - False Triggering
  - Shape of Clock Switch: Overshoot/Undershoot





# Return Loss Test

- RL Pass/Fail depends on
  - VNA configuration → Configuration Included in PHY CTS v1.1
  - Fixture Performance → Impedance within 105 Ω to 75 Ω
    - Criteria included in PHY CTS v1.1
  - DUT in UHBR mode



# DP TX testing challenges

- The test time for DP TX is significant
- DP Source not supporting PHY Test Automation
  - DP Source does not transmit the compliance pattern

# DP2.1 Receiver Test

# Electrical Receiver Tests

| Item | Name | Normative/ Informative |
|---|---|---|
| 5.1 | 8b/10b DP Sink JTOL Test | Normative |

| Item | Calibration Point | Name |
|---|---|---|
| 5.1.3.1.1 | TP1-TP3 | HBR3 Jitter Calibration |
| 5.1.3.1.2 | TP1-TP3 | HBR2 Jitter Calibration |
| 5.1.3.1.3 | TP1-TP3 | HBR Jitter Calibration |
| 5.1.3.1.4 | TP2/TP3 | HBR3 Eye Height and Total Jitter Calibration |
| 5.1.3.1.4 | TP3 | HBR2 Eye Height and Total Jitter Calibration |
| 5.1.3.1.4 | TP3 | HBR Eye Height and Total Jitter Calibration |
| 5.1.3.1.5 | TP1/TP3 | HBR3/HBR2/HBR Crosstalk Calibration |
| 5.1.3.2 | TP2/TP3 | RBR Jitter Calibration |
| 5.1.3.2 | TP3 | RBR Eye Height Calibration |
| 5.1.3.2.1 | TP3 | RBR Crosstalk Calibration |

| Item | Name | Normative/ Informative |
|---|---|---|
| 6.1 | 128b/132b DP UHBR Sink JTOL Test | Normative |

| Item | Calibration Point | Name |
|---|---|---|
| 6.1.3.1.4.1 | TP1 | AC Common-Mode Interference Calibration |
| 6.1.3.1.4.2 | TP1 | Random Jitter Calibration |
| 6.1.3.1.4.3 | TP1 | Periodic Jitter Calibration |
| 6.1.3.1.4.4 | TP1 | Total Jitter Calibration |
| 6.1.3.1.4.5 | TP1 | Eye Height Calibration |
| 6.1.3.1.5 | TP3 | Insertion Loss Calibration |
| 6.1.3.1.6 | TP3 | Eye Diagram Calibration |

# BERT Preset Calibration

- To verify the BERT FFE as outlined in the DP 2.1 PHY CTS specification
- The Preset calibration check can assist in identifying setup problems.

| Set Preset [] | Expected Preshoot [dB] | Measured Preshoot [dB] | Expected Deemphasis [dB] | Measured Deemphasis [dB] | Coeff_1 [] | Coeff0 [] | Coeff1 [] | Pass/Fail |
|---|---|---|---|---|---|---|---|---|
| 1 | 0.00 | 0.10 | -1.90 | -1.75 | 0.030 | 0.870 | -0.100 | Pass |
| 2 | -3.10 | -3.16 | -3.60 | -3.57 | 0.130 | 0.690 | -0.180 | Pass |
| 3 | 0.00 | 0.03 | -5.00 | -4.81 | 0.030 | 0.750 | -0.220 | Pass |
| 4 | 0.00 | -0.20 | -8.40 | -8.25 | 0.030 | 0.655 | -0.315 | Pass |
| 5 | 0.90 | 1.13 | 0.00 | 0.20 | -0.035 | 0.965 | 0.000 | Pass |
| 6 | 1.10 | 1.18 | -1.90 | -1.86 | -0.020 | 0.880 | -0.100 | Pass |
| 7 | 1.40 | 1.35 | -3.80 | -3.60 | -0.020 | 0.810 | -0.170 | Pass |
| 8 | 1.70 | 1.65 | -5.80 | -5.61 | -0.020 | 0.750 | -0.230 | Pass |
| 9 | 2.10 | 2.03 | -8.00 | -7.89 | -0.020 | 0.690 | -0.290 | Pass |
| 10 | 1.70 | 1.82 | 0.00 | 0.13 | -0.080 | 0.920 | 0.000 | Pass |
| 11 | 2.20 | 2.49 | -2.20 | -2.24 | -0.080 | 0.820 | -0.100 | Pass |
| 12 | 2.50 | 2.31 | -3.60 | -3.47 | -0.060 | 0.790 | -0.150 | Pass |
| 13 | 3.40 | 3.57 | -6.70 | -6.64 | -0.070 | 0.700 | -0.230 | Pass |
| 14 | 3.60 | 3.67 | 0.00 | 0.01 | -0.170 | 0.830 | 0.000 | Pass |

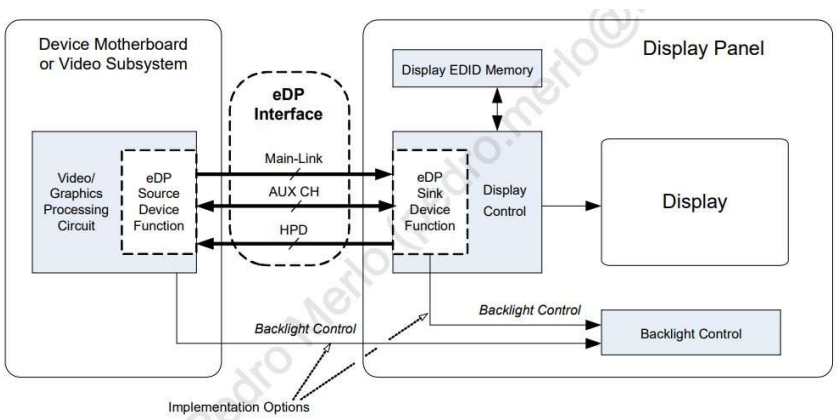
# DP RX testing challenges

- Error count registers not enabled in DP Sink
  - Error count register always report 0 errors
  - USB-C Lane orientation causing failure in error counter and link training
- Calibrations take a significant amount of time
  - Different setup needs for 8b/10b and 128b/132b

# Embedded DisplayPort

# eDP

- Standardized features and interoperability guidelines
  - Feature set determined by the system integrator
- Current specification is eDP2.0
  - Based on DP2.1
- No compliance program = Conformance Test!!



# eDP2.0 Update

- eDP2.0 v1.0 published in September 2024
- Supports 128b/132b encoding
- Supports UHBR data rates
  - UHBR10, UHBR13.5 and UHBR20
- Leverages worst-case end-to-end link budget from DP2.1

# Key Differences eDP2.0 vs DP2.1

**Required**

- DPCD registers for eDP
- Reduced AUX timing
- Enhanced framing
- Fast link training (sink)
- eDP-specific sink noise/jitter budget, reference EQ

**Optional**

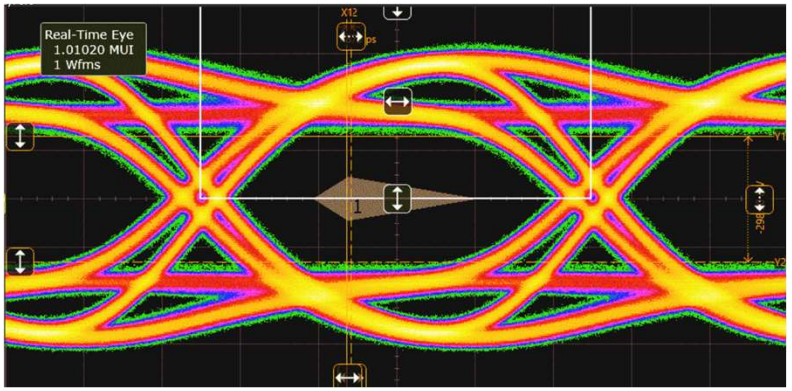
- Low AUX voltage swing
- Source detection by way of AUX CH
- STREAM_STATUS_CHANGED bits support
- GUID registers support
- Fast link training (host)
- Reduced main-link voltage swing level
- EDID
- HPD pin on sink device

**Recommended**

- Fewest number of lanes possible

# Main Link Differences

- Eight 8b/10b rates, and Three UHBR rates
- Custom rates supported
- Total jitter budget at TP3_EQ
- BER = $10^{-9}$
- Custom Differential Signal Voltage
- 1 lane (20-pin eDP), 2 lanes (30-pin eDP) and 4 lanes (40-pin eDP)



# AUX Channel Differences

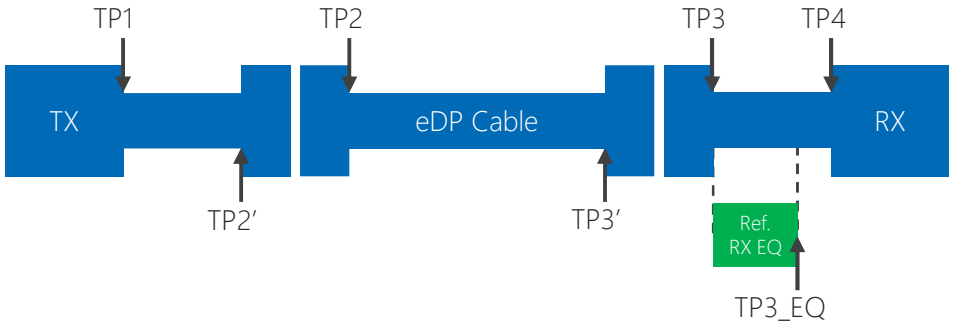
- No AC-coupling capacitors on Sink device side
- No pull-up/-down resistors
- Why?
  - The Sink device does not monitor the common mode voltage on AUX_CH_P and AUX_CH_N for Source device Hot Plug/Unplug and powered/unpowered detection

# eDP Electrical Specification

- Low voltage swing levels
- Framework to apply optional customized voltage swings
- Reduced RX differential voltage sensitivity
- New transfer rates
- Framework to apply jitter specifications to optional customized frequencies
- Same Link Training procedures and voltage swing tables like DP, but with lower signal voltages

# eDP Transmitter Test

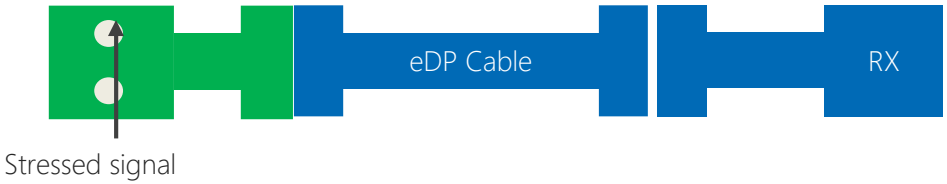
- Test Point/Fixture




| Recommended Source Main-Link TX Electrical Specification |
|---|
| Link Rate |
| Unit Interval |
| Total Jitter |
| Residual ISI |
| Non-ISI |
| Eye Diagram |

# eDP Receiver Test

- Test Point/Fixture




| RX Test |
| --- |
| Sink JTOL Test |

| Calibration Point | RX Calibration |
| --- | --- |
| TP1 | Sinusoidal Jitter Calibration |
| TP1 | Random Jitter Calibration |
| TP3 | Residual ISI |
| TP3 | Eye Diagram |
| TP3 | Crosstalk |

# Thank You!

# VESA
# Display Performance Metrics

Cyan Chen, Global Business Lead, Display Technologies

Granite River Labs

October 16, 2026

# Tables

- VESA DPM Introduction
- VESA Certified — DisplayHDR
- VESA Certified — AdaptiveSync
- VESA Certified — ClearMR
- Summary

VESA

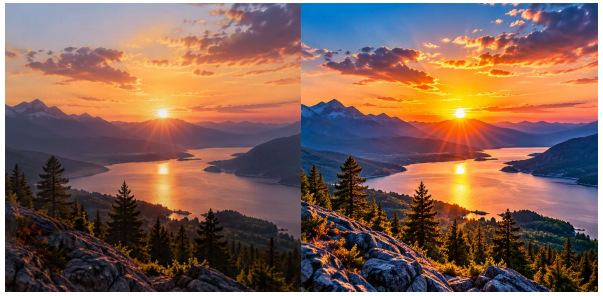
# VESA DPM Introduction

VESA

# VESA Display Performance Metrics (DPM)

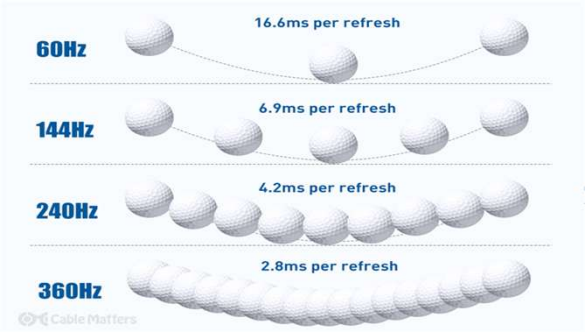
**VESA CERTIFIED DisplayHDR™**

- ✔Better brightness & contrast
- ✔Accurate color reproduction



**VESA CERTIFIED AdaptiveSync DISPLAY 144**

- ✔Dynamic refresh rate
- ✔Prevents tearing & stuttering

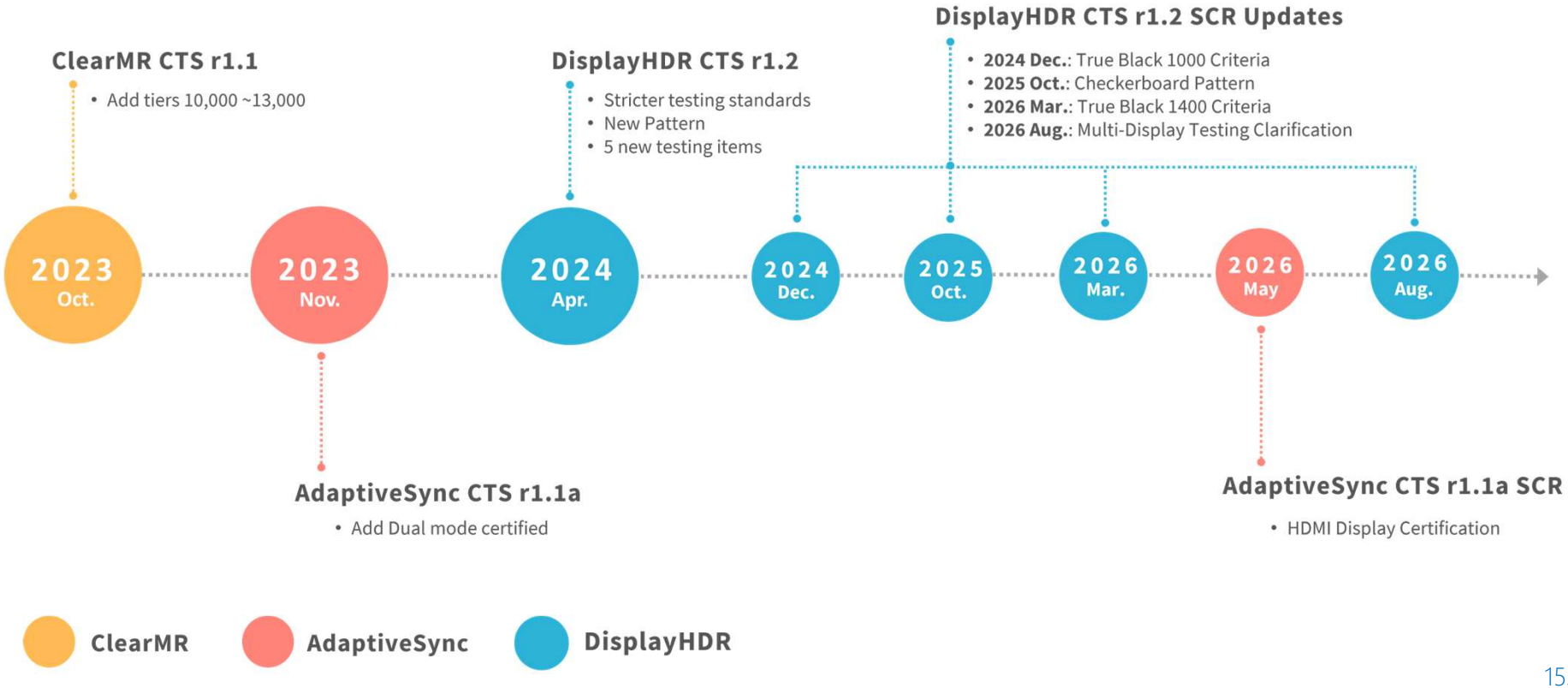



**VESA CERTIFIED ClearMR**

- ✔Motion clarity
- ✔Ratio of clear vs. blurry pixels



# VESA DPM CTS Timeline



VESA

# VESA Certified — DisplayHDR

## The Higher Standard for HDR Monitors

VESA

# DisplayHDR Certification

VESA performance certification for HDR displays

VESA CERTIFIED DisplayHDR™

HDR image quality with higher brightness, color and contrast.

- Peak Luminance
- Color & EOTF
- Contrast



VESA CERTIFIED DisplayHDR™ TRUE BLACK

HDR performance with exceptional deep black for OLED and emissive displays.

- Deep Black Level
- High Contrast
- OLED/ Emissive Displays

**DisplayHDR Performance Tier**

400 | 500 | 600 | 1000 | 1400

**DisplayHDR True Black Performance Tier**

400 | 500 | 600 | 1000 | 1400

Focus of 2026 update

# True Black Performance Tier Update

TB1000 criteria update and TB1400 reintroduction

**Apr. 2024**
**CTS r1.2**
Shared criteria with standard DisplayHDR tiers

**Dec. 2024**
**SCR: TB1000**
Dedicated TB1000 criteria introduced

**May 2026**
**SCR: TB1400**
TB1400 reintroduced with revised criteria

## Key Criteria Update

| Full-screen Luminance (cd/m²) | True Black 1000 | True Black 1400 |
|---|---|---|
| Flash Test | ~~1000~~ → **500** | **700** |
| Long Duration Test | ~~600~~ → **500** | **700** |
| Combined Color Luminance (Lr + Lg + Lb) | ~~600~~ → **500** | **700** |

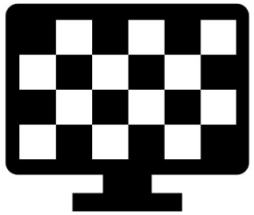
**Both TB1000 and TB1400 apply the same 50% approach for full-screen luminance.**

# True Black Checkerboard Update

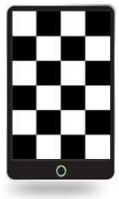
New checkerboard pattern for small-size displays

## Small Display Challenge

Existing checkerboard patterns scale with display size, resulting in measurement areas that become too small on small displays



Larger display
(6 × 4 pattern)

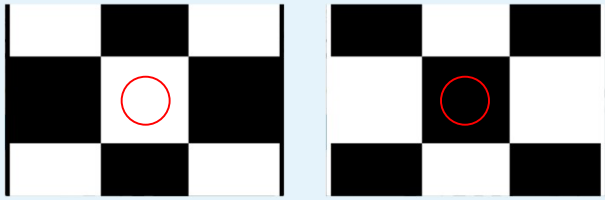


Smaller display
(patches too small)

3 × 3 Applicable Display Sizes
7 ~13" diagonal (16:9)
Other aspect ratios: 87–162 mm screen height

## New 3 × 3 Checkerboard

Introduce a cropped 3 × 3 checkerboard with fixed patch size for small displays



**80 mm**
Fixed test square

**50% Loading**
Auto-maintained

**Center Measurement**
Same probe position

| Display Size | Available Checkerboard |
|---|---|
| Default | 6 × 4 |
| < 20" | Optional 4 × 3 |
| 7–13" (16:9) | Optional Cropped 3 × 3 ***(New)*** |

# Multi-Display Certification Update

Defines certification requirements for devices with multiple integrated displays

## Secondary Displays



Examples:

- Status panel
- Control bar
- Virtual keyboard

**Primary Display Only**
*No testing for secondary display*

## Identical Displays

(Meet Family Member Definition)



**Reduced Test Set**
*for each additional display*

- 8% / Star Field Luminance
- Checkerboard Contrast Ratio
- Color Gamut

## Different Primary Displays

(Do NOT Meet Family Member Definition)



**Full Test Suite per Display**
*All test items required*

Device Certification =
**Lowest Tier Achieved**

VESA

# VESA Certified — AdaptiveSync

## Flawless Frames, Every Time

VESA

# AdaptiveSync Certification

Variable refresh rate certification for smoother, tear-free display performance

VESA CERTIFIED MediaSync DISPLAY

**Optimized for Media Playback**

Max RR ≧ 60Hz ;
Min RR ≦ 48Hz

VESA CERTIFIED AdaptiveSync DISPLAY 144

**Optimized for Gaming**

Max RR ≧ 144Hz
Min RR ≦ 60Hz

**Dual Mode Logo**

VESA CERTIFIED AdaptiveSync DISPLAY 240 2160P DISPLAY 480 1080P

Supports certification with two resolution and refreshrate modes

**240**
Max RR
@ Max Res.

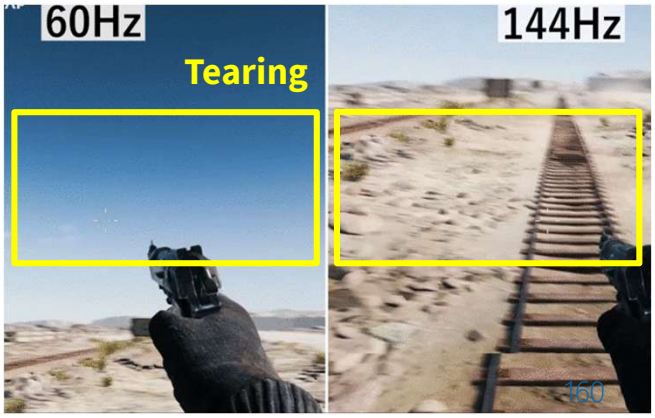
**480**
Max RR
@ Alt. Res.

**Smooth & Tear-Free Motion**

Eliminates screen tearing for better visual experience

**Low Latency & Fast Response**

More responsive and fluid motion performance



VESA

# AdaptiveSync Certification Expanded to HDMI

HDMI displays are now eligible for AdaptiveSync or MediaSync certification

DisplayPort

NEW

HDMI
HIGH-DEFINITION MULTIMEDIA INTERFACE



VESA CERTIFIED AdaptiveSync DISPLAY 144

VESA CERTIFIED MediaSync DISPLAY

### HDMI Eligible

AdaptiveSync / VRR via HDMI

### Same VRR Behavior

Equivalent panel-level operation

### Same CTS Requirements

Existing requirements still apply

# Adaptive-Sync Multi-Mode Certification

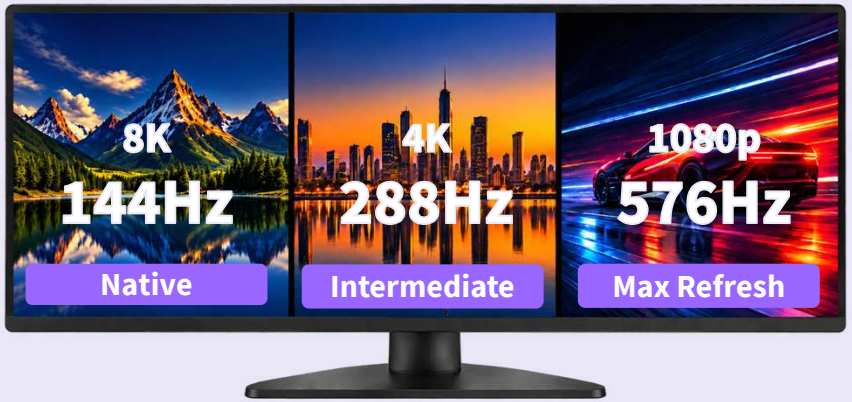
Expand from Dual mode to Multi-mode, enabling certification for displays with more than two modes

## Dual mode




2-Certified Modes

## Multi-mode




3+ Certified Modes

### 01 Dual mode Baseline

Native + Max Refresh modes remain required

### 02 All Modes Certified

All modes must meet AdaptiveSync requirements

### 03 Flexible Scaling

Non-integer scaling & different aspect ratios allowed

### 04 Testing Impact

Warm-up is required for each certified mode

VESA

# VESA Certified — ClearMR

## Clarity in Motion

# ClearMR Certification

Motion Clarity Performance for Displays

VESA CERTIFIED ClearMR 13000

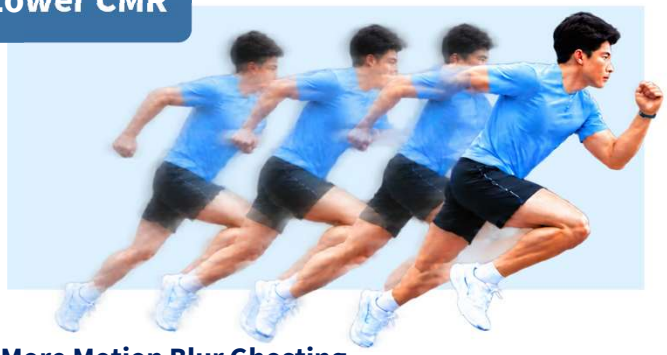
Clear Pixels : blurry pixels = 130 : 1

- Standardized motion quality metric
- Smoother motion, less ghosting

**ClearMR Tiers**

- 3000
- 4000
- 5000
- 6000
- 7000
- 8000
- 9000
- 10000
- 11000
- 12000
- 13000
- 15000
- 18000
- 21000

**Lower CMR**



More Motion Blur Ghosting

**Higher CMR**



Clearer Motion with Less Visible Blur

VESA

# Summary

VESA

# DPM Key Takeaways

Key Updates Across DisplayHDR, AdaptiveSync & ClearMR

VESA CERTIFIED DisplayHDR™

VESA CERTIFIED DisplayHDR™ TRUE BLACK

VESA CERTIFIED AdaptiveSync DISPLAY 144

VESA CERTIFIED MediaSync DISPLAY

VESA CERTIFIED ClearMR 13000

## Expanded Certification Coverage

- TB1000 / TB1400 criteria updates
- Small-display checkerboard support
- Multi-display certification

## More Certification Flexibility

- HDMI now eligible for certification
- Dual-Mode expanded to Multi-Mode
- More display modes can be certified

## Motion Clarity Benchmark

- Standardized clear-to-blurry pixel ratio
- ClearMR tiers: 3000 → 21000
- Higher CMR = better motion clarity

# GRL Worldwide Locations



**Genk Lab**
- EMC / EMI
- Performance Testing
- Protocol Testing
- Wireless

**Incheon Lab**
- Performance Testing
- Wireless

**Taipei Lab**
- Performance Testing
- Protocol Testing
- Wireless

**Karlsruhe Lab**
- Safety Certification
- EMC / EMI
- Performance Testing
- Protocol Testing
- Wireless

**Bangalore Lab**
- Safety Certification
- Protocol Testing
- Wireless
- Cybersecurity

**Dongguan Lab**
- Safety Certification
- Performance Testing
- Protocol Testing
- Wireless

**Shanghai Lab**
- Safety Certification
- Performance Testing
- Protocol Testing
- Wireless

**Yokohama Lab**
- Performance Testing
- Protocol Testing
- Wireless

**Santa Clara Lab**
- EMC / EMI
- Performance Testing
- Protocol Testing
- Wireless

# Lunch Break

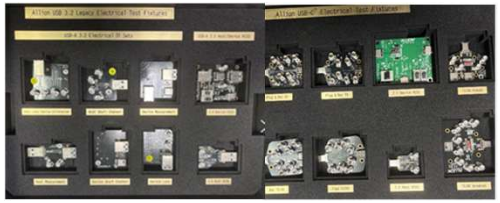
*Sessions will resume at 1 pm*

# Allion Demo Table

- Test Fixtures



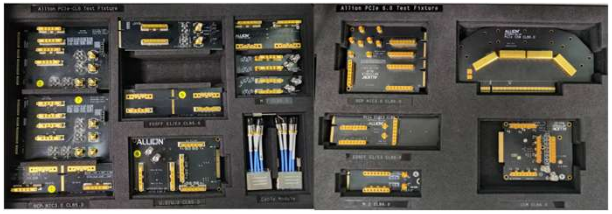

DisplayPort USB-C TO DP Cable



USB-C PHY Test




HDMI 1.x & 2.x PHY Test



PCI-E Gen 5 & 6 PHY Test

- VESA Certified DP80LL LRD Cables



Luxshare-ICT 3M DP-DP

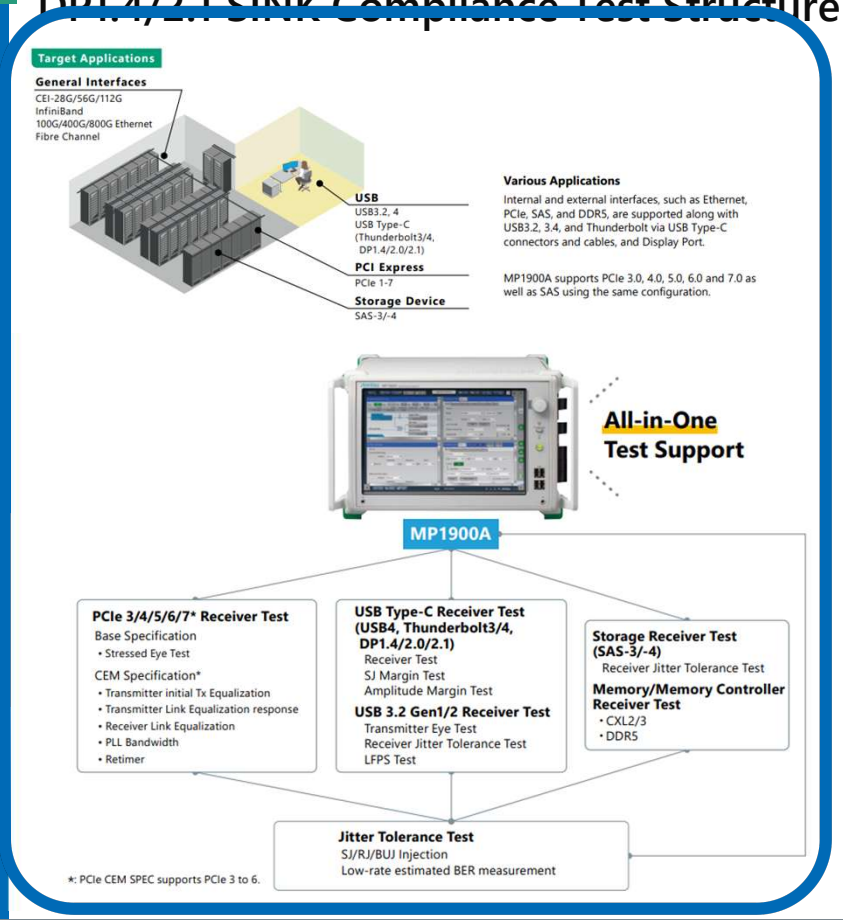


Luxshare-ICT 3M USBC-USBC

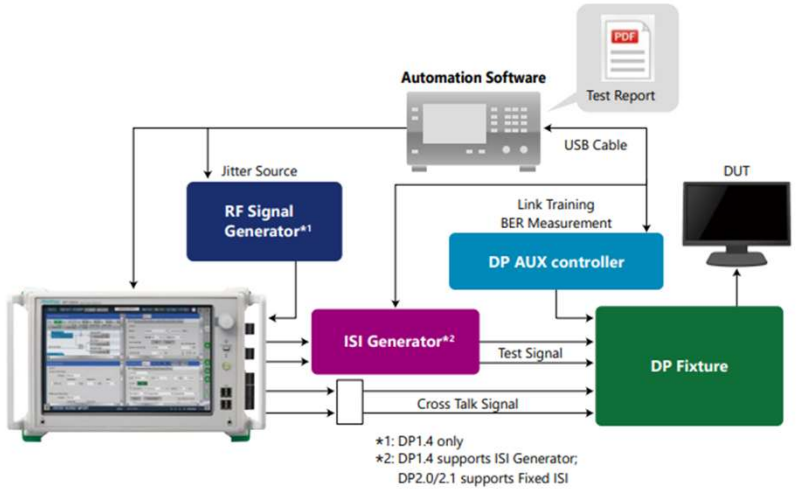


Luxshare-ICT 3M USBC-DP

# Anritsu MP1900A Signal Quality Analyzer
## DP1.4/2.1 SINK Compliance Test Structure




**DisplayPort 1.4/2.0/2.1 Sink Test**



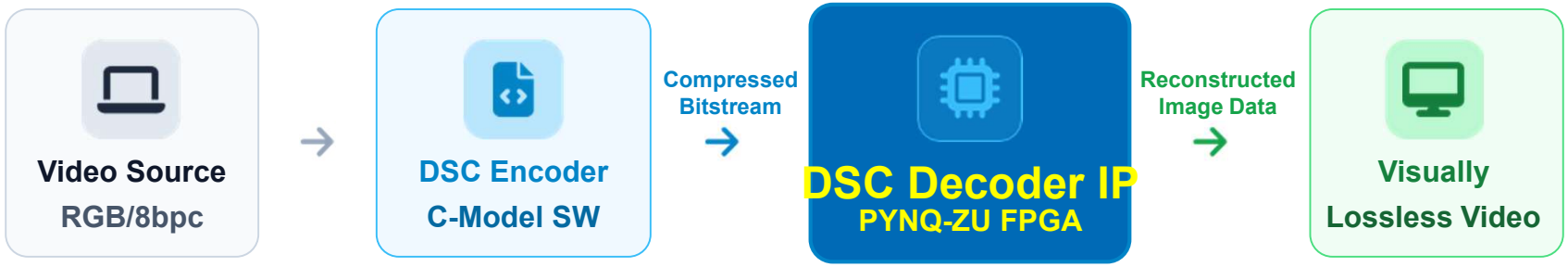

**Required Functions**

- 2.7 Gbit/s to 20 Gbit/s PPG
- Stressed Signal Calibration and Test
- USB Type-C Alternative Mode Operation

CYBERTEK SOLUTION

# VESA DSC Decoder IP Core Demo

## Demo Table




## IP Core Key Features & Specifications

### Compliance
**VESA DSC 1.2a & 1.2b**
Fully standard compliant.

### Coding Modes
**MMAP / BP / MPP / ICH**
Full picture coding suite.

### Color & Depth
**RGB & YCbCr Native**
4:4:4 / 4:2:2 / 4:2:0 (8-12 bpc)

### Performance
**3 Pixels / Clock**
High throughput hardware.

*Configurable features for gate count and speed !*

# eDP and DisplayPort Protocol Analysis and Validation Real Time *ANY* Source to *ANY* Sink

FuturePlus Systems

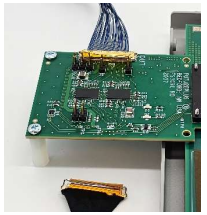
Advancing Technology Development






NEW

***eDP 2.0 Protocol Analysis With 128b/132b Decode!***



NEW

*eDP Status and Timing Breakout Board*




***Features:***

- ***Panel Self Refresh (PSR) and Selective Update Status***
- Connect Test Points to oscilloscope, mixed-signal oscilloscope, or timing analyzer
- ***Test Points can be customized!***

***All Supported!***

- ***eDP 2.0 with 128b/132b Decode***
- Panel Replay
- Aux-Less ALPM
- **UHBR13.5**



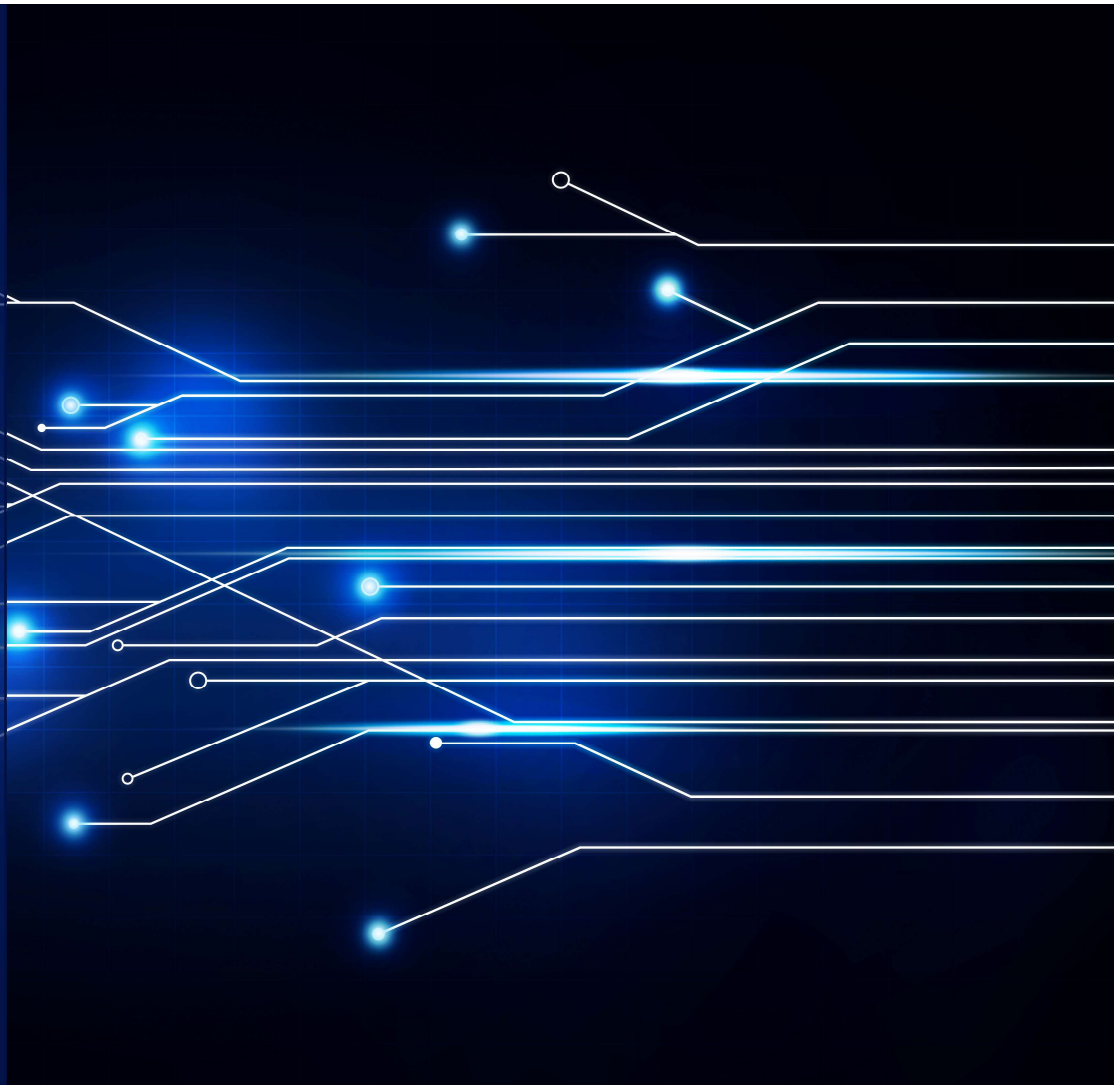

***Something Special? We Like Challenges!***

GRL By SGS

# GRL VESA Certification Testing Services

GRL Taiwan | VESA Workshop 2026

graniteriverlabs.com



# GRL VESA Certification Testing Services

Supporting Your VESA Certification Journey

DisplayPort

### DP Source & Sink Certification

- DP 1.4 & DP 2.1 (UHBR 10 / 13.5 / 20)

VESA CERTIFIED DisplayHDR™

### HDR Picture Quality Certification

- Multiple performance tiers (400 ~ 1400 / True Black)




VESA CERTIFIED AdaptiveSync DISPLAY 144

### Variable Refresh Rate Certification

- Variable refresh rate performance validation

VESA CERTIFIED ClearMR 13000

### Motion Clarity Certification

- Multiple performance tiers (ClearMR 3000 ~ 21000)

## GRL Service Scope

**Pre-Compliance**
Early issue identification

**Compliance Testing**
VESA compliance testing

**Debug Support**
Analysis & troubleshooting

**Certification Support**
Certification follow-up

## Why GRL

- VESA Authorized Test Center with **10+ years** of VESA compliance testing experience
- **3000+ products tested** across DisplayPort, DisplayHDR, AdaptiveSync, and ClearMR
- Global labs, local support in your time zone

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GRL PLATFORM SOLUTIONS

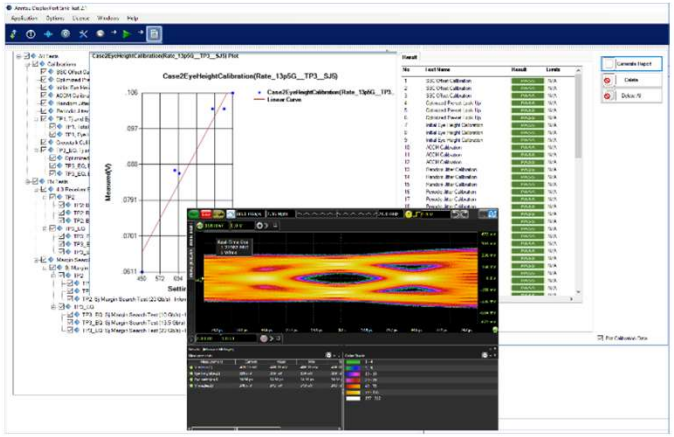
FOUNDATIONAL - INTELLIGENT - PRECISE

# GRLPS DisplayPort

DP2.1 Tx PHY Test Solution
DP2.1 Rx PHY Test Solution
DPAM Test Solution

www.grlps.com

# GRL Platform Solutions (www.grlps.com)






- USB Power Delivery Specification 3.2
- Type-C ® Functional Specification
- IEC Functional Safety ( IEC 62368-1 )
- 
- Thunderbolt 3/4/5 Alternate Mode Tests
- Thunderbolt 3/4/5 Power Tests
- Qualcomm® Quick Charge 2™
- Qualcomm® Quick Charge 3™ and 3+™
- Qualcomm® Quick Charge 4™ and 4+™
- Qualcomm® Quick Charge 5™
- BC 1.2 for QC Sink products
- IEC 63680-1-2




The only instrument you need for validating compliance, inter-operability, and reliability of your designs

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# Beyond Standard Compliance — Accelerate Your Signal Integrity Debug.

Specialized in high-speed interfaces and power architectures: your technical ally from testing to troubleshooting.

### Official Certification

Full compliance testing for USB4 / PD 3.2, HDMI 2.2, and DisplayPort 2.1.

**Standard Assurance**

### SI Debug Consulting

Signal integrity, eye diagram jitter, and layout optimization.

**Root-Cause Analysis**

### Test Automation

Custom automated measurement and calibration setups for rapid mass production.

**Faster Time-to-Market**



labs-insight.com

**Bring Your Design Specs for On-Site Advice!**
Senior test & SI engineers ready at our booth for direct consultation.

VESA · HDMI · USB-IF Authorized Lab

**Supported Application** USB4 / PD 3.2 | HDMI 2.2 | DisplayPort 2.1 | PCIe / MIPI / SATA

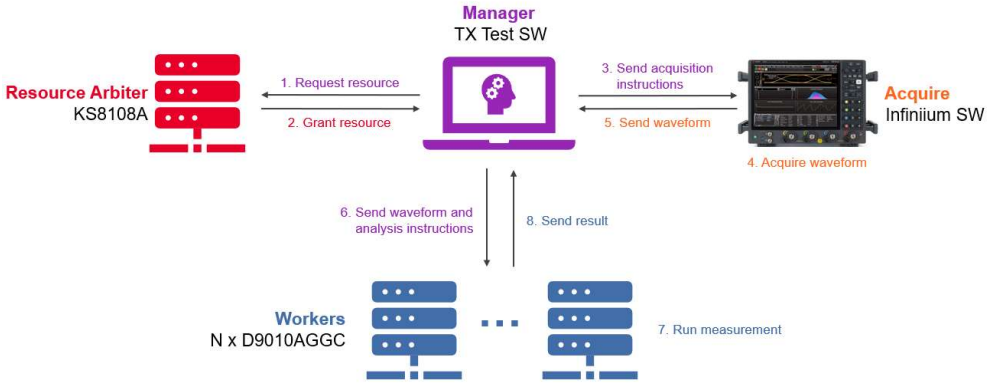

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KEYSIGHT

# Maximizing Time Efficiency & Prepared for the Future


- Contact Information
  - Abhijeet Shinde
  - Abhijeet.Shinde@keysight.com

Keysight Technologies








## XR8 + Disaggregation = Time Efficiency

**What are your costs?**
- A comprehensive test plan leads to prolonged testing durations.
- A majority, about 75%, of the testing period is consumed by data processing.

**What would be an optimal solution?**
- Considerable reduction in test time through Measurement Disaggregation.
- Maximizes the use of your existing investment.
- $$$ Cost-effective savings.
- Enhances your current equipment and expertise.

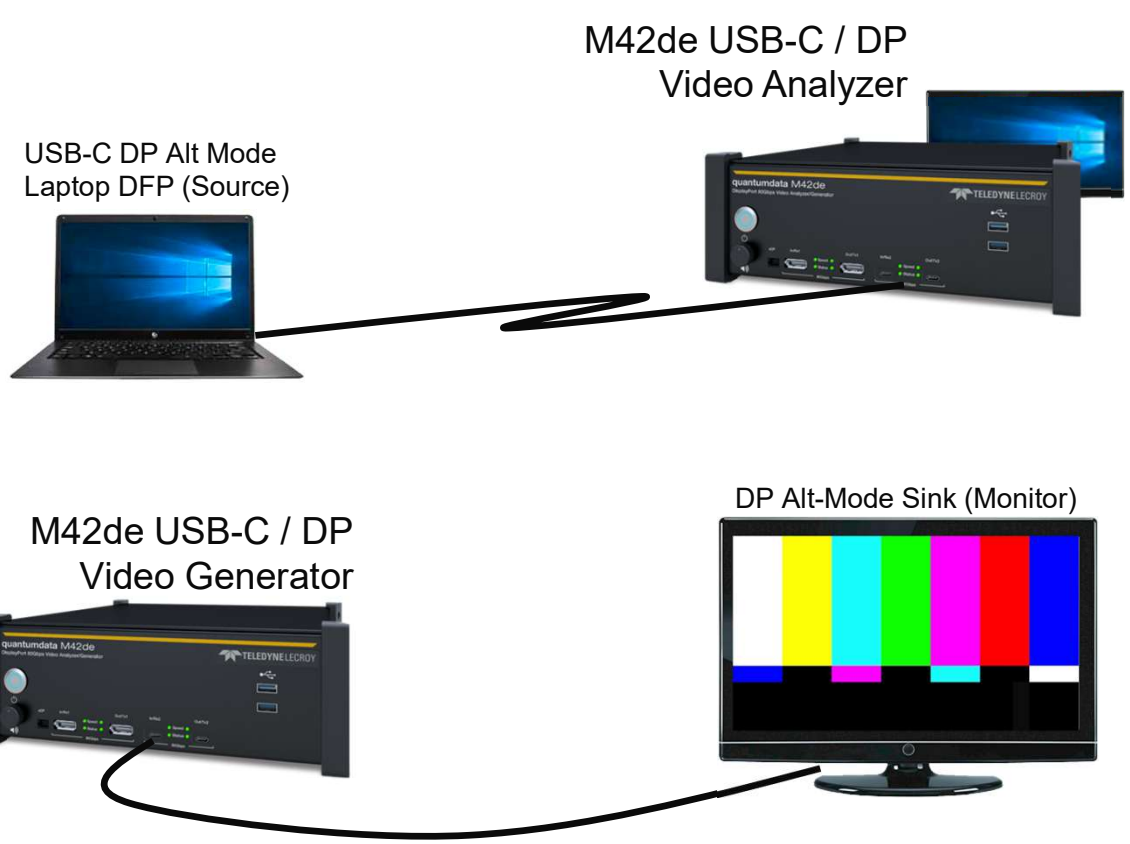
KEYSIGHT

## M8050A: Prepared for the future

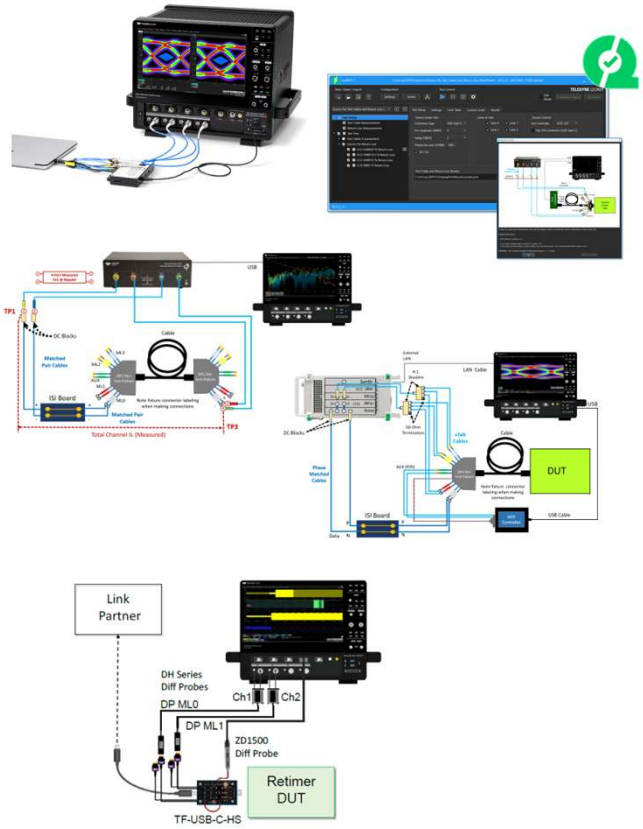
**What are your costs?**
- Investment in hardware to meet next-generation requirements
- Reduced passing margin

**What would be the optimal solution?**
- Reliable support for up to 120GBd and various PAM types
- Provides the lowest intrinsic noise, enhancing passing margin
- Facilitates hassle-free stress calibration, saving both time and money

# M42de Supports DP2.1 SRC/SNK Testing




- Protocol Analysis - Source Testing
  - Sink emulation EDID, DPCD.
  - Protocol Analysis – Main Link & Aux
  - Compliance Testing - Link Layer, (including FEC), DSC, HDCP.
- Video Generation - Sink Testing
  - Source emulation and Link Training control.
  - Video Pattern Testing –generation of Display Stream Compression (DSC) Panel Replay and FEC.
  - Compliance Testing (Link Layer, FEC, HDCP).
- DP Alt Mode Testing
  - Run all VESA source and sink testing through the USB-C DP Alt Mode ports.




- DisplayPort 2.1 Source (Tx) Compliance
  - WaveMaster/SDA 8000HD with QualiPHY® 2 software
  - SDAX-DP expert analysis – Find Best CTLE/DFE
  - Reduced test times with QPHY2-PC
  - Automated Return Loss with WavePulser 40iX
- DisplayPort 2.1 Sink (Rx) Compliance
  - WaveMaster/SDA 8000HD with QualiPHY 2 software
  - SSG Cal and BER testing using Anritsu MP1900 SQA
  - Automated Channel Cal with WavePulser 40iX
- PHY-Logic (Interop) Debug
  - AUX Triggered + Main Link capture
  - TF-USB-C-HS – probing access
  - DP-AUX, USB-PD TDMP software
  - Clock switch testing on live link

Teledyne Confidential; Commercially Sensitive Business Data

# Voyager M4120

## Complete USB4® v2 Solution

**Analyzer, Exerciser, & Compliance Tester**

## Asymmetric Link Capture

Capable of capturing and testing 120Gb/s Asymmetric Link Configurations

## Traffic Decoding & Unified Workflow

HopIDs Automatically Detected; **Tunneled DisplayPort Decoded**

Single Click Export Native **DisplayPort Traffic**, view in VPS




## All Speeds, One Unit

- USB4 v2 120Gb/s (PAM3, Asymmetric)
- USB4 v1 40Gb/s (NRZi)
- Thunderbolt™ 5, 4, & 3
- USB 3.2, USB 2.0
- USB-PD, & Type-C

TELEDYNE | LECROY

# USB Explorer™ 350

- Protocol Analyzer
- Traffic Generator
- Automated Compliance Tester

- USB Type-C™
- Display Port ALT Mode
- USB Power Delivery (USB PD) 2.0 and 3.0*
- USB Type-C™ Cables and Connectors
- SuperSpeed USB 10Gbps (USB 3.1 Gen 2)
- SuperSpeed USB (USB 3.1 Gen 1)
- USB 2.0 High Speed

SYMBIOSYS Alliance Member




ellisys
Better Analysis

# UCD-500 Gen3

## 16K DP 2.1b Generator & Analyzer

- DP 2.1b Sinks and Sources up to 8K@60Hz
- Supports DP and USB-C connectors
- DP 2.1b and DP 1.4a Link Layer CTS including DSC, LTTPR, DisplayID/EDID, MST, Adaptive-Sync and more.




# UTC-274

## USB Type-C Tester for Test Automation

- Test DP Alt Mode, Power Delivery and USB speed
- 2 upstream USB-C test ports
- EPR function test up to 240W Source and Sink



# DP LRD Active Cable Testing

**Lexus Lee, Technical Program**
Allion Labs, Inc.
*October 16, 2026*

# Overview

- Why VESA Defines LRD Active Cable Spec
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA  Connector Certification Introduction
- Cable Next - Active Optical Cable?

# Overview

- Why VESA Defines LRD Active Cable Spec
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA  Connector Certification Introduction
- Cable Next - Active Optical Cable?

# Why VESA Defines LRD Active Cable Spec

- Enable UHBR20 transmission over a 2-meter cable
  - Only works for 1-meter passive cable, which cannot meet all use-case requirements
- LRD Active Cable Type for VESA Certification

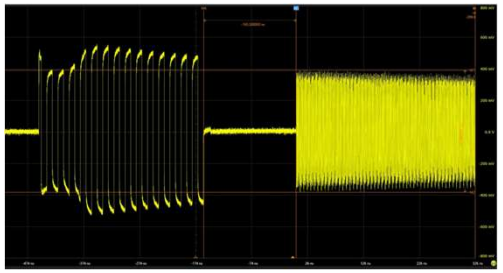


# Overview

- Why VESA Defines LRD Active Cable Spec
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
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- Cable Next - Active Optical Cable?

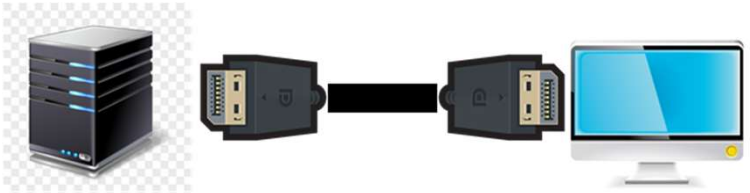
# What Is Inside VESA LRD Cable CTS?

- Time Domain test
  - Eye Diagram
  - Instantaneous Common Mode Voltage
  - CONFIG2 Voltage and No DP_PWR thru Cable
  - AUX-Less ALPM
  - LOS Test
  - Inrush Current Test
  - AUX Voltage Clamping
  - Preset Distortion Thru the cable



# What Is Inside VESA LRD Cable CTS? Cont’

- Functional test
  - Successful Link Training
    - All data rate(from RBR to UHBR20)
    - All lane count (1-Lane, 2-Lane,4-Lane)
    - Bidirectional (Swap Sink/Source end)
    - Power management (Active Power ,Wake/Sleep, Aux-less ALPM)
    - USB-C Orientation (Flip/Normal)



  - SOP/SOP’ Response Check(SVDM2.0/SVDM2.1)

# What Is Inside VESA LRD Cable CTS? Cont'

- Frequency Domain test
  - Insertion Loss Fit
  - Receiver Margin Evaluation
  - IRL Integrated Return Loss

**Table 4-14: DP80LL Nyquist Frequencies and their ILFitAtNq Mandates (Normative)**

| Nyquist Frequency (GHz) | DP-to-DP and USB-C-to-DP ILFitAtNq Mandate (dB)[a] |
|---|---|
| 15.00 | > -10.40 |
| 12.50 | > -9.50 |
| 10.00 | > -6.50 |
| 6.75 | > -5.20 |
| 5.00 | > -4.55 |
| 2.70 | > -3.25 |
| 0.10 | > -1.00 |

*a. Cable values are measured mated pair-to-mated pair.*

### 8.3.3 Receiver Margin Evaluation

*Channel Operating Margin (COM) ≥ 3 dB*

**Table 8-6: LRD Cable IRL Limits**

| Mode | IRL Limit |
|---|---|
| DP80 | *if (-4 dB ≤ ILfit@Nq): IRL ≤ -13 dB*<br>*if (ILfit@Nq < -4 dB): IRL ≤ ILfit@Nq – 9* |
| DP54 | $IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 8.784$ |

# Update About LRD Active Cable in DP 2.1b Spec

- DP80LL (Low Loss)
  - The only difference between the DP80LL and DP80 cable spec is the IL FitAtNq requirement.

**Table 4-14: DP80LL Nyquist Frequencies and their ILFitAtNq Mandates (Normative)**

| Nyquist Frequency (GHz) | DP-to-DP and USB-C-to-DP ILFitAtNq Mandate (dB)[a] |
|---|---|
| 15.00 | > -10.40 |
| 12.50 | > -9.50 |
| 10.00 | > -6.50 |
| 6.75 | > -5.20 |
| 5.00 | > -4.55 |
| 2.70 | > -3.25 |
| 0.10 | > -1.00 |

*a. Cable values are measured mated pair-to-mated pair.*

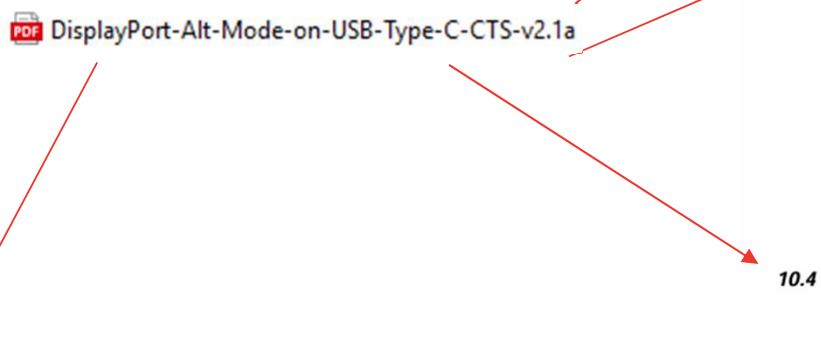
**Table 4-12: DP80 Nyquist Frequencies and their ILFitAtNq Mandates (Normative)**

| Nyquist Frequency (GHz) | ILFitAtNq Mandate (dB) | |
|---|---|---|
| | DP-to-DP[a] | USB-C-to-DP[b] |
| 15.00 | > -12.0 | > -12.25 |
| 10.00 | > -7.50 | > -8.10 |
| 6.75 | > -6.00 | > -6.20 |
| 5.00 | > -5.25 | > -5.30 |
| 2.70 | > -3.75 | > -3.80 |
| 0.10 | > -0.75 | > -1.00 |

*a. Cable values are measured mated pair-to-mated pair.*
*b. Cable values are measured plug-to-mated pair.*

# What Is Inside VESA LRD Cable CTS? Cont'

- Additional Tests Added for USB-C to DP LRD Active Cable
  - From DP Alt Mode 2.1 CTSa




10.6 *DisplayPort Alternate USB-C to DP Adapter Tests ..... 141*
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# CTS Testing Challenges

- Knowledge to get DP LRD cable to work up
  - AUX and DP_PWR Electrical setting
    - Sink devices and Source devices

1. Aux P: Pull down to GND
2. Aux N: Pull high to 2.89~3.6V.
3. DP_PWR:2.89~3.6V
4. Aux transaction if needed



1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull high to 2.25~3.6V
5. Aux transaction if needed

# CTS Testing Challenges Cont'

- Knowledge to get USB-C to DP LRD cable to work up
  - Vconn, AUX, and DP_PWR Electrical setting
    - Sink devices and Source devices

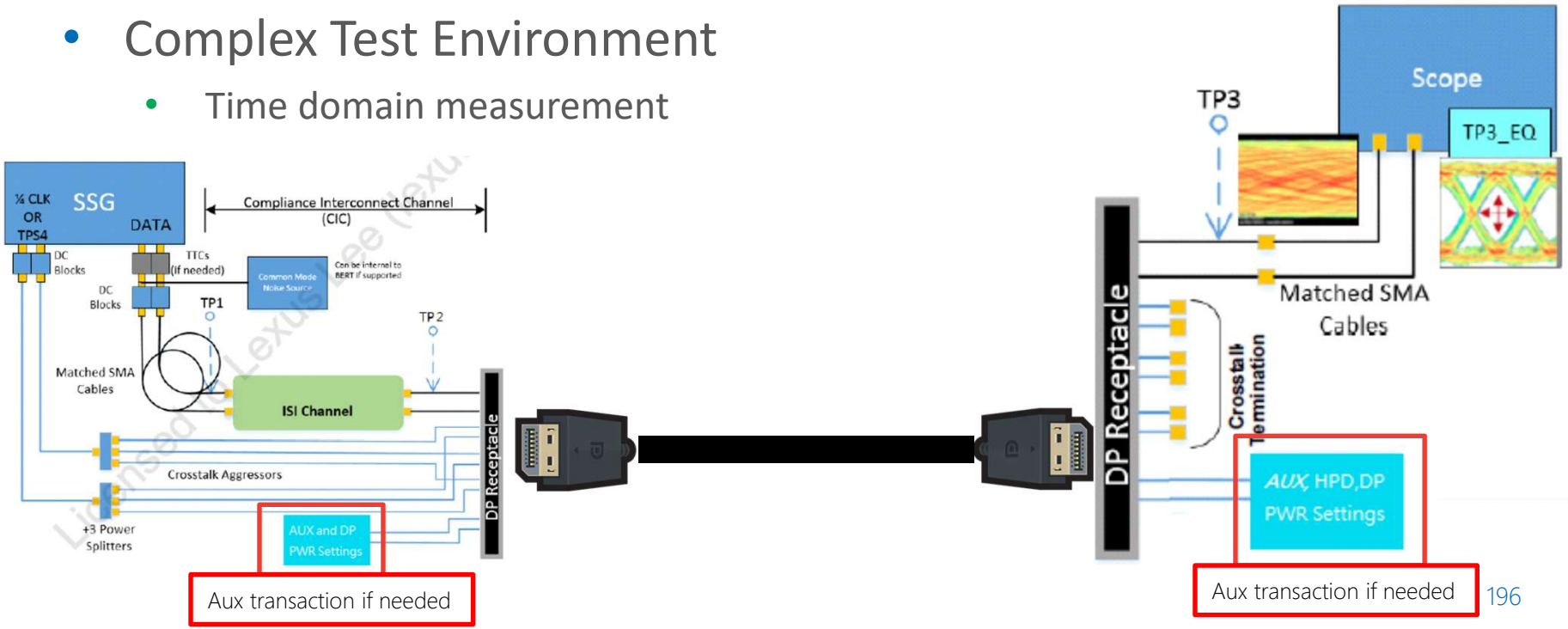
1. Vconn:3.0~5.5V
2. DP alt mode exerciser if needed.
3. Aux circuitry if needed.
4. Aux transaction if needed




1. Aux P: Pull high to 2.25~3.6V
2. Aux N: Pull down to GND.
3. DP_PWR:2.89~3.6V
4. HPD: Pull High to 2.25~3.6V
5. Aux transaction if needed

# CTS Testing Challenges Cont’

- Complex Test Environment
  - Time domain measurement



# CTS Testing Challenges Cont’

- Complex Test Environment
  - Frequency domain measurement



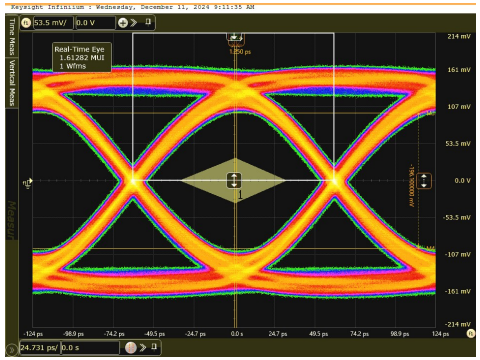
# Overview

- Why VESA Defines LRD Active Cable Spec
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA  Connector Certification Introduction
- Cable Next - Active Optical Cable?

# The Most Frequently Failed Items

- Eye Diagram
  - UHBR20 Criteria
    - TP3_EQ-Inner Eye Height: 100mV
    - TP3_EQ-Eye Width: 560mUI
    - Cannot hit the eye mask

| Preset Configuration # | Preshoot (dB) | De-emphasis (dB) |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | -1.9 |
| 2 | 0 | -3.6 |
| 3 | 0 | -5.0 |
| 4 | 0 | -8.4 |
| 5 | 0.9 | 0 |
| 6 | 1.1 | -1.9 |
| 7 | 1.4 | -3.8 |
| 8 | 1.7 | -5.8 |
| 9 | 2.1 | -8.0 |
| 10 | 1.7 | 0 |
| 11 | 2.2 | -2.2 |
| 12 | 2.5 | -3.6 |
| 13 | 3.4 | -6.7 |
| 14 | 3.6 | 0 |
| 15 | 1.7 | -1.7 |

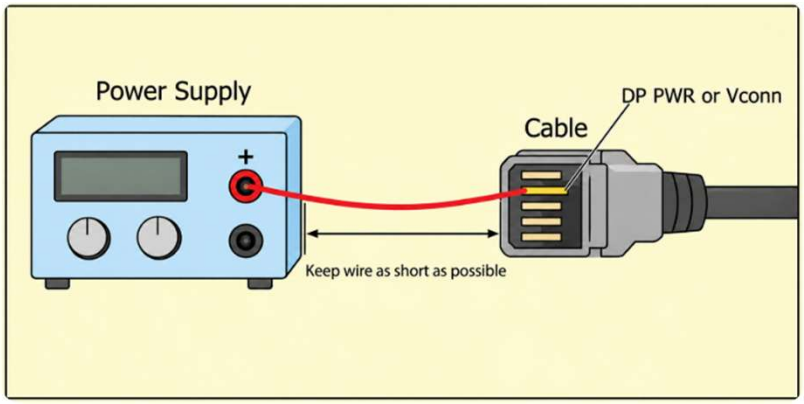



  - Requirement: Need to pass  with 3 TxFFE Presets  and average of 5 times.

  - Caused by Raw cable material quality and cable vendor manufacturing capability

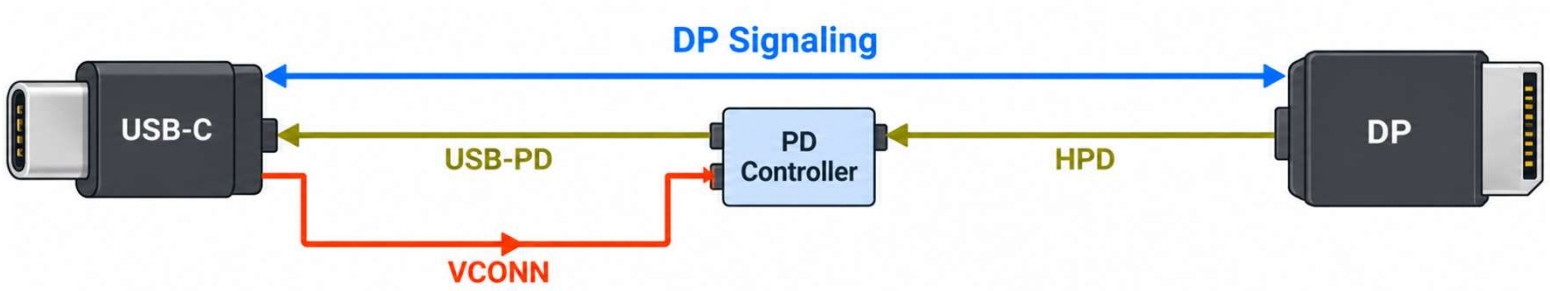
# The Most Frequently Failed Items Cont’

- The Minimal Required Voltage
  - DP PWR Range: 2.89-3.6V for DP-DP Cable
    - Voltage Range : 2.89-3.6V
    - 2.89V → Failure
  - Vconn Range for USB-C to DP Cable
    - Voltage Range: 3.0-5.5V
    - 3.0V → Failure



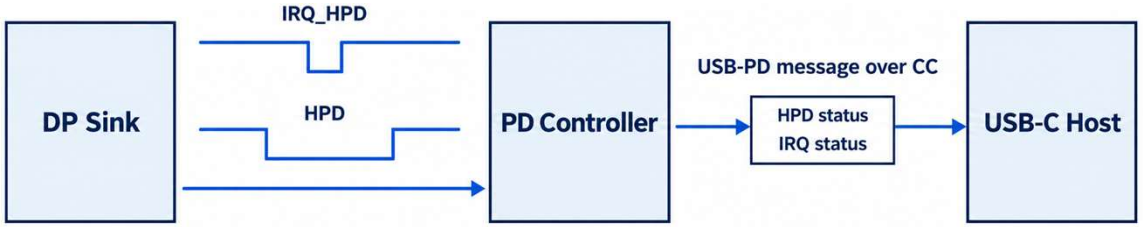
# The Most Frequently Failed Items Cont'

- USB-C to DP Cable Structure



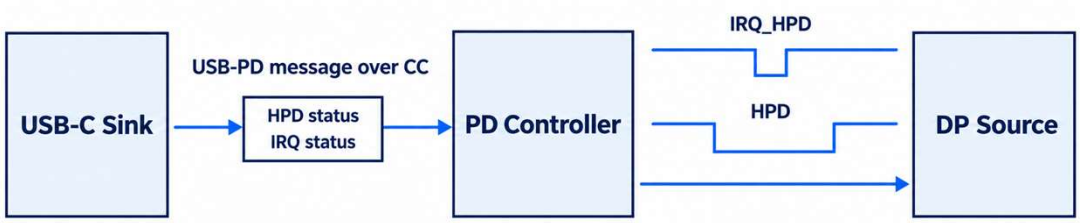
# The Most Frequently Failed Items Cont'

- HPD to PD Conversion
  - Different IRQ_HPD width
    - 2.05 to 2.1msec
    - 1.9 to 1.95msec
    - **2.60 to 270usec**
    - 230 to 240usec
  - Different HPD width
    - 5ms
    - 150ms

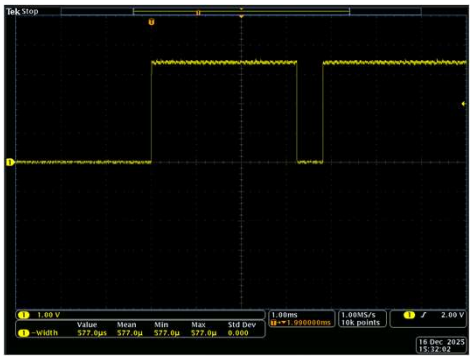


# The Most Frequently Failed Items Cont'

- PD to HPD Conversion
  - IRQ_HPD status flag is set
  - HPD_Low is set
    - HPD_High is set
  - HPD_Low is set for 100ms
  - HPD_High and IRQ_HPD are set
    - In a single message

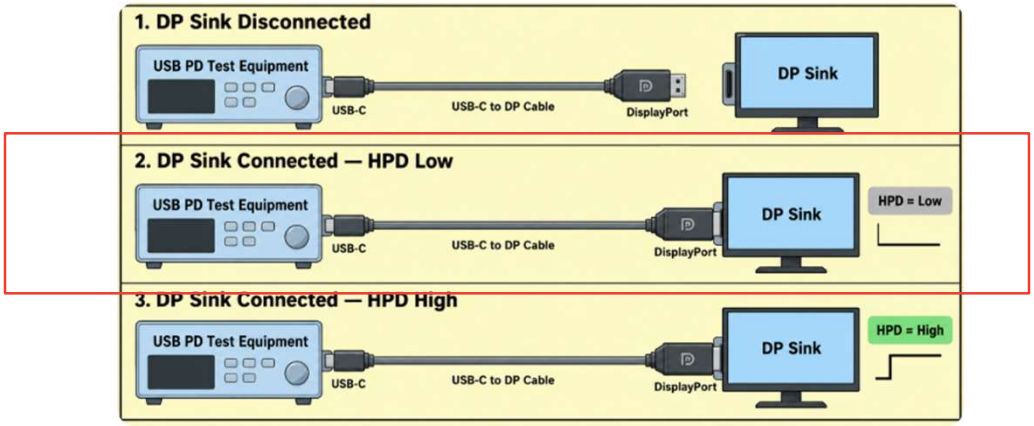




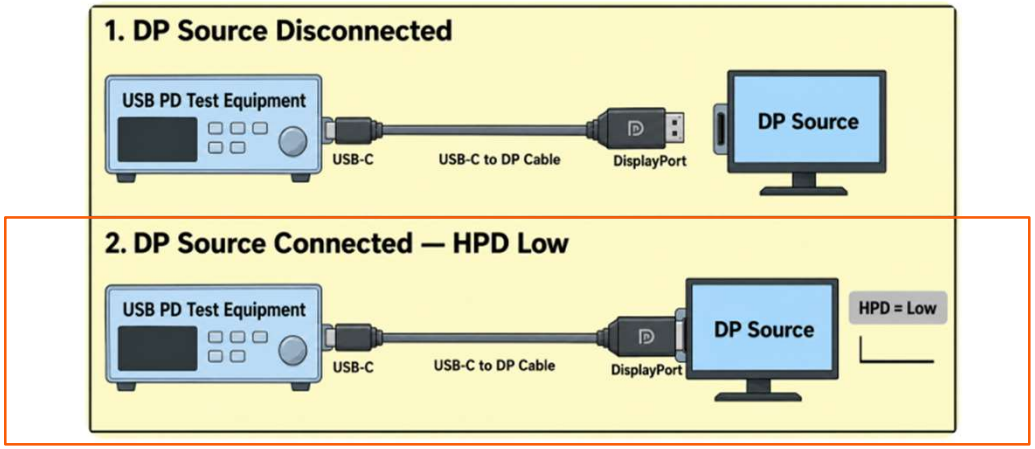
# The Most Frequently Failed Items Cont'

- Attach to DP Sink
  - 3 test cases
    - Middle one→Failure
      - Assertion of DP Sink Disconnected



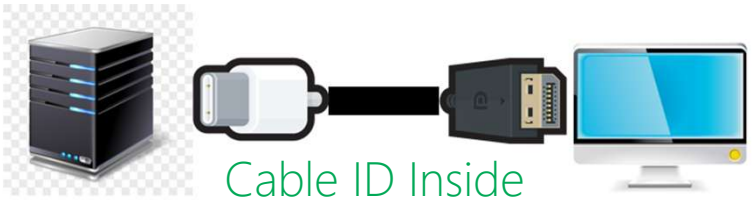
# The Most Frequently Failed Items Cont'

- Attach to DP Source
  - 2 test cases
    - Buttom one→Failure
      - Assertion of "DP Source Disconnected" when HPD is low



# The Most Frequently Failed Items Cont'

- Typical Application of Cable ID







Rx: Read Cable ID from Cable

Tx: Read Cable ID from The Cable at USB-C end

Tx: Inform Rx of Cable ID at USB-C end

Rx: Read Cable ID from Cable

Tx: Read Cable ID from Rx

# The Most Frequently Failed Items Cont'

- Cable ID at USB-C Connector
  - Rely of SOP' Discover Modes
- If UHBR20 Is Set
  - UHBR13.5 shall be set accordingly

| Bit(s) | Description | Values |
|---|---|---|
| 1:0 | **RESERVED** | RESERVED (always 00b). |
| 5:2 | **Signaling for Transport of DisplayPort Protocol**[b] | XXX1b = Supports all defined *DP* bit rates up to HBR3. XX1Xb = Supports *DP* bit rate UHBR10.<br>X1XXb = Supports *DP* bit rate of UHBR20 (e.g., 0111b supports all *DP* bit rates, including UHBR10 and UHBR20).<br>All other values are RESERVED for higher bit rates.[c] |
| 7:6 | **RESERVED** | RESERVED (always 00b). |
| 15:8 | **DP Source Device Pin Assignments Supported** | 0Ch = Pin Assignments C and D are supported.<br>10h = *USB-C* and *DP* connector Pin Assignment E is supported.<br>All other values are RESERVED. |
| 23:16 | **DP Sink Device Pin Assignments Supported** | 0Ch = Pin Assignments C and D are supported (USB-C-to-USB-C cable).<br>10h = *USB-C* and *DP* connector Pin Assignment E is supported.<br>All other values are RESERVED. |
| 25:24 | **RESERVED** | RESERVED (always 00b). |
| 26[d] | **UHBR13.5** | 0 = UHBR13.5 is not supported.<br>1 = UHBR13.5 is supported.[e] |
| 27 | **RESERVED** | RESERVED (always 0). |
| 29:28[d] | **Active Component** | 00b = Passive.<br>01b = Active re-timer. 10b = Active re-driver.<br>11b = Optical. |
| 31:30 | **DPAM Version** | 00b = Version 2.0 or earlier.<br>01b = Version 2.1 or higher. |

# Overview

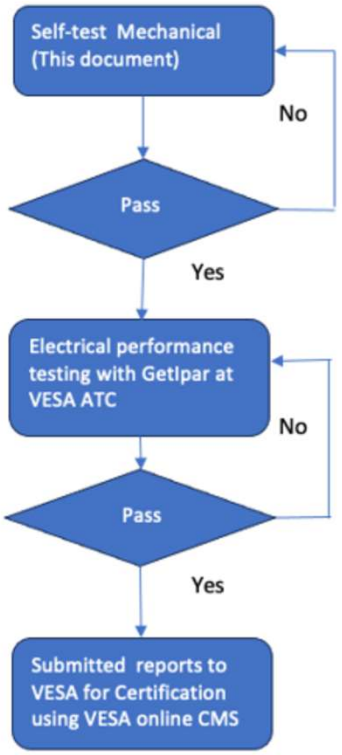
- Why VESA Defines LRD Active Cable Spec
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA  Connector Certification Introduction
- Cable Next - Active Optical Cable?

# DP Connector Certification Status

- Connector certification
  - Legacy Connector(HBR2 and below)
    - Has been phased out from end of 2025
  - DP8K & Enhanced Connector
    - Self-test Mechanical

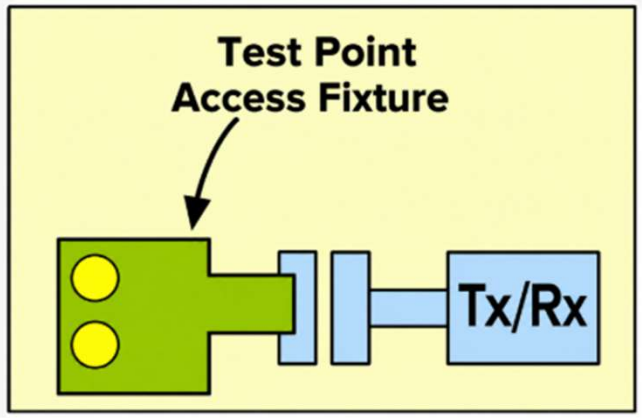
**VESA® DisplayPort™ Self-Test Report for Connectors v2.1**

**VESA® DisplayPort™ Self-Test Report for DP Connectors Supporting HBR3 Link Rate and DP8K Cables**



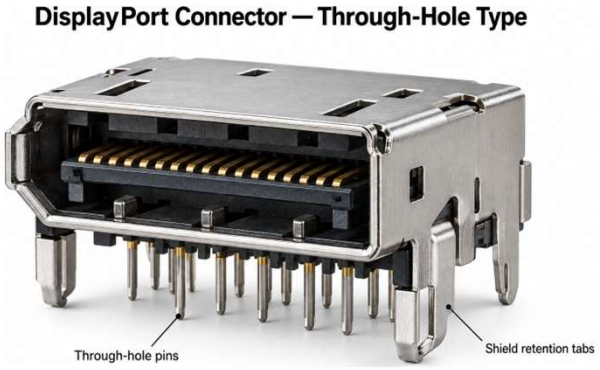
# DP Connector Certification Status Cont'

- Enhanced DP Connector (DIP Type)
  - Possibly causing Sink/Source Return Loss test to fail
    - Even if it is a certified EnDP connector
    - Test method different between Connector and Sink/Source in CTS









# Overview

- Why VESA Defines LRD Active Cable Standard
- VESA LRD Active Cable Testing Challenges
- VESA LRD Active Cable Testing Experience
- VESA  Connector Certification Introduction
- Cable Next - Active Optical Cable?

# Active Optical Cable

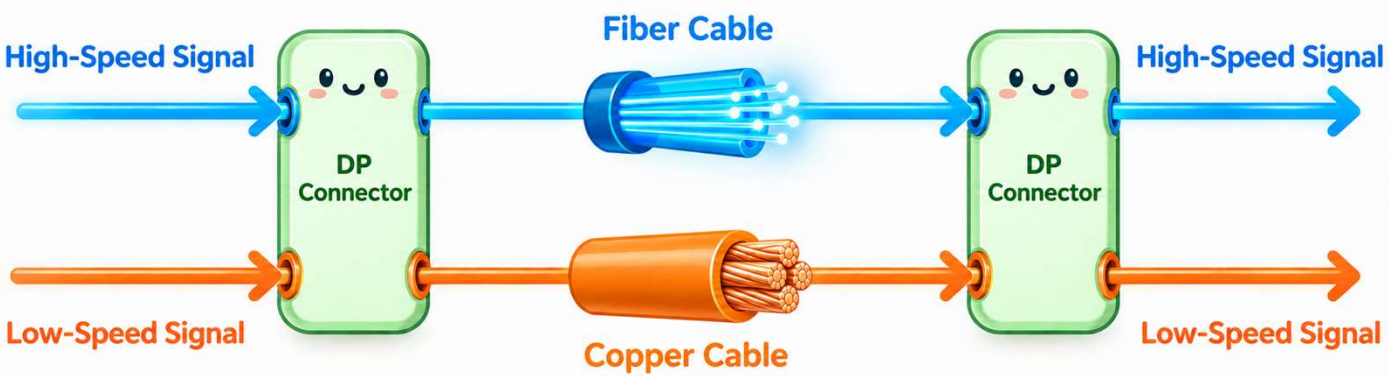
- Definition of DPCD  02217h and 00110h
  - Will add optical cable type in Bit 5:3 Cable Type field: 100b = Optical cable

| | | |
|---|---|---|
| | 5:3 | **Cable Type**<br>000b = Cable type is unknown (default; a DPRX device with a DP receptacle connector shall keep this value).<br>001b = Passive cable.<br>010b = LRD cable.<br>011b = LTTPR re-timer active cable.<br>All other values are RESERVED. |
| | 7:6 | **RESERVED** |

Licensed to

# Active Optical Cable Cont'

- The Optical Cable's Structure
  - Fiber used for Main-Link channels (High-Speed Data)
  - Copper used for Non-Main-Link channels



# Active Optical Cable Cont'

- Allion has been verifying AOC performance
  - Equalization Setting on Each Lane
    - USB-C to USB-C Ends
      - Could be different due to the loss different definition between DP and USB specs while in Pin Assignment D Mode
    - USB-C to DP/mDP Ends and DP/mDP to DP/mDP Ends
      - Should be the same or be closer.
  - Creating PHY test proposal
    - Test items Include common items like Jitter/Eye/SSC/Skew
    - More focus on "Stressed Signal Condition" verification for TP3/TP3_EQ Eye




# Thank you

VESA

# Design Considerations for USB-C Products

**Abel Astley**
Unigraf
*October 2026*

# Design Considerations for USB-C



==



# Design Considerations for USB-C

## Agenda

- **Back to Basics**: Sources, Sinks, and how they interoperate
- **Common Mistakes** and how to avoid them
- **Factory Testing** Challenges and Solutions
- **Recent Updates** to DP Alt Mode
- **USB4** and how it fits in

# Back to Basics
## Vocabulary

# Back to Basics: Vocabulary

- From *USB Type-C® Cable and Connector Specification*, Rev 2.5 (March 2026)

| | |
|---|---|
| Source | Port asserting ***Rp*** on CC and when attached is providing power over VBUS; most commonly a Host or Hub DFP. |
| Sink | Port asserting ***Rd*** on CC and when attached is consuming power from VBUS; most commonly a Device. |

- In USB Speak, ***Source*** and ***Sink*** refer to a device's ***power role***, not its video role
- Where possible, this presentation will explicitly state which role is being referenced

# Back to Basics: Vocabulary

| | |
|---|---|
| DFP | Downstream Facing Port, specifically associated with the flow of data in a USB connection. Typically, the ports on a host or the ports on a hub to which devices are connected. In its initial state, the DFP sources VBUS and VCONN, and supports data. A charge-only DFP port only sources VBUS. |
| UFP | Upstream Facing Port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks VBUS and supports data. |
| DRD (Dual-Role-Data) | The acronym used in this specification to refer to a USB port that can operate as either a DFP (Host) or UFP (Device). The role that the port initially takes is determined by the port's power role at attach. A Source port takes on the data role of a DFP and a Sink port takes on the data role of a UFP. The port's data role ***may*** be changed dynamically using ***USB PD*** Data Role Swap. |
| DRP (Dual-Role-Power) | The acronym used in this specification to refer to a USB port that can operate as either a Source or a Sink. The role that the port offers ***may*** be fixed to either a Source or Sink or ***may*** alternate between the two port states. Initially when operating as a Source, the port will also take on the data role of a DFP and when operating as a Sink, the port will also take on the data role of a UFP. The port's power role ***may*** be changed dynamically using ***USB PD*** Power Role Swap. |

# Common Mistakes

## The importance of Rd

# Back to Basics



**Figure 4-5 Pull-Up/Pull-Down CC Model**

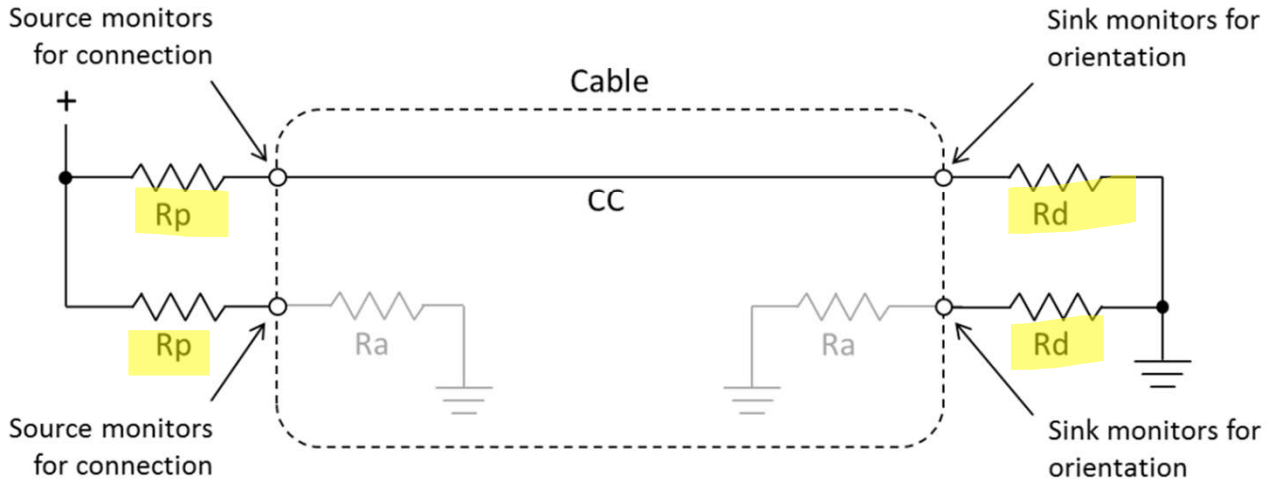



**Figure 4-6 Current Source/Pull-Down CC Model**

# The importance of Rd



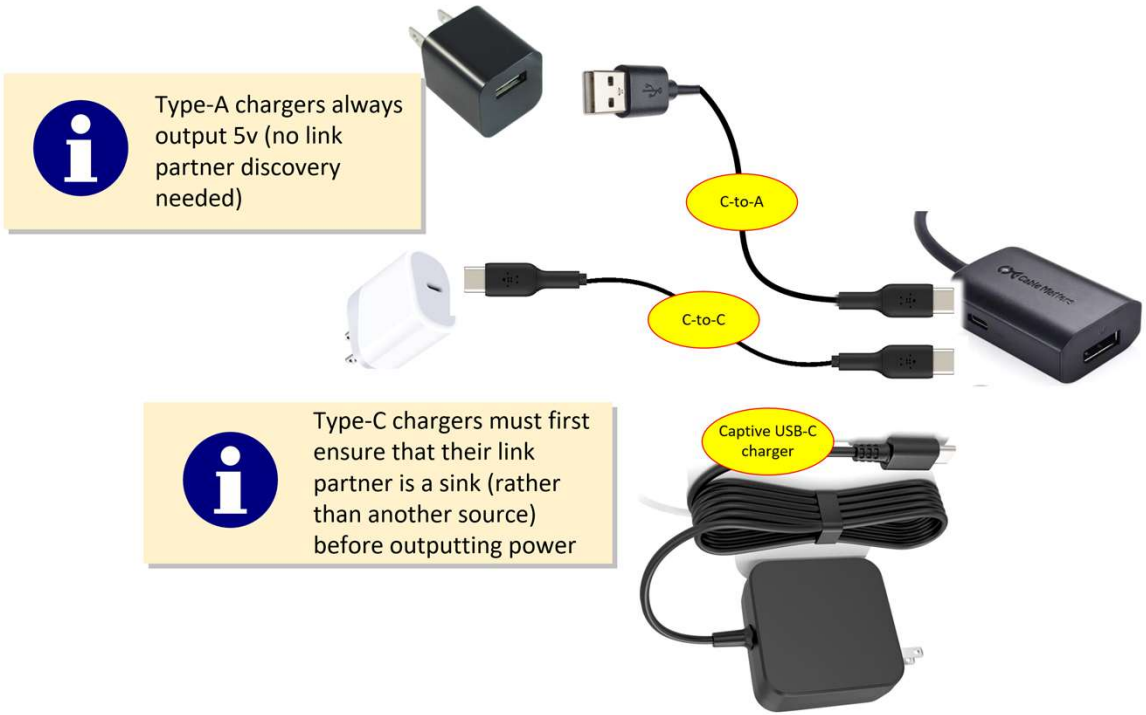
# The importance of Rd




- User may connect any of these charger types to the charge-through port

# The importance of Rd

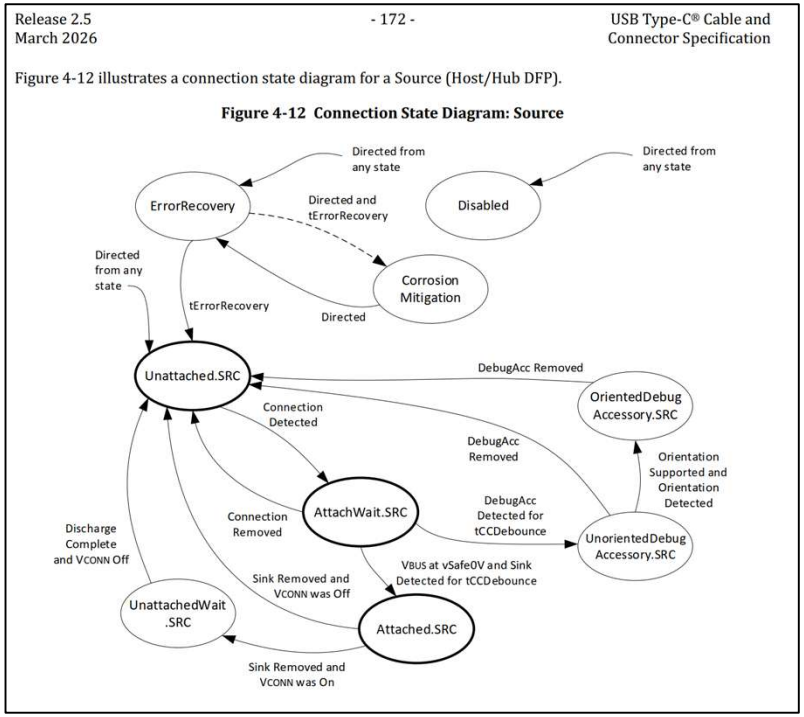
- User may connect any of these charger types to the charge-through port



# The importance of Rd

- From *USB Type-C® Cable and Connector Specification*, Rev 2.5 (March 2026)

- **Key point: if a USB-C Charger doesn't see Rd, it will *not* enable its output**



Takeaway:

**USB-C ports should be designed to work with C-to-C cables as well as C-to-legacy adaptors**

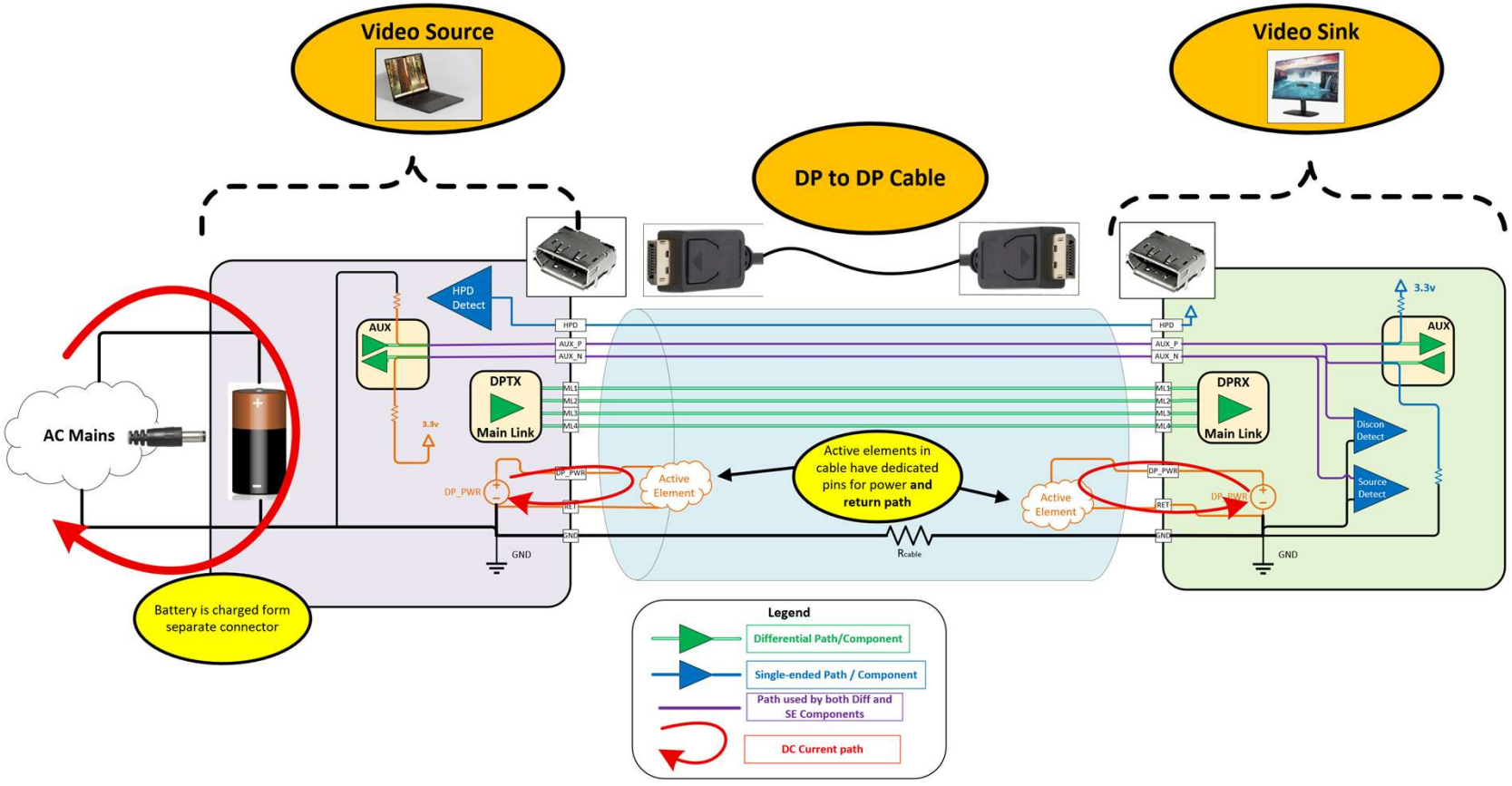
# Common Mistakes

## The Impact of Ground Current

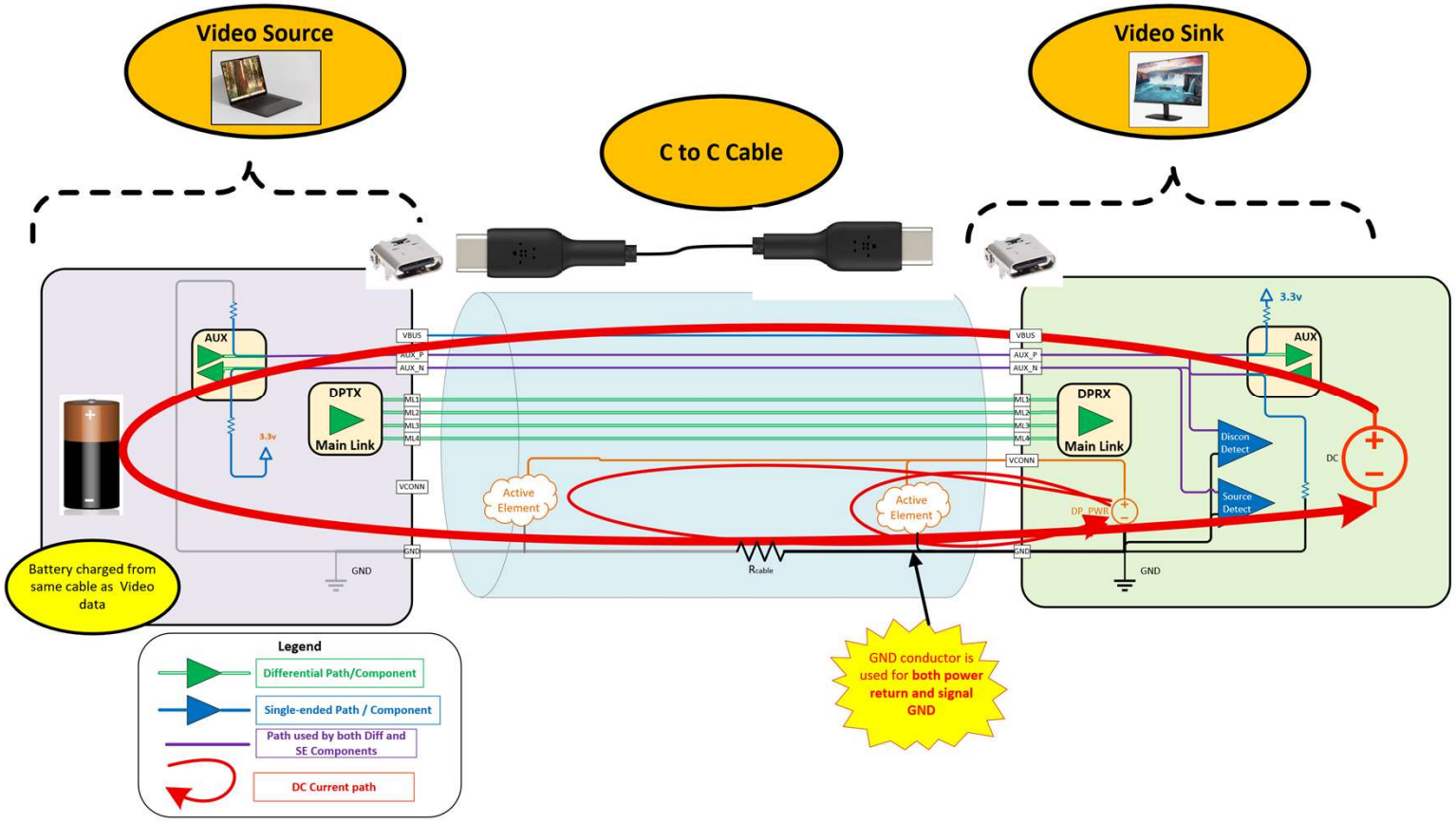
# Ground Current

- ***Ground Current*** refers to current flowing through the cable GND conductors
- For Native DP, the Ground Current should be **close to zero**
- For USB-C, the Ground Current can be **5 amps in either direction**, and can **change dynamically**

# Native DP Link



# USB-C Link


Video Source
C to C Cable
Video Sink
AUX
DPTX
Main Link
3.3v
VBUS
AUX_P
AUX_N
ML1
ML2
ML3
ML4
VCONN
GND
Active Element
Active Element
Rcable
DPRX
Main Link
Discon Detect
Source Detect
DP_PWR
DC
Battery charged from same cable as Video data
GND conductor is used for both power return and signal GND
Legend
Differential Path/Component
Single-ended Path / Component
Path used by both Diff and SE Components
DC Current path

# Notes on Ground Current

- Bad/old cable will increase effect
- Usually can't fix in fw
- From *Universal Serial Bus Power Delivery Specification*, Release 3.2, Version 1.2, May 20, 2026:

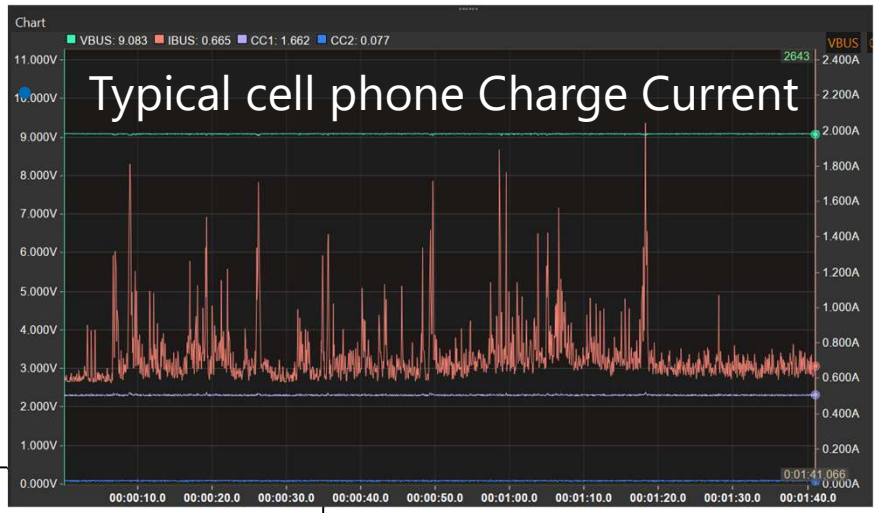



**Table 4.7. Sink Electrical Parameters**

| Parameter Name | Min Value | Nom Value | Max Value | Unit | Description |
|---|---|---|---|---|---|
| cSnkBulk | | | See [USB3] | | Sink bulk capacitance on VBUS at Attach and during FRS after the Initial Source stops sourcing and prior to establishing the First Explicit Contract. |
| cSnkBulkPd | | | 100 | µF | Bulk Capacitance that a Sink is allowed to present on VBUS after a successful Negotiation. |
| iLoadReleaseRate | -150 | | | mA/ µs | Load release di/dt. |
| iLoadStepRate | | | 150 | mA/ µs | Load step di/dt. |
| iPpsCLLoadStep | -500 | | 500 | mA | Maximum Current set-point change while operating in CL Mode. |

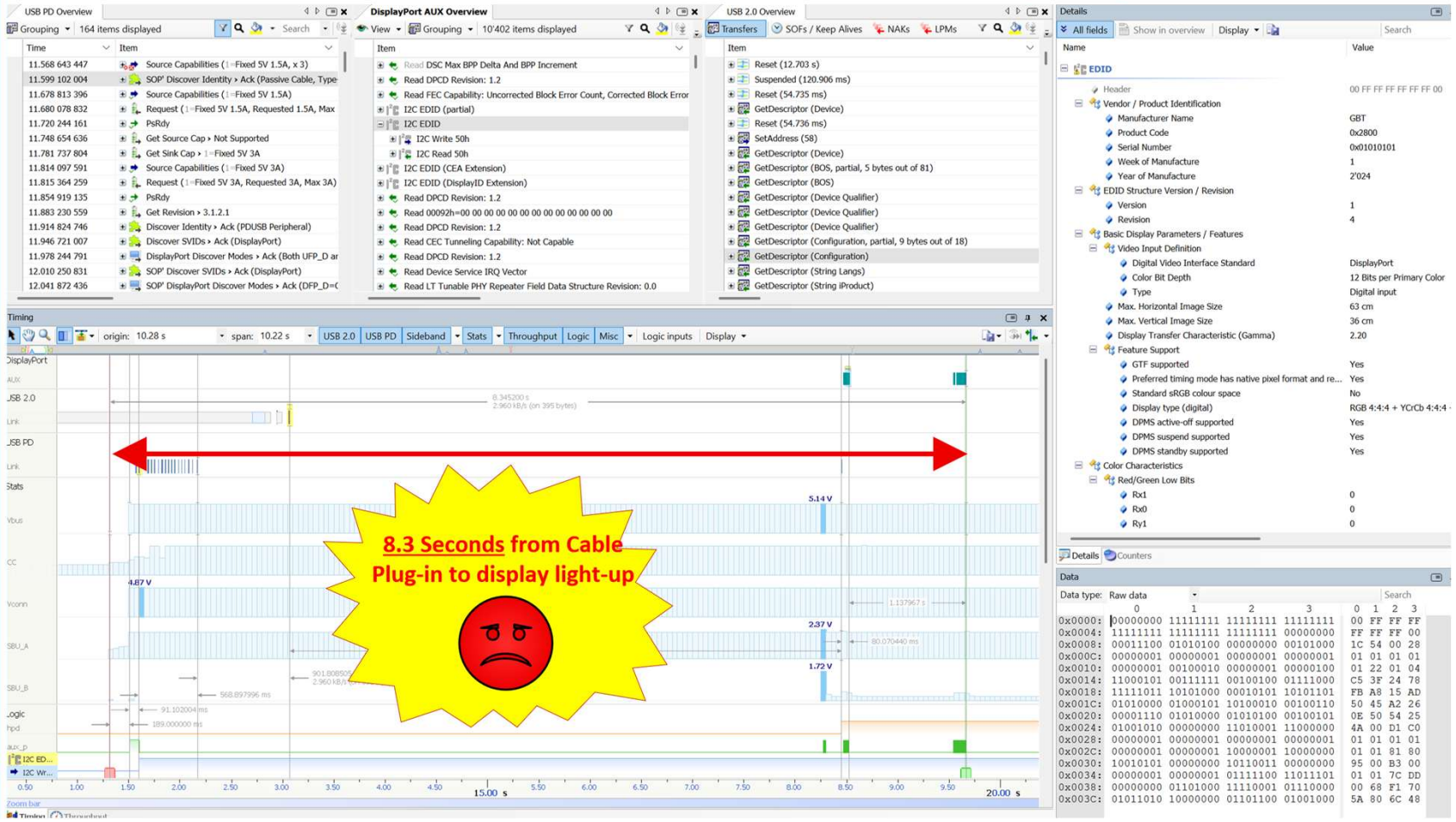
# Common Mistakes

## Delay from Cable plug-in to display light-up

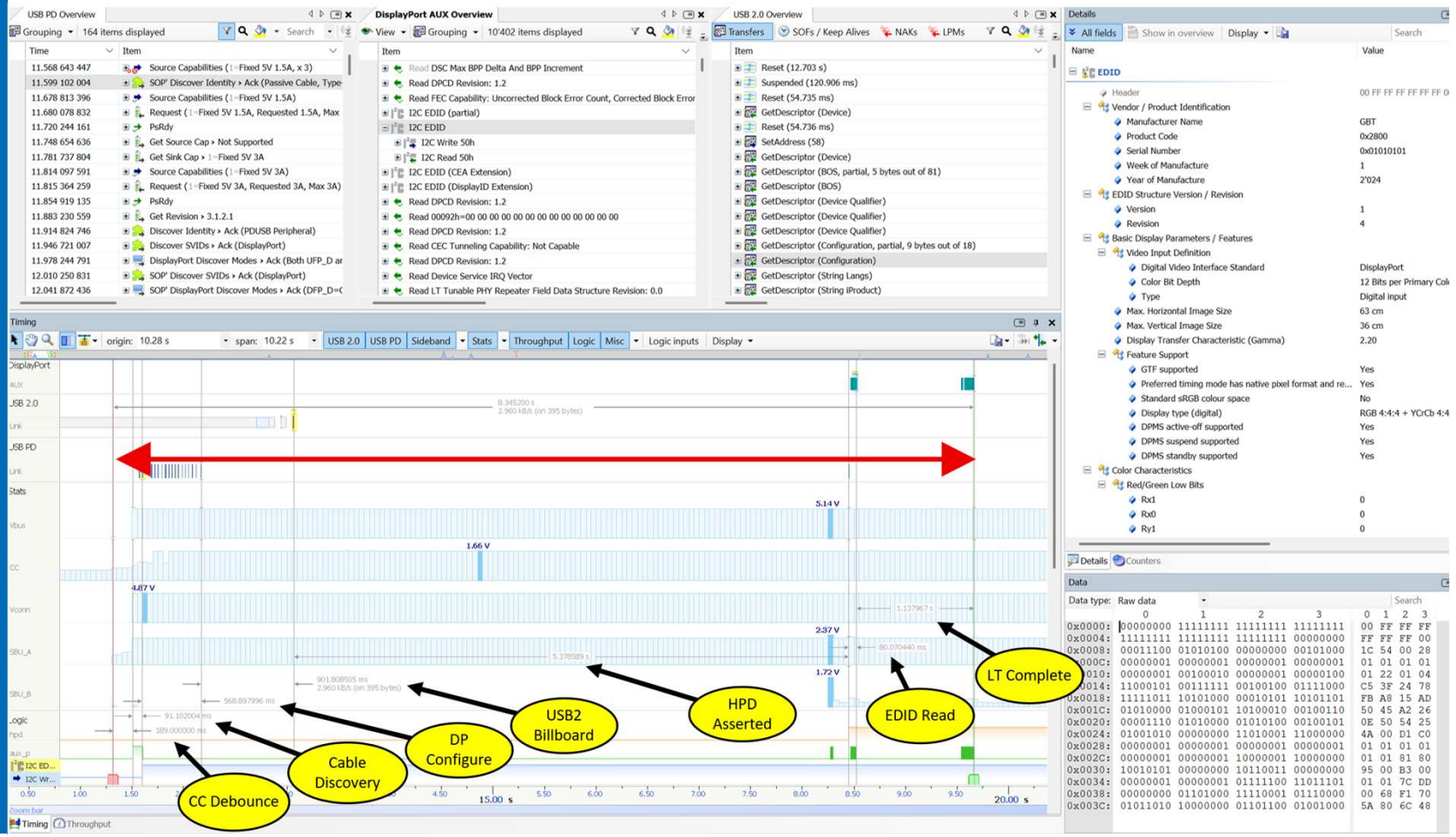
# Common Mistakes: Display light-up delay

- USB-C/PD and DP subsystems are usually developed by **different engineering teams**
- There is **no standardized interface** for passing info/events between PD and DP
- This sometimes leads to **sub-optimal behavior**, such as delay on initial plug-in

# Common Mistakes: Display light-up delay



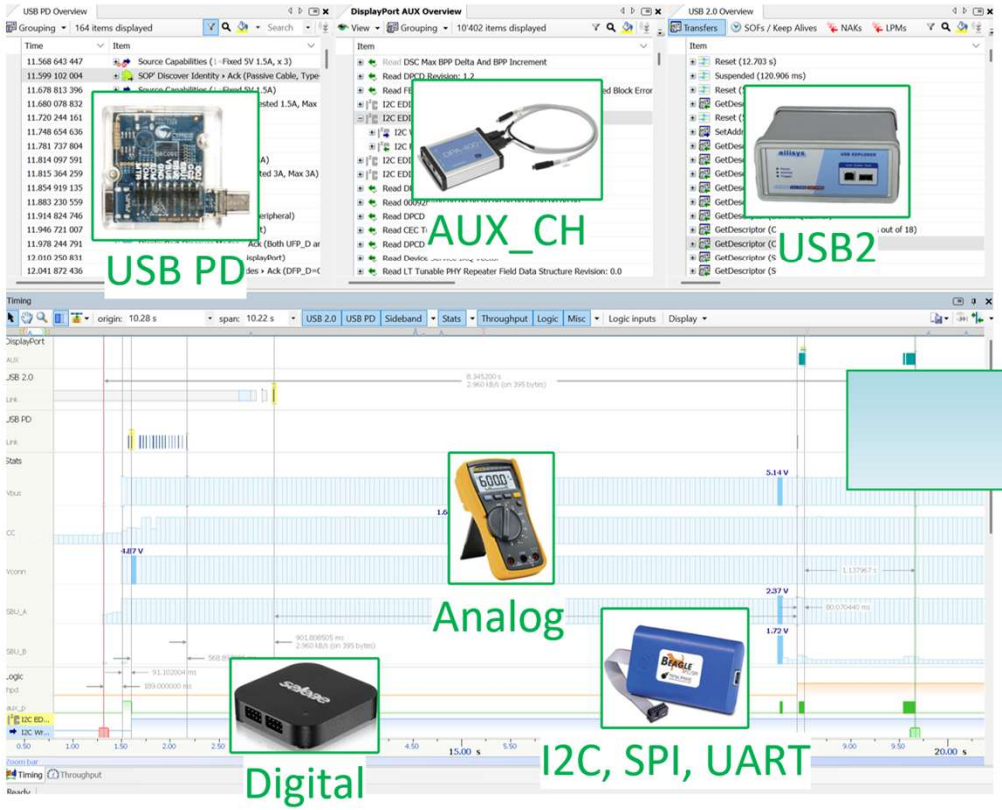
# Common Mistakes: Display light-up delay



Takeaway:

**Be sure your equipment can capture and decode all relevant data on the USB-C interface**

# Ellisys C-Tracker






# Factory Testing

## Considerations for improving accuracy in production line test environments

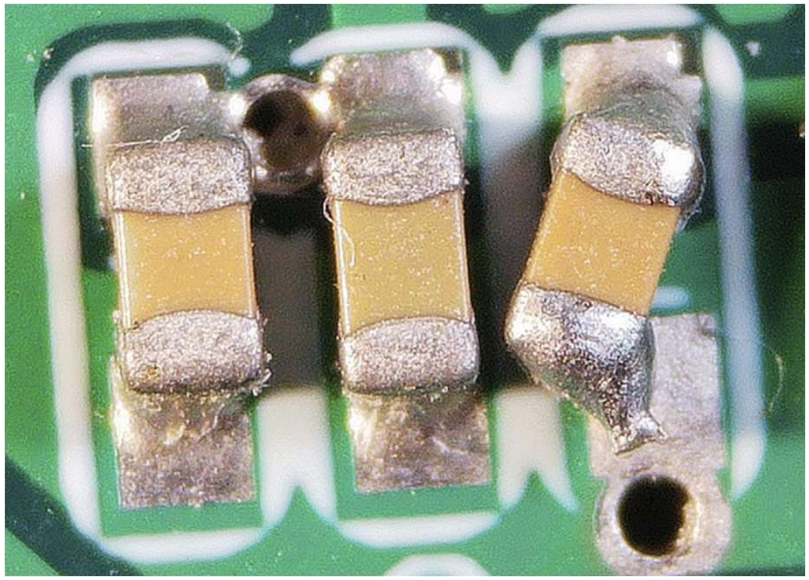
# Factory Testing: Definitions

***False Pass:*** when a defective product erroneously passes (even though it should have failed)

***DPPM:*** Defective Parts Per Million

# Factory Testing Basics

- Purpose: Detect manufacturing defects, such as **cold solder joint** or **misaligned component**



# Factory Testing: Why it matters

2022 RECALL

## HYPER

**Stackable GaN USB-C Chargers**



**65W / 100W**

OVERHEATING

Product design issue identified
Potential fire hazard
Approx. three confirmed incidents

**Design and thermal risks can trigger a market recall.**

Ref : https://reurl.cc/k9gGYn

OCT 2024 RECALL

## ANKER

**Portable Charging Power Banks**




**≈ 2,100 units**

FIRE & BURN HAZARD

Lithium-ion batteries could overheat
28 reported incidents
Two reported burn injuries

**Charging products require robust safety validation.**

Ref : https://reurl.cc/dOAKjy

NOV 2023 RECALL

## BELKIN

**BoostCharge Pro Power Bank 10K**



**≈ 83,500 units**

FIRE HAZARD

Lithium-ion battery could overheat
One reported product fire
House fire with property damage

**A field failure can affect safety and customer trust.**

Ref : https://reurl.cc/dOAKkg

**A product recall can cost far more than investing in proper validation.**

# Factory Testing Basics

- For USB-C connector testing, it is critical that **all pins are connected**, and **none of them are shorted**

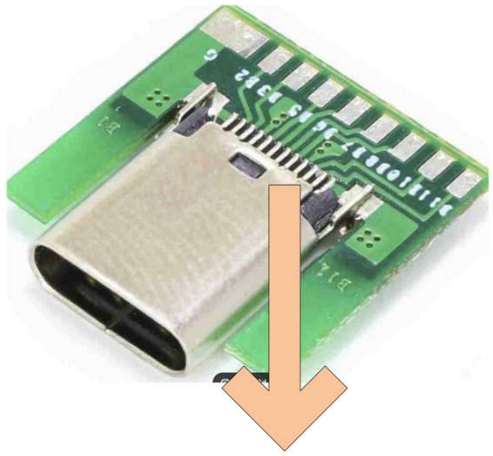
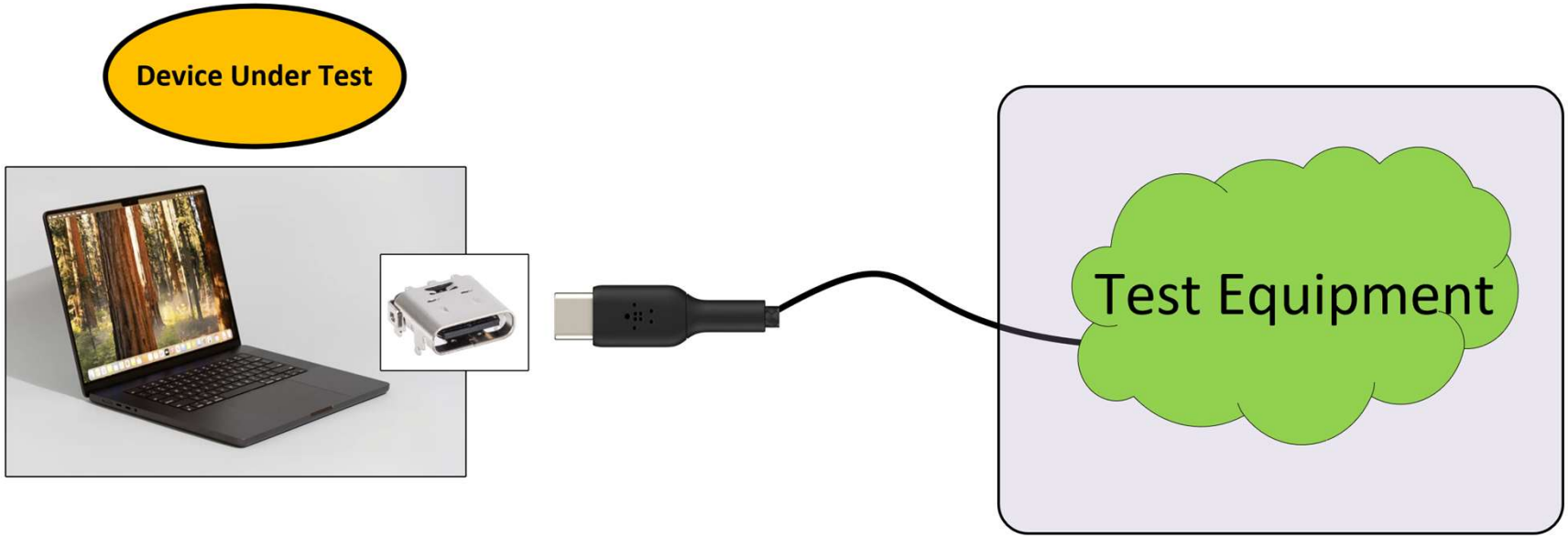


Figure 2-1 USB Type-C Receptacle Interface (Front View)

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | TX1+ | TX1− | VBUS | CC1 | D+ | D− | SBU1 | VBUS | RX2− | RX2+ | GND |
| | | | | | | | | | | | |
| GND | RX1+ | RX1− | VBUS | SBU2 | D− | D+ | CC2 | VBUS | TX2− | TX2+ | GND |
| B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |

# Factory Test Setup



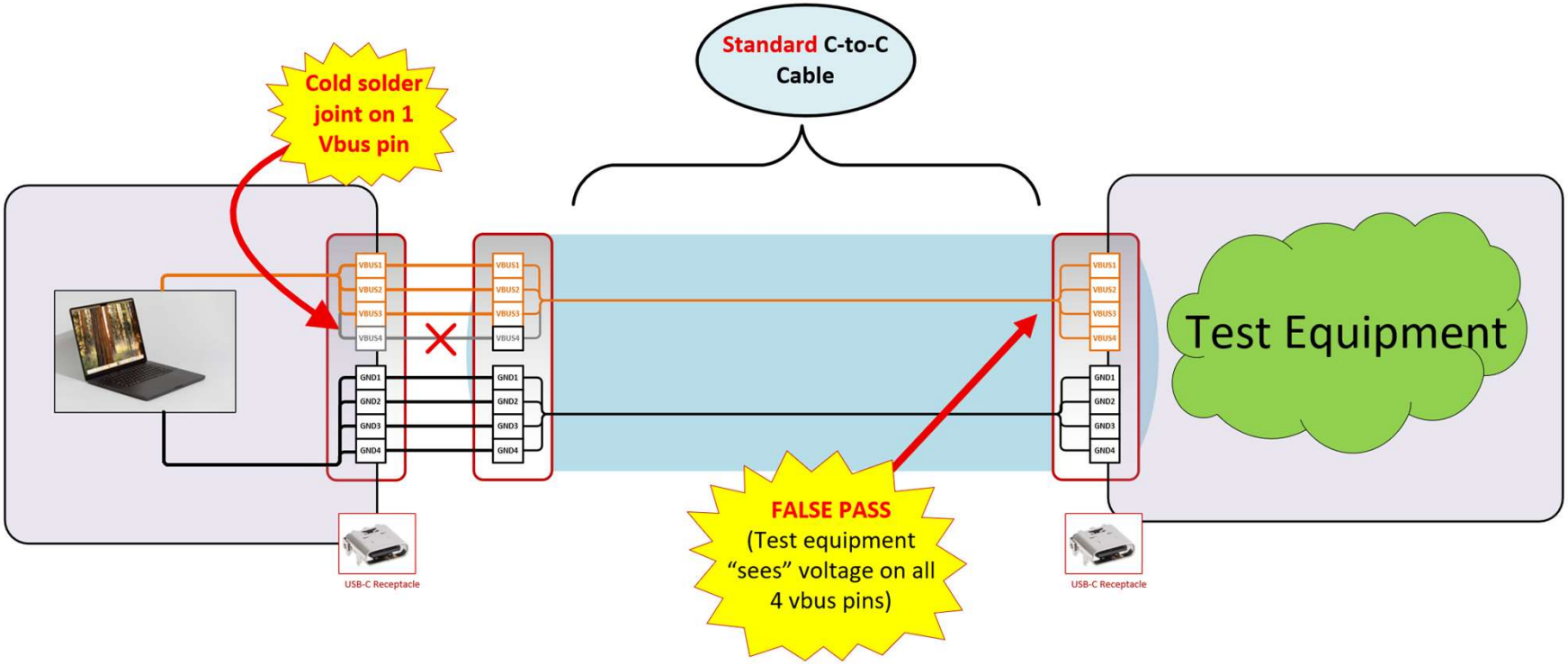
# Factory Test Example: Defect on Vbus

- Question: What happens if one (and only one) of the VBUS pins is not making proper contact?

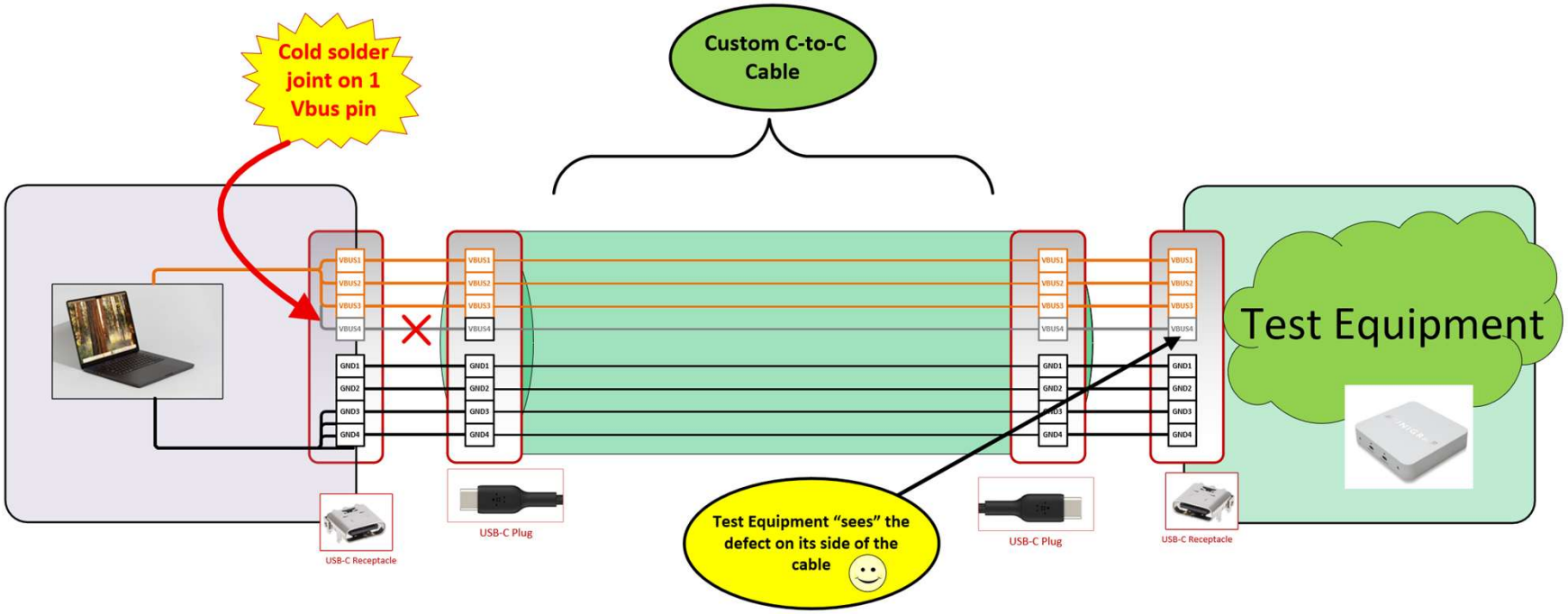
**Figure 2-1 USB Type-C Receptacle Interface (Front View)**

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | TX1+ | TX1− | VBUS | CC1 | D+ | D− | SBU1 | VBUS | RX2− | RX2+ | GND |
| GND | RX1+ | RX1− | VBUS | SBU2 | D− | D+ | CC2 | VBUS | TX2− | TX2+ | GND |
| B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |

# Factory Test Example: Defect on Vbus



# Factory Test Example: Defect on Vbus



# Factory Test Example: Defect on Vbus

**Takeaway:**

To detect a **single-pin defect** on ***Vbus*** or ***GND***, the test equipment must have **independent visibility** of all 8 of these pins (4 vbus and 4 gnd).

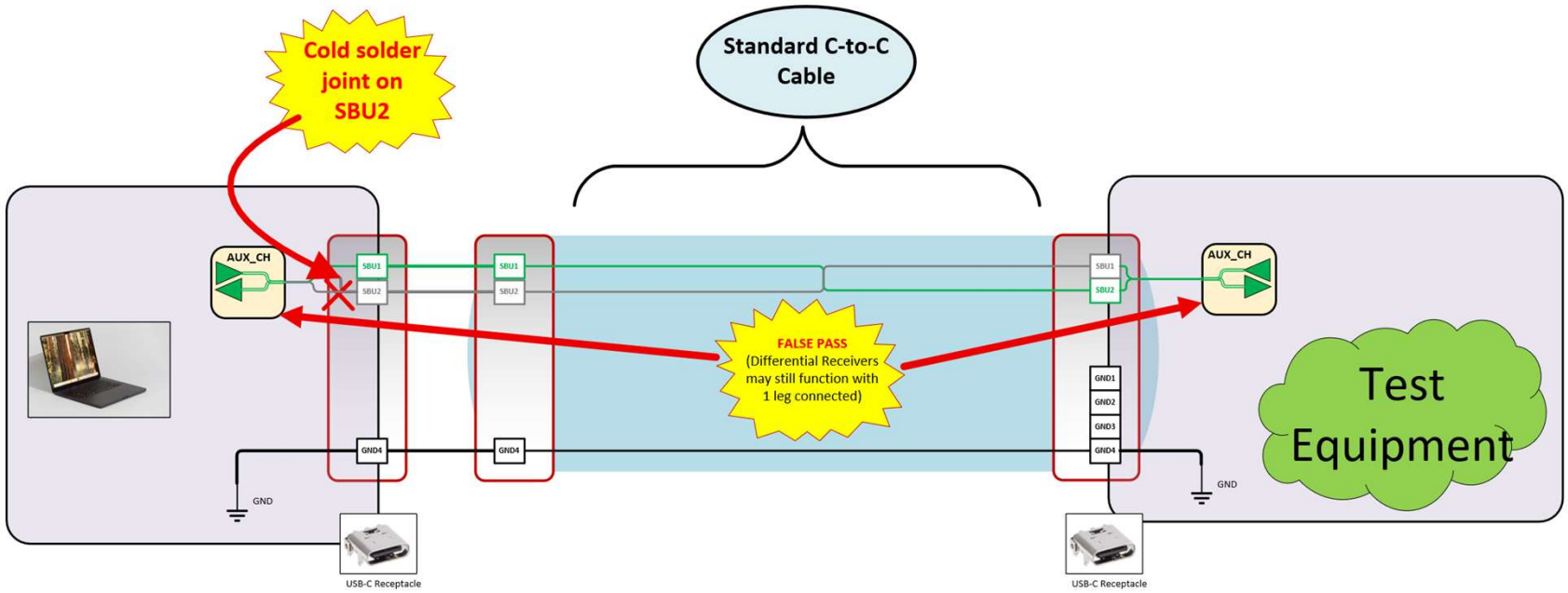
# Factory Test Example: Defect on SBU

- Question: What happens if one (and only one) of the **SBU** pins is not making proper contact?

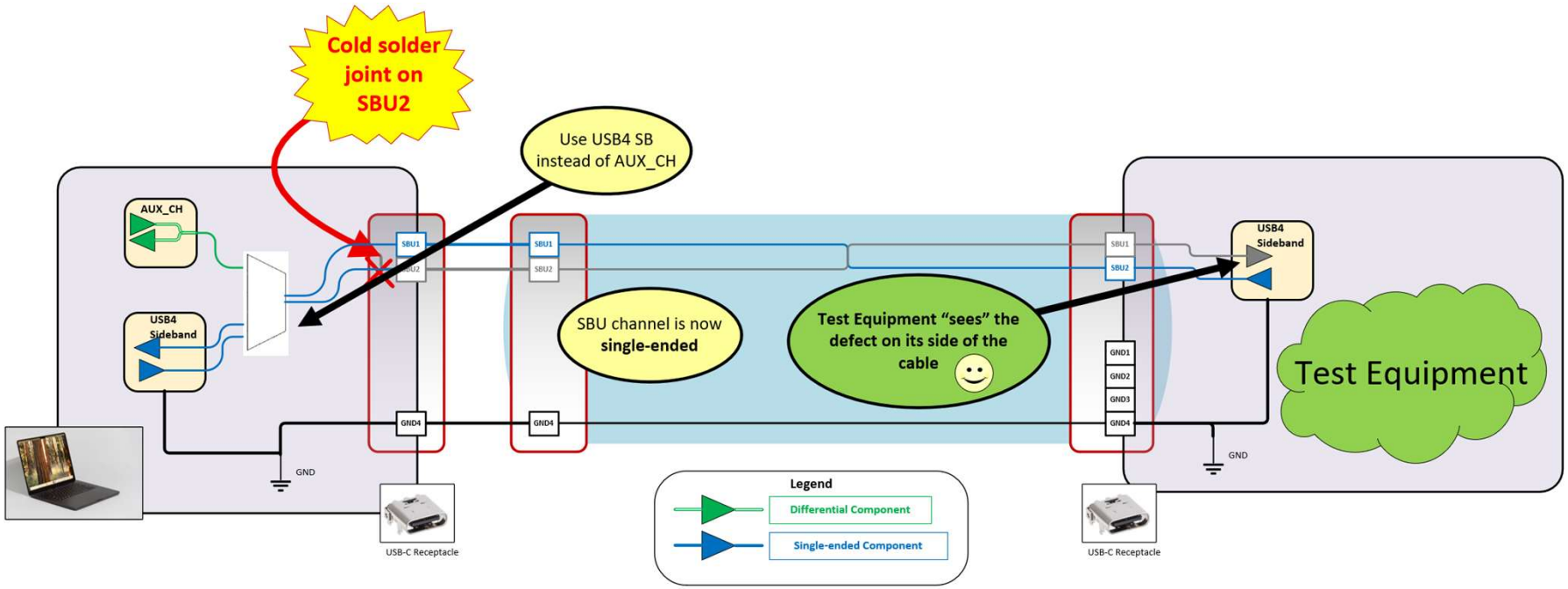
**Figure 2-1 USB Type-C Receptacle Interface (Front View)**

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | TX1+ | TX1− | VBUS | CC1 | D+ | D− | SBU1 | VBUS | RX2− | RX2+ | GND |
| | | | | | | | | | | | |
| GND | RX1+ | RX1− | VBUS | SBU2 | D− | D+ | CC2 | VBUS | TX2− | TX2+ | GND |
| B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |

# Factory Test Example: Defect on SBU



# Factory Test Example: Defect on SBU



# Factory Test Example: Defect on SBU

**Takeaway:**

The most reliable way to detect **single-pin defects** on ***SBU*** is to configure these pins for a **single-ended application** (for example, USB4)

# Factory Test

- Question: What about the other pins??

**Figure 2-1 USB Type-C Receptacle Interface (Front View)**

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | TX1+ | TX1− | VBUS | CC1 | D+ | D− | SBU1 | VBUS | RX2− | RX2+ | GND |
| GND | RX1+ | RX1− | VBUS | SBU2 | D− | D+ | CC2 | VBUS | TX2− | TX2+ | GND |
| B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |

# Factory Testing: Unigraf UTC-274

- ✓ **Purpose-built** for production environments
- ✓ Reliably detects **single-pin defects** on **all 24** USB-C pins
- ✓ Cost-effective for **large-scale deployments**
- ✓ Automatable



# Recent Updates

## Noteworthy changes to *USB PD* and *DisplayPort Alternate Mode* Specifications

# DPAM Suspend

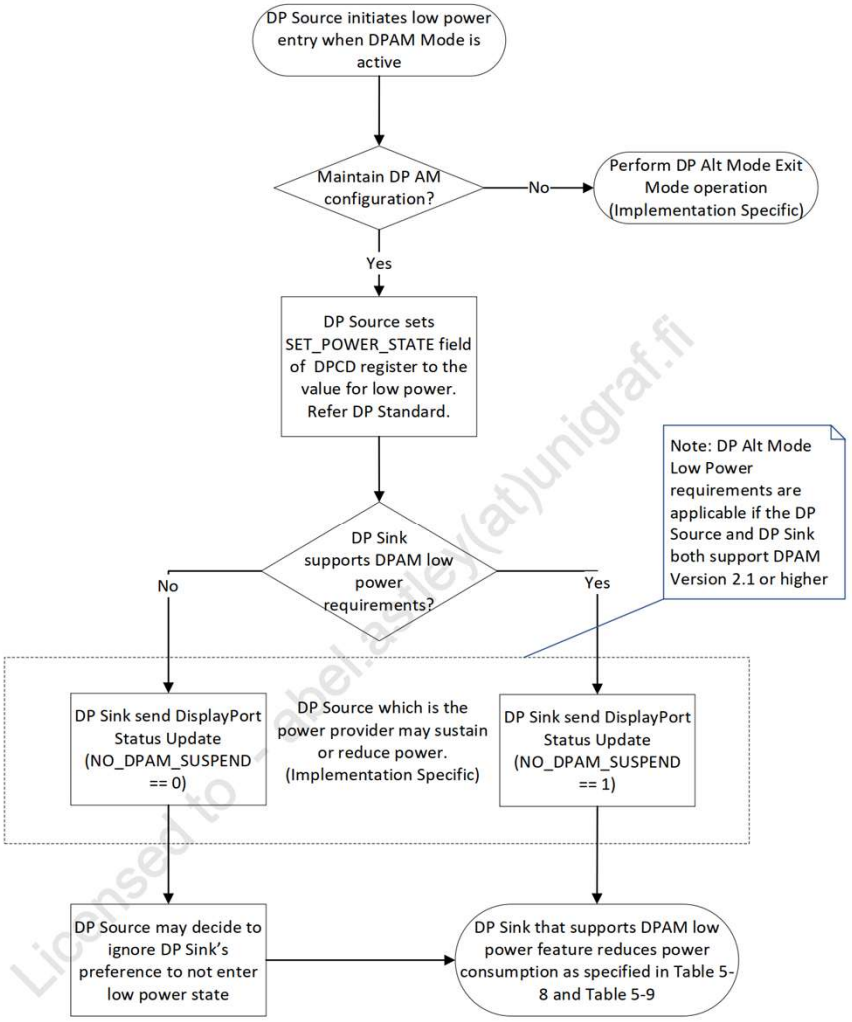


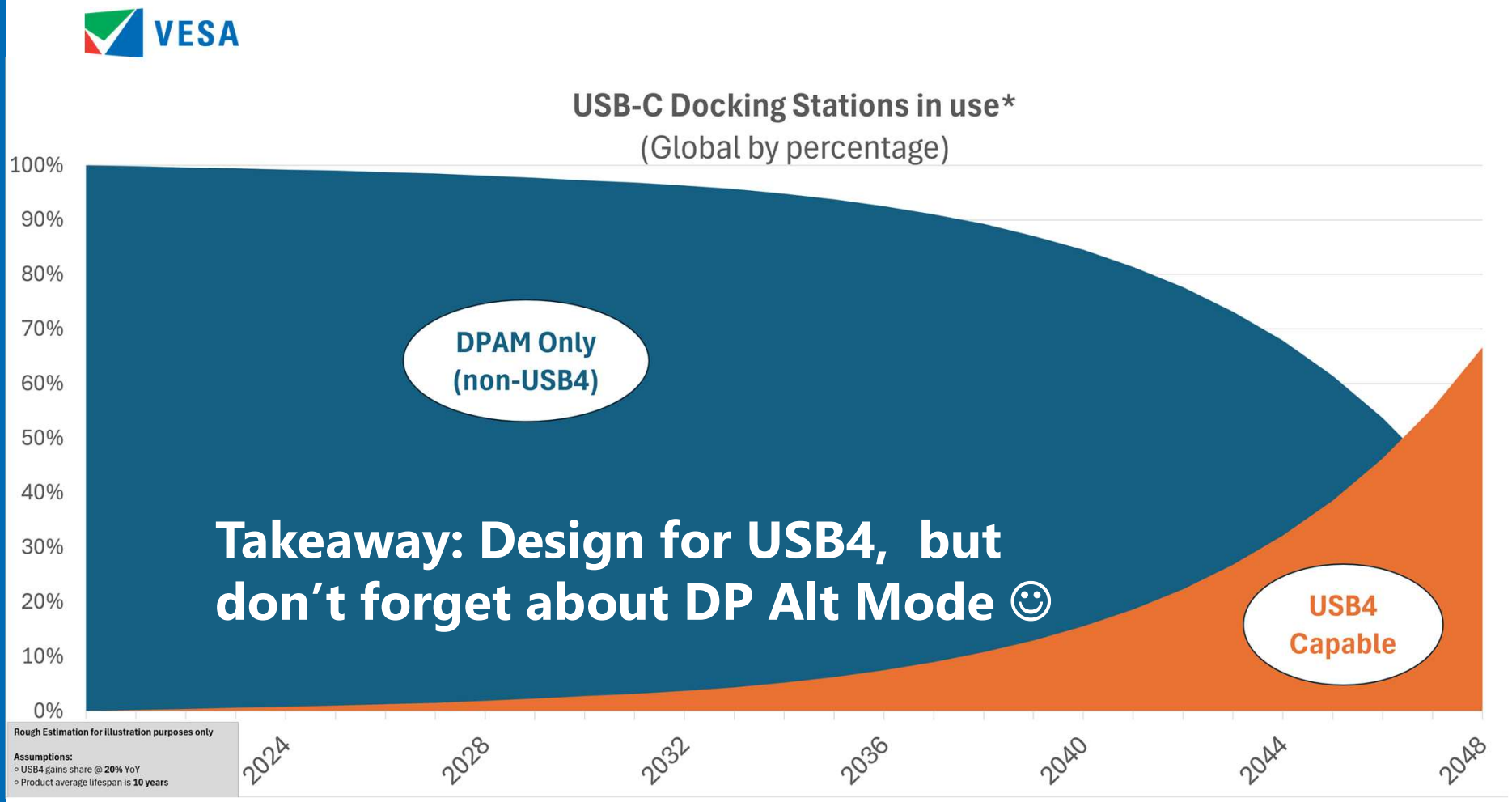

**Figure 6-1: High-level example DP Alt Mode low power flow with a bus powered UFP_U/DP Sink**

# Recent Updates: *Source Type Power Rules*

- Currently, USB-C ports on laptops are (basically) limited to 5v output due to strict rules regarding PD power sources

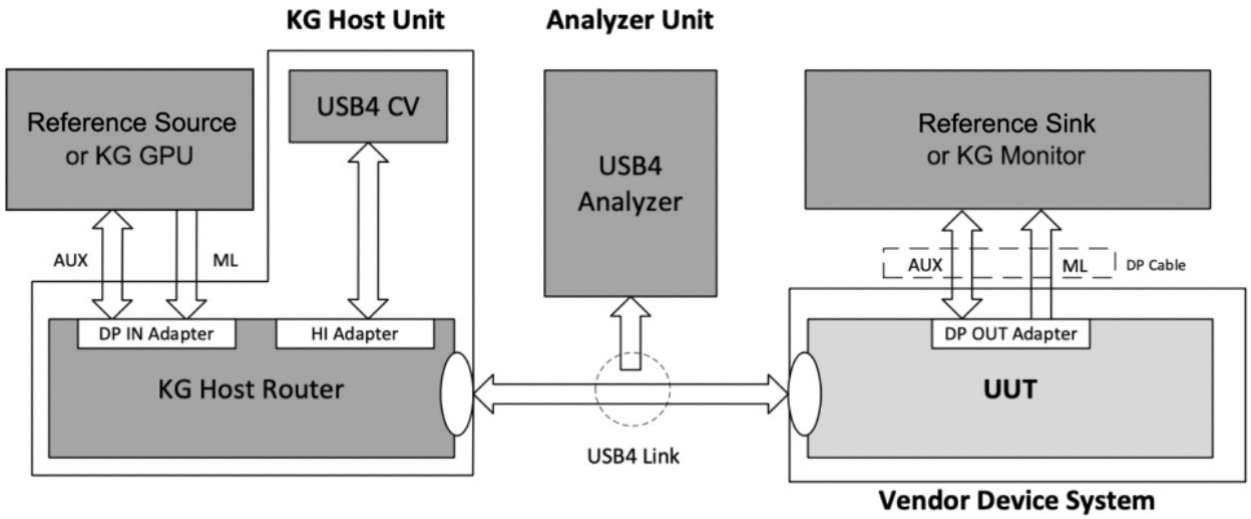
- This may change in the near future, enabling laptops to (more practically) output 9v and/or PPS on their USB-C ports

# USB4


VESA
USB-C Docking Stations in use*
(Global by percentage)
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
DPAM Only
(non-USB4)
USB4
Capable
Takeaway: Design for USB4, but
don't forget about DP Alt Mode ☺
Rough Estimation for illustration purposes only
Assumptions:
◦ USB4 gains share @ 20% YoY
◦ Product average lifespan is 10 years
2024
2028
2032
2036
2040
2044
2048

# USB4 Testing

- From *USB4 DP Tunneling CTS Rev 2.6*



# UCD-500 Gen 3

## 16K DP 2.1b Generator & Analyzer

- DP 2.1b Sinks and Sources up to 8K@60Hz
  (16K@60Hz with DSC up to UHBR 20 Bit Rate)
- Supports DP and USB-C connectors
- GPIO interface for external control
- New fan cooler and chassis design
- Adaptive Sync, DSC, FEC and LTTPR support
- DP 2.1b and DP 1.4a Link Layer CTS Tool including DSC, LTTPR, DisplayID/EDID and Adaptive-Sync
- MST (up to 4 streams) with MST CTS Source and Branch DUT
  (full test set for Branch scheduled release in 4Q 2026)
- HDCP 2.3 Compliance Test Device for Transmitters, Receivers and Repeaters
- Color depth 6 to 16bpc
- Capture memory 16GB
- Now featuring Link Analyzer (monitor), *Panel Replay and eDP 1.5 test functions (eDP 2.0 scheduled release in 4Q 2026)

16K UHD

DP 2.1 LL CTS

HDCP 2.3 CTS











*Demo video on Youtube

# Summary

# Summary

- Consider all possible link partners and cabling topologies (not only the cables/accessories that ship in-box)
- Factory testing mistakes are costly; don’t skimp on test engineering development or equipment
- For questions on USB-C product design or testing, don’t hesitate to reach out to us at www.unigraf.fi

# QA

# Afternoon Break

*Sessions will resume at 2:45 pm*

VESA

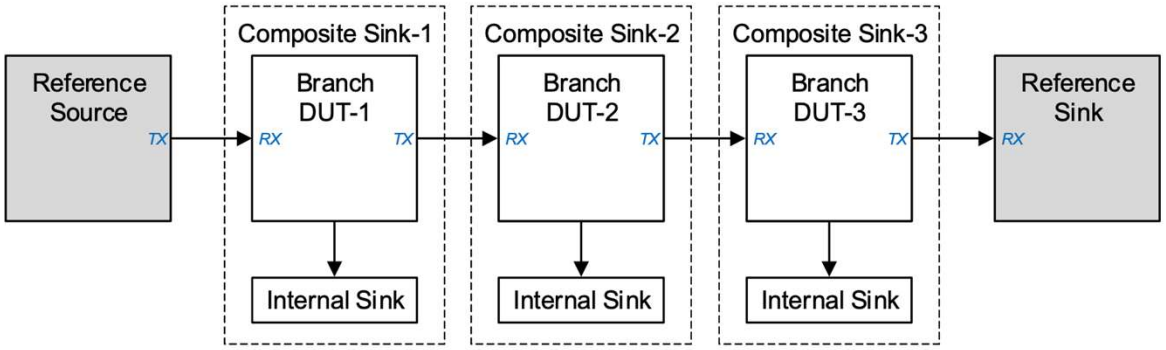
# Compliance Testing

# VESA PlugTest Events

- Provide significant value to VESA compliance program and member companies, particularly as new capabilities and products are deployed.
- Demonstrate and improve traditional interoperability
- Test Native DP and DP Alt Mode over USB Type-C™ products
  - UHBR rates, DSC, New MST Link Layer Tests, FEC, DisplayHDR and other new capabilities
  - Verify Test Equipment Correlation
- VESA hosted two successful PlugTests in 2025 (Taiwan and US)
- VESA hosts two PlugTests in 2026
  - Honolulu, Hawaii USA: **May 2026 (completed)**
  - Taipei, Taiwan: **October 19-23, 2026 (next week)**

# Multi-Stream Transport (MST) Compliance Testing Enhancements

- After over a year of specification and test equipment test development VESA is preparing to release its biggest MST test update since DP 1.2. With the introduction of UHBR20 + DSC, users can now daisy chain multiple 4K/120Hz displays from a single output connector
- The unique DP capability of driving multiple daisy chained displays with a single output connection/cable is increasingly the most popular feature of DP for end users
- To further improve end user experience with MST configurations, VESA's latest DP Link Layer Compliance Test Specification adds dozens of new MST source/sink tests to verify products are implemented according to DP specifications




DP 2.1a LL CTS Composite Sink (Daisy-chainable Sink) Setup 3

# DP54, DP80 and DP80LL Cable Specifications and Certification program

- Work on Enhanced DP cable and connector specifications and test requirements started in 2021 to ensure high performance connectors and cables would be available for products supporting UHBR rates
- DP54 and DP80 Certified cables provide added assurance of proper operation at the highest link rates (UHBR10, UHBR13.5 and UHBR20 Gbps).
- DP80LL active LRD cable CTS and certification added to provide UHBR20 Gbps rate support for longer cables (can support ~3 meter cables)
  - Linear Redrivers (LRD) are level boosting amplifiers that boost signal transmission over longer distances
- Over 150 Enhanced DP cables and connectors have been certified since launch of the Enhanced DP cable and connector certification programs

# Product certifications* 2024/2025/2026

| Products | 2024 | 2025 | 2026 |
|---|---|---|---|
| DP Sources | 93 | 136 | 81 |
| DP Sinks | 491 | 428 | 362 |
| DP Cables | 70 | 57 | 34 |
| DisplayHDR | 556 | 582 | 528 |
| ClearMR | 53 | 71 | 68 |
| AdaptiveSync | 75 | 113 | 122 |

*Note: Numbers are base model certs not including family models. Updates to Compliance Management System (CMS) will include feature to count family models in the future.

# DisplayPort Link Testing
# Source CDF Tool

## Overview

**VESA Workshop**

*Oct 14 2026*

# What is a DisplayPort CDF

- **CDF** stands for Capability Declaration Form.
- A **CDF** is an official document or electronic form that a product manufacturer (OEM or brand) fills out and submits when seeking official DisplayPort Certification.
- **Purpose:** It serves as a detailed checklist recording all the exact capabilities, hardware features, and specifications supported by a DisplayPort transmitter (source, like a graphics card) or receiver (sink, like a monitor).
- **Authorized Test Centers** (ATCs) use the data entered into the CDF to configure automated testing equipment. The test equipment dynamically builds test parameters to verify that the device actually behaves according to the capabilities claimed in its CDF.

# Source CDF Tool

The **Source CDF Tool** is an active Excel Spreadsheet but can be used without enabling Macros

# Source CDF Tool

The **Source CDF Tool** is available to VESA members on the VESA Causeway Test Implementation Subgroup Page

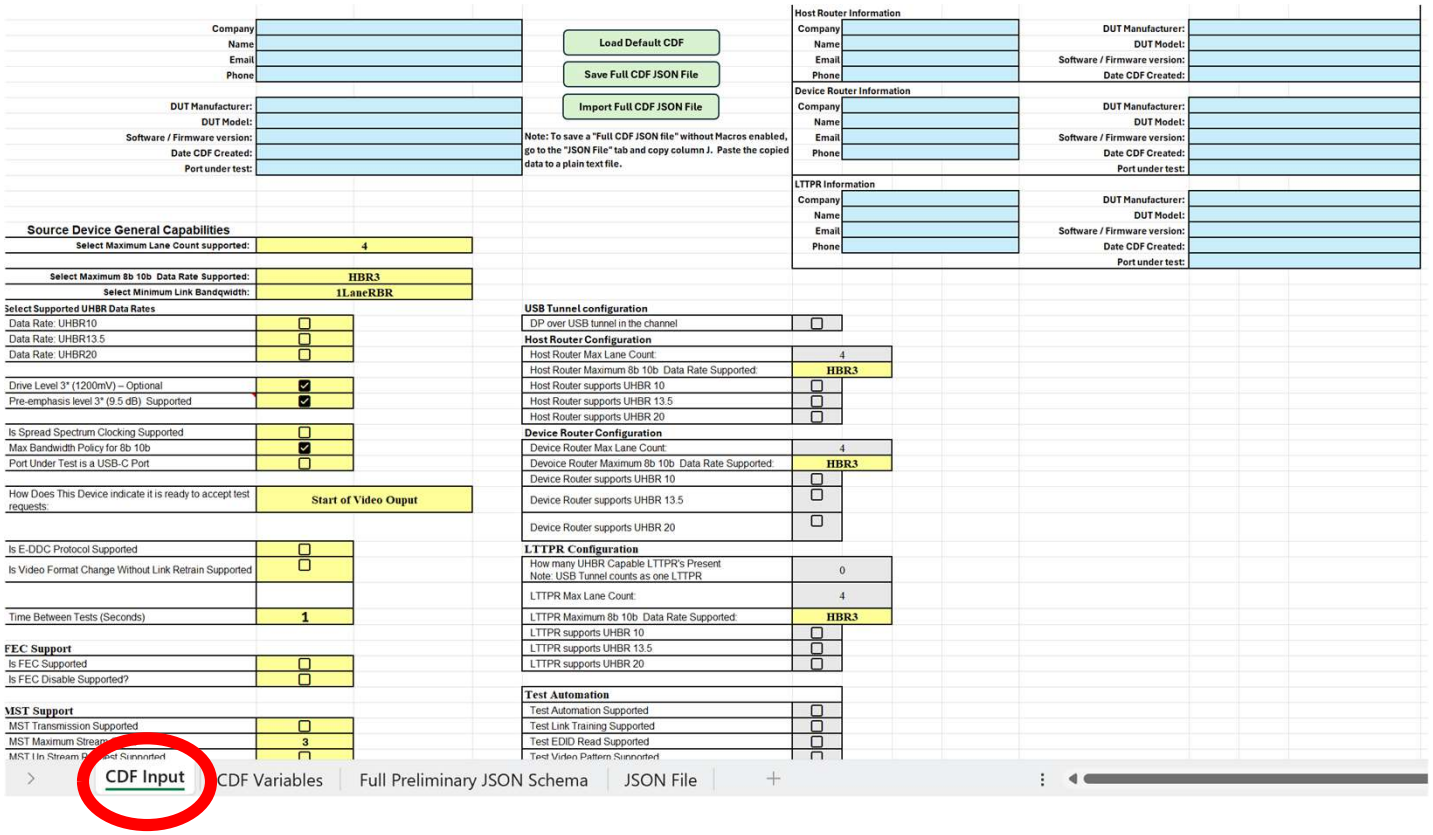
**SourceCDFTool_Beta_xxxx_xx_2026.xlsm**

# Source CDF Tool

The **Source CDF Tool** creates a CDF file in json format that can be imported and used with the two approved Link Test Equipment:
**UCD500** and **M42d / M42de**

# Source CDF Tool

## The Source CDF Tool takes user input in the first "CDF Input" tab



| | |
|---|---|
| Company | |
| Name | |
| Email | |
| Phone | |
| DUT Manufacturer: | |
| DUT Model: | |
| Software / Firmware version: | |
| Date CDF Created: | |
| Port under test: | |

Load Default CDF

Save Full CDF JSON File

Import Full CDF JSON File

Note: To save a "Full CDF JSON file" without Macros enabled, go to the "JSON File" tab and copy column J. Paste the copied data to a plain text file.

| Host Router Information | | | |
|---|---|---|---|
| Company | | DUT Manufacturer: | |
| Name | | DUT Model: | |
| Email | | Software / Firmware version: | |
| Phone | | Date CDF Created: | |

| Device Router Information | | | |
|---|---|---|---|
| Company | | DUT Manufacturer: | |
| Name | | DUT Model: | |
| Email | | Software / Firmware version: | |
| Phone | | Date CDF Created: | |
| | | Port under test: | |

| LTTPR Information | | | |
|---|---|---|---|
| Company | | DUT Manufacturer: | |
| Name | | DUT Model: | |
| Email | | Software / Firmware version: | |
| Phone | | Date CDF Created: | |
| | | Port under test: | |

**Source Device General Capabilities**

| | |
|---|---|
| Select Maximum Lane Count supported: | 4 |
| Select Maximum 8b 10b Data Rate Supported: | HBR3 |
| Select Minimum Link Bandqwidth: | 1LaneRBR |

| Select Supported UHBR Data Rates | |
|---|---|
| Data Rate: UHBR10 | ☐ |
| Data Rate: UHBR13.5 | ☐ |
| Data Rate: UHBR20 | ☐ |
| Drive Level 3* (1200mV) – Optional | ☑ |
| Pre-emphasis level 3* (9.5 dB) Supported | ☑ |
| Is Spread Spectrum Clocking Supported | ☐ |
| Max Bandwidth Policy for 8b 10b | ☑ |
| Port Under Test is a USB-C Port | ☐ |
| How Does This Device indicate it is ready to accept test requests: | Start of Video Ouput |
| Is E-DDC Protocol Supported | ☐ |
| Is Video Format Change Without Link Retrain Supported | ☐ |
| Time Between Tests (Seconds) | 1 |

| FEC Support | |
|---|---|
| Is FEC Supported | ☐ |
| Is FEC Disable Supported? | ☐ |

| MST Support | |
|---|---|
| MST Transmission Supported | ☐ |
| MST Maximum Stream | 3 |
| MST Up Stream Request Supported | ☐ |

| USB Tunnel configuration | |
|---|---|
| DP over USB tunnel in the channel | ☐ |

| Host Router Configuration | |
|---|---|
| Host Router Max Lane Count: | 4 |
| Host Router Maximum 8b 10b Data Rate Supported: | HBR3 |
| Host Router supports UHBR 10 | ☐ |
| Host Router supports UHBR 13.5 | ☐ |
| Host Router supports UHBR 20 | ☐ |

| Device Router Configuration | |
|---|---|
| Device Router Max Lane Count: | 4 |
| Devoice Router Maximum 8b 10b Data Rate Supported: | HBR3 |
| Device Router supports UHBR 10 | ☐ |
| Device Router supports UHBR 13.5 | ☐ |
| Device Router supports UHBR 20 | ☐ |

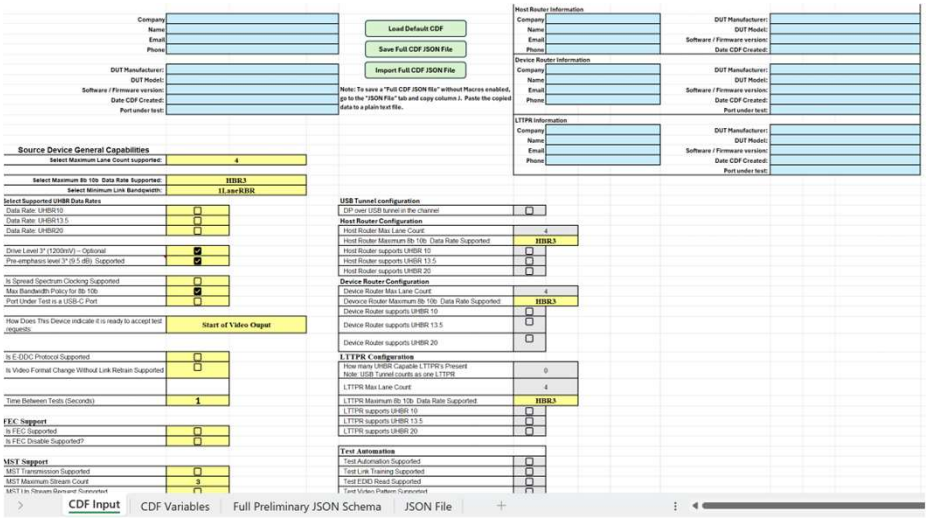
| LTTPR Configuration | |
|---|---|
| How many UHBR Capable LTTPR's Present Note: USB Tunnel counts as one LTTPR | 0 |
| LTTPR Max Lane Count: | 4 |
| LTTPR Maximum 8b 10b Data Rate Supported: | HBR3 |
| LTTPR supports UHBR 10 | ☐ |
| LTTPR supports UHBR 13.5 | ☐ |
| LTTPR supports UHBR 20 | ☐ |

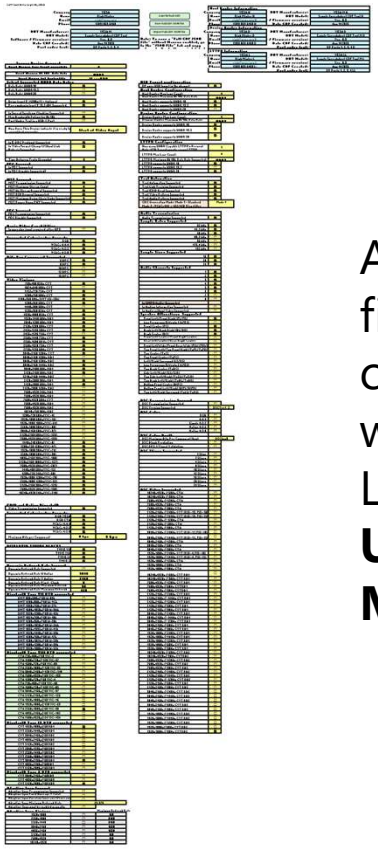
| Test Automation | |
|---|---|
| Test Automation Supported | ☐ |
| Test Link Training Supported | ☐ |
| Test EDID Read Supported | ☐ |
| Test Video Pattern Supported | ☐ |

CDF Input | CDF Variables | Full Preliminary JSON Schema | JSON File

# Source CDF Tool

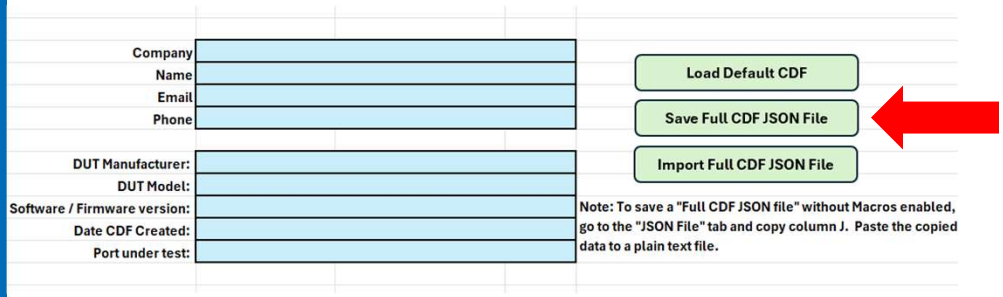
**The Source CDF Tool allows full CDF User Input (up to 330+ input fields)**

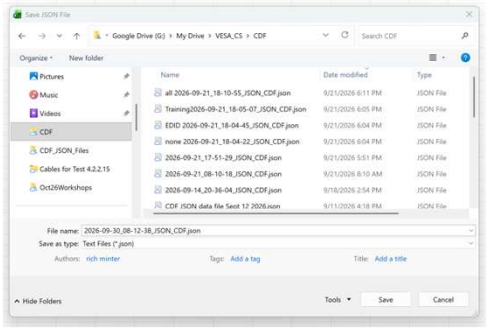


Allows input for every field required for compliance testing with the two approved Link test tools: **UCD500** and **M42d / M42de**

# Source CDF Tool



After completing the CDF input information, the CDF JSON file can be saved. A file save dialog will open to allow saving the CDF JSON file.

**Note: If Macros are not enabled in your excel application, you may save the JSON file manually**

# Source CDF Tool

A comprehensive Source CDF Tool Tutorial has instructions to load CDF files into the Test Equipment

M42de: Instructions to load a CDF file see: Slide 16 - 22

UCD500: Instructions to load a CDF file see: Slide 23 - 27

The Source CDF Tool Tutorial is available on VESA Causeway Test Implementation Subgroup Documents Page:

Source CDF Tool Tutorial.ppsx

END

VESA

# Summary

# Summary

- VESA-based product shipments and certifications have transitioned from rapid growth to a steady state of high-volume output.
- DP 2.1 UHBR capable product development and certifications are in mass production and continue to grow
- VESA Enhanced cable and connector certification programs have been very successful with significant numbers of DP54, DP80 and now DP80LL cables certified
- MST continues to be a popular DP feature and with UHBR20 + DSC it can be used to drive multiple high resolutions displays at high refresh rates through a single connector
- Display Performance Standards adoption and certification have been extremely successful the last several years
- Development and adoption of new technologies continues to drive steady VESA membership growth



# Questions?

# Thank you to the contributors that made this event possible

- ***Thank you, speakers.*** For donating your time, energy and expertise
- ***Thank you, VESA organizing staff.*** The detailed work of arranging these events is tedious and tiring but critical.
- ***Thank you, attendees.*** You are why we are here. Let us know how we did in feedback and include any suggestions for additional topics or improvement for next year.

VESA

# THANK YOU

DisplayPort.org
DisplayHDR.org
ClearMR.org
AdaptiveSync.org
VESA.org